P²CCD filter combination for CVBS and S-VHS

TDA8453A

GENERAL DESCRIPTION

The TDA8453A is an integrated P²CCD (Profiled Peristaltic Charge Coupled Device) filter combination which can accommodate CVBS and S-VHS input signals. The device has been designed to be used in conjunction with various colour decoders and incorporates a luminance delay with chrominance trap, a chrominance bandpass filter, a wideband delay line, clock drivers for the filters which are driven from an internal VCO locked to the 2 x f_{sc} signal (obtained from the decoder oscillator), a video switch for three different input signals (2 x CVBS and 1 luminance S-SVHS) and a switch for the chrominance S-VHS. This IC replaces TDA8453.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8453A	18	DIL	plastic	SOT102RG.4

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	supply voltage					
$V_{p(a)}$	analog (pin 3)		10.8	12.0	13.2	V
$V_{p(d)}$	digital (pin 13)		10.8	12.0	13.2	V
	supply current					
$I_{p(a)}$	analog (pin 3)		12	22	30	mA
$I_{p(d)}$	digital (pin 13)		20	50	70	mA
$V_{I(p-p)}$	CVBS input (pins 16 and 18) (peak-to-peak value)		–	0.7	1.0	V
$V_{I(p-p)}$	Y-SVHS input (pin 2) (peak-to-peak value)		–	1.0	1.42	V
$V_{I(p-p)}$	C-SVHS input (pin 10) (peak-to-peak value)		–	660	935	mV
$V_{6(p-p)}$	luminance output for CVBS (pin 6) (peak-to-peak value)		–	0.45	–	V
$V_{6(p-p)}$	luminance output for S-VHS (pin 6) (peak-to-peak value)		–	0.45	–	V
$V_{8(p-p)}$	chrominance output for CVBS (pin 8) (peak-to-peak value)		425	600	850	mV
$V_{8(p-p)}$	chrominance output for S-VHS (pin 8) (peak-to-peak value)		525	594	660	mV
$V_{4(p-p)}$	delayed CVBS output (pin 4) (peak-to-peak value)		–	1.0	–	V
$V_{4(p-p)}$	delayed S-VHS output (pin 4) (peak-to-peak value)		–	0.9	–	V
R_O	output resistance (pins 4, 6 and 8)		300	500	800	Ω
$V_{12(p-p)}$	oscillator input signal (peak-to-peak value)	2 x f_{sc}	200	–	–	mV

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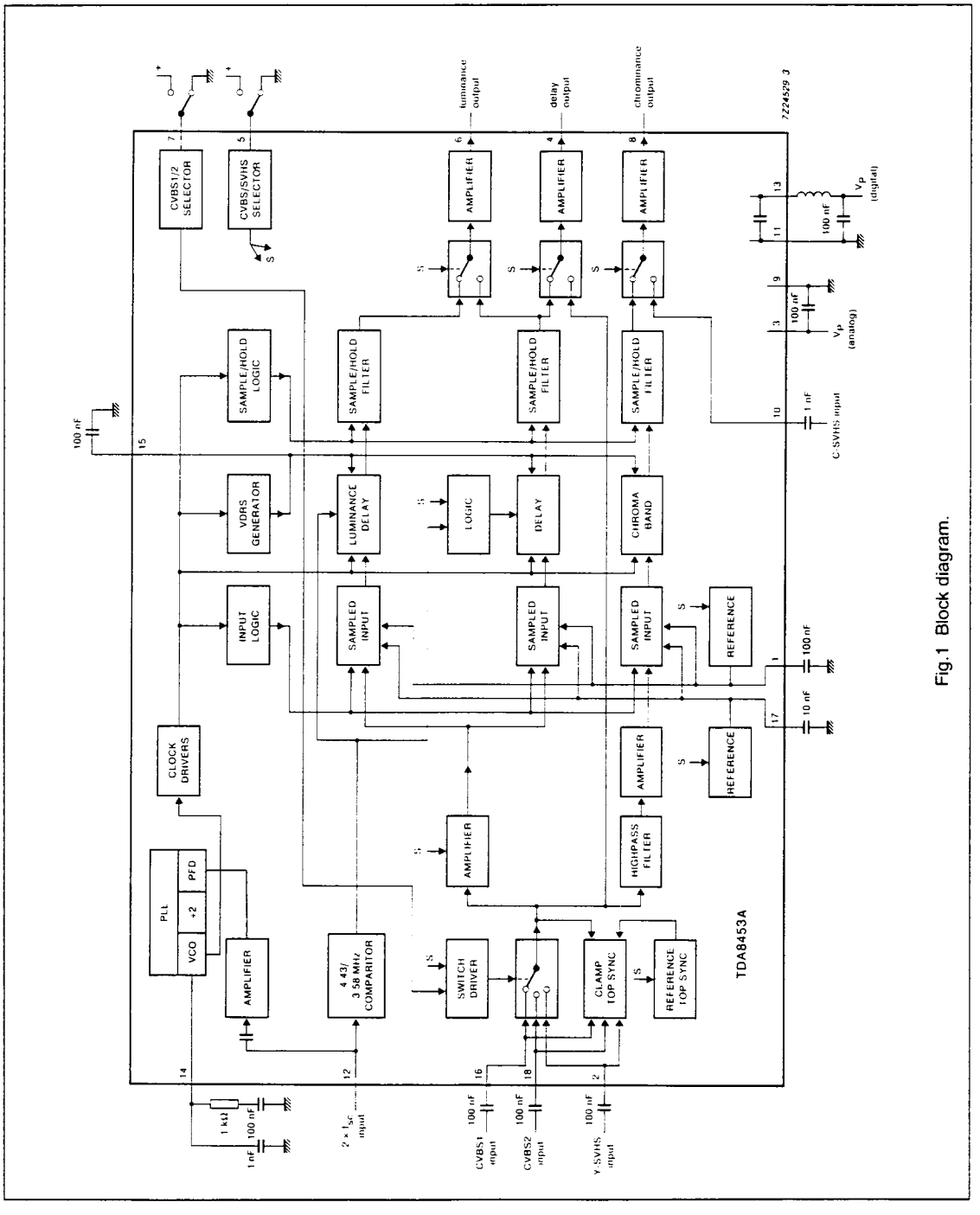

Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The device has four AC-coupled video inputs; CVBS1 (pin 16), CVBS2 (pin 18), luminance S-VHS (Y-SVHS pin 2) and chrominance S-VHS (C-SVHS pin 10).

CVBS1, CVBS2 and S-VHS selectors (pins 5 and 7)

The device can accommodate three different video input signals:

- CVBS1 pins 5 and 7 LOW
- CVBS2 pin 5 LOW, pin 7 HIGH
- S-VHS contains Y-SVHS and C-SVHS; pin 5 HIGH

The slicing level of the CVBS/S-VHS selector and of the CVBS1/CVBS2 selector are different. This means, therefore, that the selectors can be controlled with one signal wire that has three different levels (e.g. by the TDA8466).

CVBS inputs (pins 16 and 18)

When either input is selected by the input switch the signal is routed through three separate paths before being applied to the sample-and-hold filter stages. The paths are via:

- A delay line used to drive the sync separator circuit, teletext and SECAM decoders etc.
- A luminance delay line with chrominance trap
- A chrominance bandpass filter.

The sample-and-hold lowpass filter stages are used to reduce the clock signals. For the 3.58 MHz TV systems the luminance signal will 'skip' part of the delay line to ensure equal delay times in the chrominance and luminance paths.

PINNING

PIN	DESCRIPTION
1	reference decoupling
2	luminance S-VHS input
3	analog supply voltage input
4	delayed CVBS output or undelayed Y-SVHS output
5	CVBS/S-VHS input selector
6	luminance output
7	CVBS1/CVBS2 input selector
8	chrominance output
9	analog ground
10	chrominance S-VHS input
11	digital ground
12	2 x f_{sc} plus 4.43/3.58 MHz selector input
13	digital supply voltage input
14	PLL filter
15	voltage drain reset generator decoupling
16	CVBS1 input
17	reference decoupling
18	CVBS2 input

S-VHS inputs (pins 2 and 10)

If the CVBS/S-VHS selector is in the S-VHS position (pin 5 HIGH), the luminance signal will be routed through two separate paths. The paths are:

- Directly through the input switch to the output switch (pin 4). This signal is used to drive the sync separator circuit
- Via a luminance delay without chrominance trap.

The chrominance S-VHS signal is routed directly to the chrominance output switch (pin 8).
To ensure that the delay of the luminance signal in both the 4.43 MHz and 3.58 MHz TV systems are equal to the total delay of the chrominance S-VHS signal (which is the sum of the delays in the decoder and the delay line IC), the delay line incorporates more stages in the 4.43 MHz TV system than the 3.58 MHz TV system.

Luminance, chrominance and delayed outputs (pins 6, 8 and 4)

The position of the three output switches depends on the selected input (CVBS or S-VHS). The device also incorporates three output amplifiers:

Luminance output (pin 6)

- CVBS luminance delay with chrominance trap
- S-VHS delayed Y-SVHS without chrominance trap

Delay output (pin 4)

- CVBS delayed CVBS signal
- S-VHS undelayed Y-SVHS signal

Chrominance output (pin 8)

- CVBS chrominance bandpass filter with delay
- S-VHS undelayed C-SVHS signal without bandpass filter

Because the amplitude of the CVBS and S-VHS input signals are different, the gain of the input amplifiers and the level of top sync are varied to obtain optimal biasing if S-VHS is selected.

Oscillator (pins 12 and 14)

The reference for the PLL is obtained from the decoder IC which derives the 2 x f_{sc} signal from its reference oscillator (the amplitude of this signal may be small, minimum 200 mV(p-p)). The VCO operates at 4 x f_{sc}, the delay lines and filters are 4 phase clocked at 4 x f_{sc}.
The information whether the incoming signal is 2 x 3.58 MHz or 2 x 4.43 MHz is generated in the decoder IC and fed to the TDA 8453A via the DC level of the 2 x f_{sc} oscillator signal (pin 12). The filter for the PLL is connected to pin 14.

Voltage drain reset generator decoupling (pin 15)

The TDA8453A requires a supply voltage of 12 V. The output stages require a higher voltage (approximately 15 V). This voltage is generated internally with a decoupling capacitor connected to pin 15.

Decoupling reference (pins 1 and 17)

The reference for the sampled inputs of the delay lines and filters are decoupled externally. When S-VHS is selected the reference will vary to give an optimum bias for the sampled input to enable it to adapt to the change in amplification.

A circuit for the TDA8453A together with a PAL decoder (TDA8391) is illustrated in Fig.6. A circuit for the TDA8453A together with a PAL/NTSC decoder (TDA8466) and a SECAM decoder (TDA8490) is illustrated in Fig.7. The TDA8490 can also be used in combination with the TDA8391.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{p(a)}$	analog supply voltage	–	13.2	V
$V_{p(d)}$	digital supply voltage	–	13.2	V
P_{tot}	total power dissipation	–	1.45	W
T_{amb}	operating ambient temperature range	−25	+70	°C
T_{stg}	storage temperature range	−55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	55	–	K/W

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (note 1)						
$V_{p(a)}$	analog supply voltage (pin 3)		10.8	12.0	13.2	V
$I_{p(a)}$	analog supply current (pin 3)		12	22	30	mA
SVRR	supply voltage ripple rejection at 100 mVeff (pin 3)	f = 100 Hz	–	7	–	db
$V_{p(d)}$	supply voltage digital (pin 13)		10.8	12.0	13.2	V
$I_{p(d)}$	supply current digital (pin 13)		20	50	70	mA
SVRR	supply voltage ripple rejection at 100 mVeff (pin 13)	f = 100 Hz	–	7	–	dB
P_{tot}	total power dissipation		–	0.86	1.3	W
Composite video inputs (pins 16 and 18)						
AC COUPLED AND CLAMPED ON TOP SYNC (NOTE 2)						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	0.7	1.0	V
I_I	input current	non-selected input	–	–	0.1	µA
I_I	input current during non-clamping period of selected input		1.0	3.0	5.0	µA
C_I	input capacitance		–	5	–	pF
α	suppression of any other input signal when CVBS1 or CVBS2 is selected (0 to 5 MHz)	R_i = 75 Ω	–	50	–	dB
Y-SVHS input (pin 2)						
AC COUPLED AND CAMPLED ON TOP SYNC; NOTE 3						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	1.0	1.42	V
I_I	input current	non-selected input	–	–	0.1	µA
I_I	input current during non-clamping period of selected input		1.0	3.0	5.0	µA
C_I	input capacitance		–	5	–	pF
α	suppression of any other input signal when Y-SVHS is selected (0 to 5 MHz)	R_i = 75 Ω	–	50	–	dB
C-SVHS input (pin 10); note 4						
$V_{I(p-p)}$	input signal (peak-to-peak value)		–	660	935	mV
R_I	input resistance		4	6	12	kΩ
C_I	input capacitance		–	4	–	pF
α	suppression of any other input signal when C-SVHS is selected (3.8 to 4.9 MHz)	R_i = 75 Ω	–	50	–	dB
CVBS switch control (pin 7)						
V_7	CVBS1 input (pin 16)	pin 5 LOW	0	–	1.5	V
V_7	CVBS2 input (pin 18)	pin 5 LOW	4	–	V_P	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS/S-VHS switch control (pin 5)						
V_5	CVBS1 or CVBS2 input		0	–	6.8	V
V_5	S-VHS input (pins 2 and 10)		8.2	–	V_P	V
PLL reference input signal (pin 12)						
$V_{12(p-p)}$	input signal (peak-to-peak value)	2 x f_{sc}	200	–	–	mV
C_I	input capacitance		–	6	–	pF
R_I	input resistance		1	–	–	MΩ
V_{12}	DC level for: 4.43 MHz signal 3.58 MHz signal		 0 6.7	 – –	 5.3 V_P	 V V
Luminance signal output (pin 6)						
R_O	output resistance		300	500	800	Ω
V_6	output level for top sync		3	–	7	V
I_6	luminance output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio		–	60	–	dB
Luminance signal output for CVBS (pin 5 LOW); note 2						
$V_{6(p-p)}$	output signal (peak-to-peak value)	CVBS input signal = 0.7 V	–	0.45	–	V
$V_{6(p-p)}$	black-to-white output signal (peak-to-peak value)	note 2	225	320	450	mV
$V_{6(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{6(p-p)}$	linearity black-to-white (peak-to peak-value)	note 7 CVBS input signal = 0.7 V CVBS input signal = 1.0 V	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	3.7	3.8	–	MHz
Δf	frequency response with regard to 0 MHz (Fig.2) at 2.2 MHz at 3.0 MHz at 3.8 MHz at 4.26 MHz at 4.43 MHz at 4.64 MHz at 5.5 MHz		 –1.0 –0.5 –4.0 –20 – –18 –5.0	 0.5 1.0 –2.5 –15 –25 –12 –2.0	 2.0 2.5 –1.0 –12 –20 –10 1.0	 dB dB dB dB dB dB dB
t_d	luminance signal delay at 8.87 MHz reference input at 7.16 MHz reference input		 2060 2270	 2090 2300	 2120 2330	 ns ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Luminance signal output for S-VHS (pin 5 HIGH); note 3						
$V_{6(p-p)}$	output signal	V_2 = 1 V(p-p)	–	0.45	–	V
$V_{6(p-p)}$	black-to-white output signal (peak-to-peak value)	note 3	225	320	450	mV
$V_{6(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{6(p-p)}$	linearity black-to-white	note 7 V_2 = 1 V(p-p) V_2 = 1.42 V(p-p)	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	5.5	6.5	–	MHz
Δf	frequency response with regard to 0 MHz (Fig.3) at 2.2 MHz at 3.0 MHz at 4.43 MHz at 5.5 MHz		 0 0.5 1.0 –1.0	 1.0 1.5 2.0 0.5	 2.5 3.0 3.5 +2.0	 dB dB dB dB
t_d	luminance signal delay at 8.87 MHz reference input at 7.16 MHz		 1045 1010	 1075 1040	 1105 1070	 ns ns
Chrominance signal output (pin 8)						
R_0	output resistance		300	500	800	Ω
V_8	DC output level		3.0	–	7.5	V
I_8	chrominance output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio	note 5	–	65	–	dB
Chrominance signal output for CVBS						
$V_{8(p-p)}$	output signal (peak-to-peak value)	V_{16-18} = 0.465 V(p-p)	425	600	850	mV
$V_{8(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 6	 – – –	 – – –	 0.2 10 12	 mV mV mV
$L_{8(p-p)}$	linearity of output signals	note 7 V_{16-18} = 0.465 V(p-p) V_{16-18} = 0.66 V(p-p)	 – –	 0.97 0.95	 – –	
B	bandwidth	at –3 dB	–	1.15	–	MHz
Δf	frequency response with regard to 4.43 MHz (Fig.4) at 0.9 MHz at 1.9 MHz at 2.5 MHz at 3.0 MHz at 3.8 MHz at 4.93 MHz at 5.6 MHz		 – – – – –3.5 –4.0 –	 –20 –35 –30 –20 –2.5 –3.0 –16	 –15 –30 –25 –16 –1.5 –2.0 –14	 dB dB dB dB dB dB dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Chrominance signal output for CVBS						
t_d	chrominance filter delay					
	at 8.87 MHz reference input		990	1020	1050	ns
	at 7.16 MHz reference input		1220	1250	1280	ns
Chrominance signal output for S-VHS (pin 5 HIGH); note 4						
$V_{8(p-p)}$	output signal (peak-to-peak value)	V_8 = 0.66 V(p-p)	525	594	660	mV
$V_{8(rms)}$	rest clock signals (RMS value)	note 6				
	at 4.43 MHz		–	–	0.2	mV
	at 8.87 MHz		–	–	10	mV
	at 17.73 MHz		–	–	12	mV
$L_{8(p-p)}$	linearity of the output signal	note 7				
		$V_{16,\ 18}$ = 0.66 V(p-p)	0.97	–	–	
		$V_{16,\ 18}$ = 0.935 V(p-p)	0.95	–	–	
B	bandwidth	at –3 dB	6.0	–	–	MHz
Δf	frequency response with regard to 4.43 MHz					
	at 0.9 MHz		–0.5	0	+0.5	dB
	at 3.0 MHz		–0.5	0	+0.5	dB
	at 5.6 MHz		–1.0	0	+0.5	dB
t_d	chrominance signal delay		–	30	–	ns
Delayed signal output (pin 4)						
R_0	output resistance		300	500	800	Ω
V_4	output level for top sync		2.5	–	7.0	V
I_4	delayed output internal load		0.4	–	1.5	mA
S/N	signal-to-noise ratio	note 5	–	65	–	dB
Delayed signal output for CVBS						
$V_{4(p-p)}$	output signal (peak-to-peak value)	input signal = 0.7 V CVBS(p-p)	–	1.0	–	V
$V_{4(p-p)}$	black-to-white output signal (peak-to-peak value)	note 2	0.49	0.70	0.98	V
$V_{4(p-p)}$	output sync pulse (peak-to-peak value)	input sync pulse = 210 mV(p-p)	210	–	–	mV
$V_{4(rms)}$	rest clock signals (RMS value)	note 4				
	at 4.43 MHz		–	–	1	mV
	at 8.87 MHz		–	–	10	mV
	at 17.73 MHz		–	–	12	mV
$L_{4(p-p)}$	linearity black-to-white	note 7				
		$V_{16,\ 18}$ = 0.7 V(p-p)	0.95	–	–	
		$V_{16,\ 18}$ = 1 V(p-p)	0.94	–	–	
B	bandwidth	at –3 dB	5.5	6.5	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Delayed signal output for CVBS						
Δf	frequency response with regard to 0 MHz (Fig.5) at 0.9 MHz at 2.2 MHz at 3.1 MHz at 5.5 MHz		 –0.5 0 0 –3.0	 0.5 1.0 1.5 –1.5	 1.5 2.5 2.5 0.5	 dB dB dB dB
t_d	CVBS signal delay at 8.87 MHzreference input at 7.16 MHz reference input		 595 730	 695 760	 655 790	 ns ns
Delayed signal output for S-VHS (pin 5 HIGH); note 3						
$V_{4(p-p)}$	output signal (peak-to-peak value)	V_2 = 1 V(p-p)	–	0.9	–	V
$V_{4(p-p)}$	black-to-white output signal (peak-to-peak value)	note 3	0.55	0.63	0.70	V
$V_{4(p-p)}$	output sync pulse (peak-to-peak value)	input sync pulse = 300 mV(p-p)	210	–	–	mV
$V_{4(rms)}$	rest clock signals (RMS value) at 4.43 MHz at 8.87 MHz at 17.73 MHz	note 4	 – – –	 – – –	 1 10 12	 mV mV mV
$L_{4(p-p)}$	linearity black-to-white	note 7 V_2 = 1 V(p-p) V_2 = 1.42 V(p-p)	 0.95 0.94	 – –	 – –	
B	bandwidth	at –3 dB	6.0	–	–	MHz
Δf	frequency response with regard to 0 MHz at 2.2 MHz at 5.5 MHz		 –0.5 –1.0	 0 0	 0.5 0.5	 dB dB
t_d	Y-SVHS signal delay		–	40	–	ns

Notes to the characteristics

1. To prevent linearities and rest clock signals from deteriorating, it is recommended that the difference between the supply voltages at pins 3 and 13 should be less than 500 mV.
2. Unless otherwise specified all figures are related to a CVBS input signal of 0.7 V(p-p); 100% contrast; 75% saturation.

   In this condition the input signal is formed by the following components:

   210 mV(p-p) sync pulse

   490 mV(p-p) black-to-white

   465 mV(p-p) chrominance
3. The figures are related to a Y-SVHS input signal of 1 V(p-p), 100% contrast. In this condition the input signal is formed by the following components:

   300 mV(p-p) sync pulse

   700 mV(p-p) luminance

Notes to the characteristics

4. The figures are related to a C-SVHS input signal of 660 mV(p-p). This amplitude corresponds to a video signal of 1 V(p-p). 100% contrast and 75% saturation.
5. The signal-to-noise ratio is specified as nominal $V_{out(p-p)}/V_{noise(rms)}$ (0 to 5 MHz).
6. The rest clock signals are measured with an FET probe (3.5 pF in parallel with a 1 MΩ resistor) connected directly to pins 4 and 9, pins 6 and 9 or pins 8 and 9.
7. The linearity is defined as the amplification at the given input voltage swing, divided by the amplification when the input voltage swing is decreased to 70%.

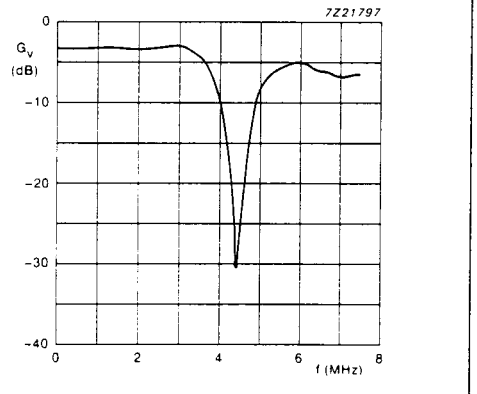

Fig.2 Typical frequency response of luminance signal (CVBS).

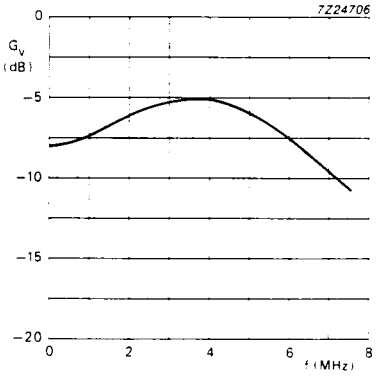

Fig.3 Typical frequency response of luminance signal (S-VHS).

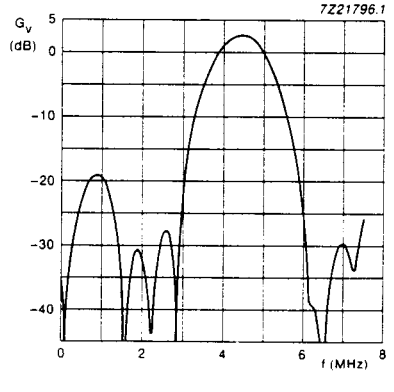

Fig.4 Typical frequency response of chrominance signal (CVBS).

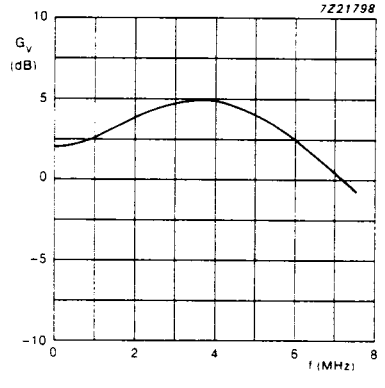

Fig.5 Typical frequency response of delayed signal (CVBS).

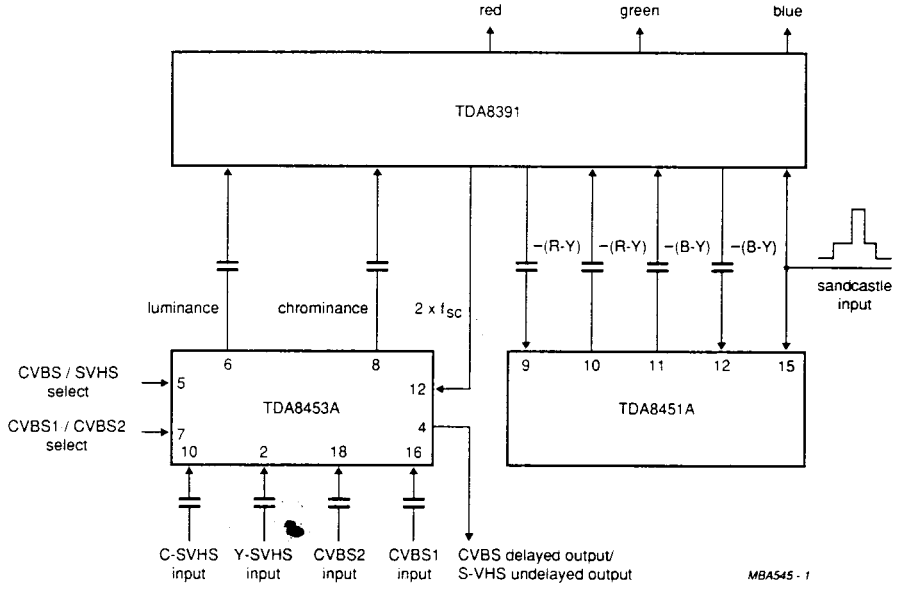

Fig.6 PAL decoder configuration.

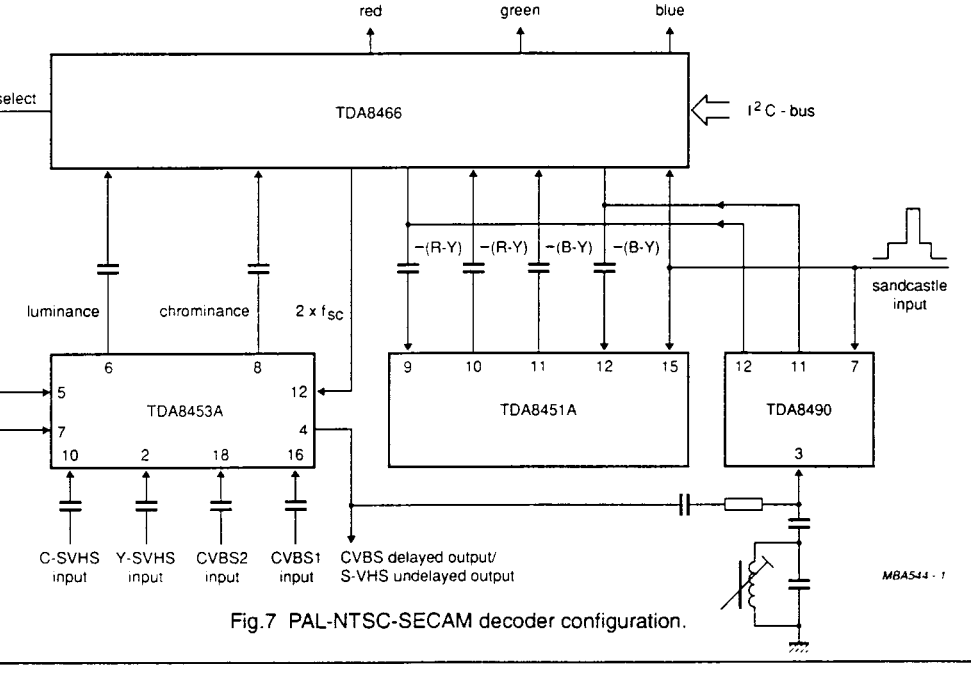

Fig.7 PAL-NTSC-SECAM decoder configuration.