TDA8587J

4 × 25 W BTL power amplifier and multiple voltage regulator with power switch

Rev. 01 — 23 December 2004 Preliminary data sheet

1. General description

The TDA8587J is a combination of a quad Bridge-Tied Load (BTL) power amplifier, a multiple voltage regulator and a power switch. Several protections and diagnostic options (e.g. DIAG, WARN) are incorporated in this design.

This device is primarily developed to cover the complete power supply and audio amplifier requirements in low and mid-end car radio applications.

The switchable regulators (regulators 1, 3 and 4) are intended to be used as supplies for the tuner, logic, digital or analog sound processor and CD / tape control.

The standby regulator (regulator 2) is specially designed as supply for a microcontroller. In combination with the reset delay capacitor (pin RDC) and the reset output (pin RST), a proper start-up sequence for the microcontroller is guaranteed. The storage capacitor (pin STC) makes this regulator output insensitive for short battery drops (e.g. engine start).

The power switch (pin PSW) can be used for switching e.g. an electrically powered antenna, display unit or CD / tape driver.

The smart combination of two dynamic buffers and four amplifier output stages makes it possible to create a full quad BTL amplifier, using only six output pins.

2. Features

2.1 General

- Protected against ElectroStatic Discharge (ESD)
- Thermal (foldback) protection to prevent overheating
- Load dump/overvoltage protection
- Single mode control pin (standby, operating: mute/on)
- Low standby current (only regulator 2 active)
- Hysteresis on internal switching levels
- Low power dissipation in any short-circuit condition
- Package with flexible leads (easy manual assembly)
- DBS27 package with low thermal resistance

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2.2 Regulator part

- Three mode pin controlled regulators i.e. regulator 1 = 8.5 V, regulator 3 = 5.0 V and regulator 4 = 3.3 V
- One mode pin controlled power switch
- One standby regulator i.e. regulator 2: 5.0 V (e.g. supply for a microcontroller)
- A storage capacitor is present as back-up supply for regulator 2 in case of loss of battery
- All regulator and power switch outputs are short-circuit proof to ground and to the supply lines (current foldback)
- In the event of an internal or external fault condition a warning output can be used to trigger a microcontroller
- A reset output can be used to 'call' a microcontroller in a smooth way (adjustable delay) at the first power-up

2.3 Amplifier part

- Four 25 W BTL power amplifiers, realized in a unique six pin output configuration
- Internally fixed gain (26 dB)
- No switch-on / switch-off plops when switching between standby and mute and between mute and operating
- All amplifier outputs are short-circuit proof to ground, supply lines and across the speakers (soft + hard detection)
- A low supply mute function is implemented to obtain a fast mute at supply voltage drops (e.g. engine start)
- A diagnostic output gives clip information (THD = 10 %), indicates a short-circuit at an amplifier output and gives a thermal foldback pre-warning

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
V_P	supply voltage					
	operating	all modules	8	14.4	18	V
		standby regulator (REG2)	4	14.4	50	V
	jump start	$t \leq 10$ minutes	-	-	30	V
	load dump	$t \leq 50$ ms; $t_r \geq 2.5$ ms	-	-	50	V
I_q	quiescent current					
	standby	V_P = 14.4 V; no loads	-	105	135	µA
	operating	V_P = 14.4 V; no loads	-	200	350	mA
Regulator part						
$V_{o(REG1)}$	output voltage regulator 1	$I_{o(REG1)}$ = 1 mA to 200 mA	8.1	8.5	8.9	V
$V_{o(REG2)}$	output voltage regulator 2	$I_{o(REG2)}$ = 1 mA to 200 mA	4.75	5.0	5.25	V
$V_{o(REG3)}$	output voltage regulator 3	$I_{o(REG3)}$ = 1 mA to 900 mA	4.75	5.0	5.25	V
$V_{o(REG4)}$	output voltage regulator 4	$I_{o(REG4)}$ = 1 mA to 200 mA	3.15	3.3	3.45	V

Table 1: Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{drop(SW)}$	drop-out voltage switch	I_{SW} = 1 A; V_P = 13.5 V	-	0.45	0.7	V
$I_{DC(SW)}$	continuous current switch		1.4	2.0	-	A
$I_{pulse(SW)}$	pulsed current switch		2.5	3.0	-	A
Amplifier part						
V_{OO}	DC output offset voltage	mute	–20	0	+20	mV
		on	–100	0	+100	mV
G_v	voltage gain		25	26	27	dB
P_o	output power	THD = 10 %; V_P = 14.4 V; R_L = 4 Ω	15	17.5	-	W
		square wave; V_P = 14.4 V; R_L = 4 Ω	22	25	-	W
THD	total harmonic distortion	f = 1 kHz; P_o = 1 W	-	0.05	0.3	%
SVRR	supply voltage ripple rejection	mute; f = 1 kHz; V_{ripple} = 0.7 V	55	60	-	dB
ISRR	input signal rejection ratio	mute; f = 1 kHz; V_i = 1 V	100	120	-	dB
α_{ct}	crosstalk	f = 1 kHz; P_o = 1 W; R_s = 10 kΩ	60	70	-	dB
$V_{o(n)}$	noise output voltage	on; R_s = 0 Ω; B = 20 Hz to 20 kHz	-	120	150	μV

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8587J	DBS27P	plastic DIL-bent-SIL power package; 27 leads (lead length 7.7 mm)	SOT521-1

5. Block diagram

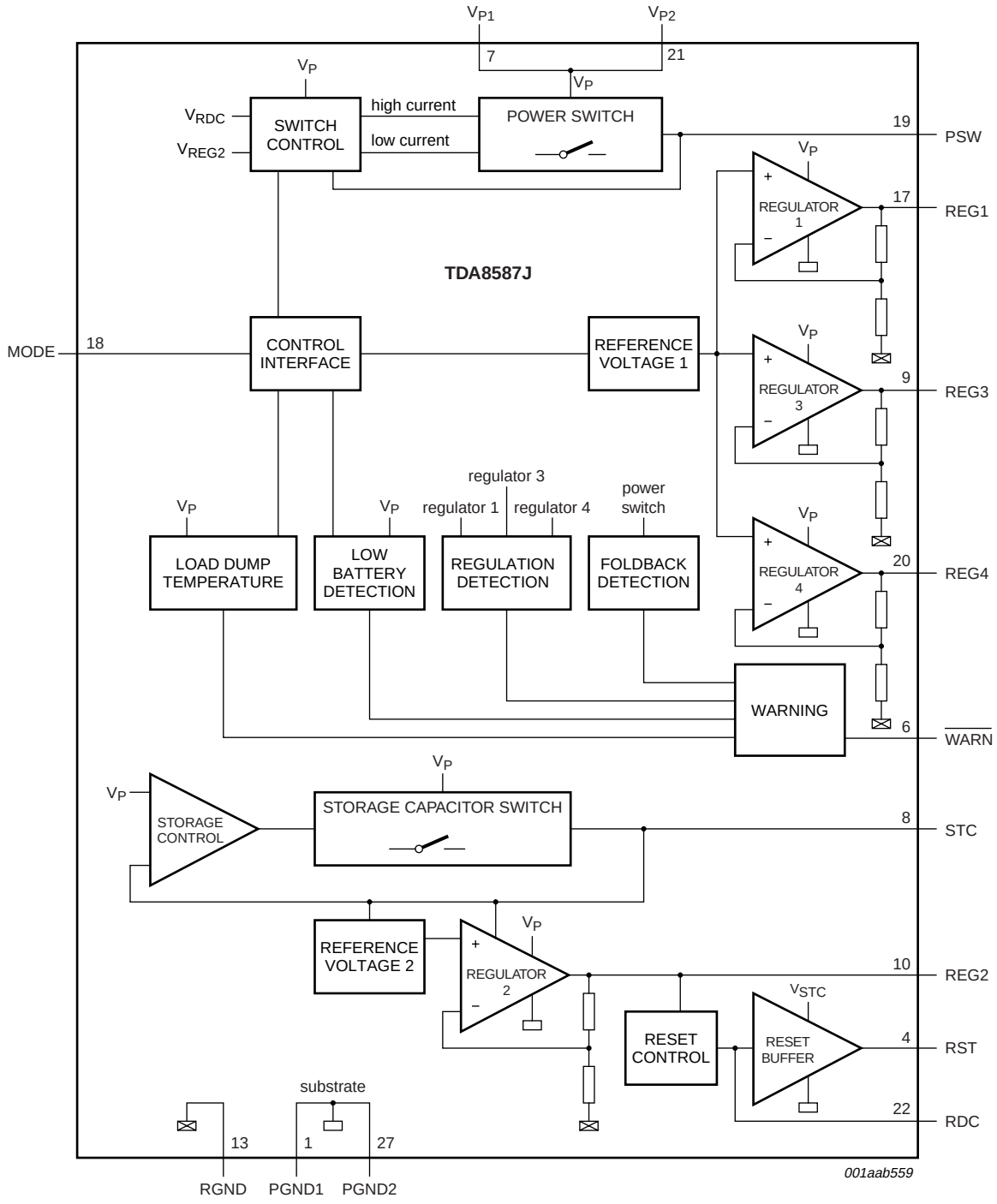


Fig 1. Block diagram (regulator part)

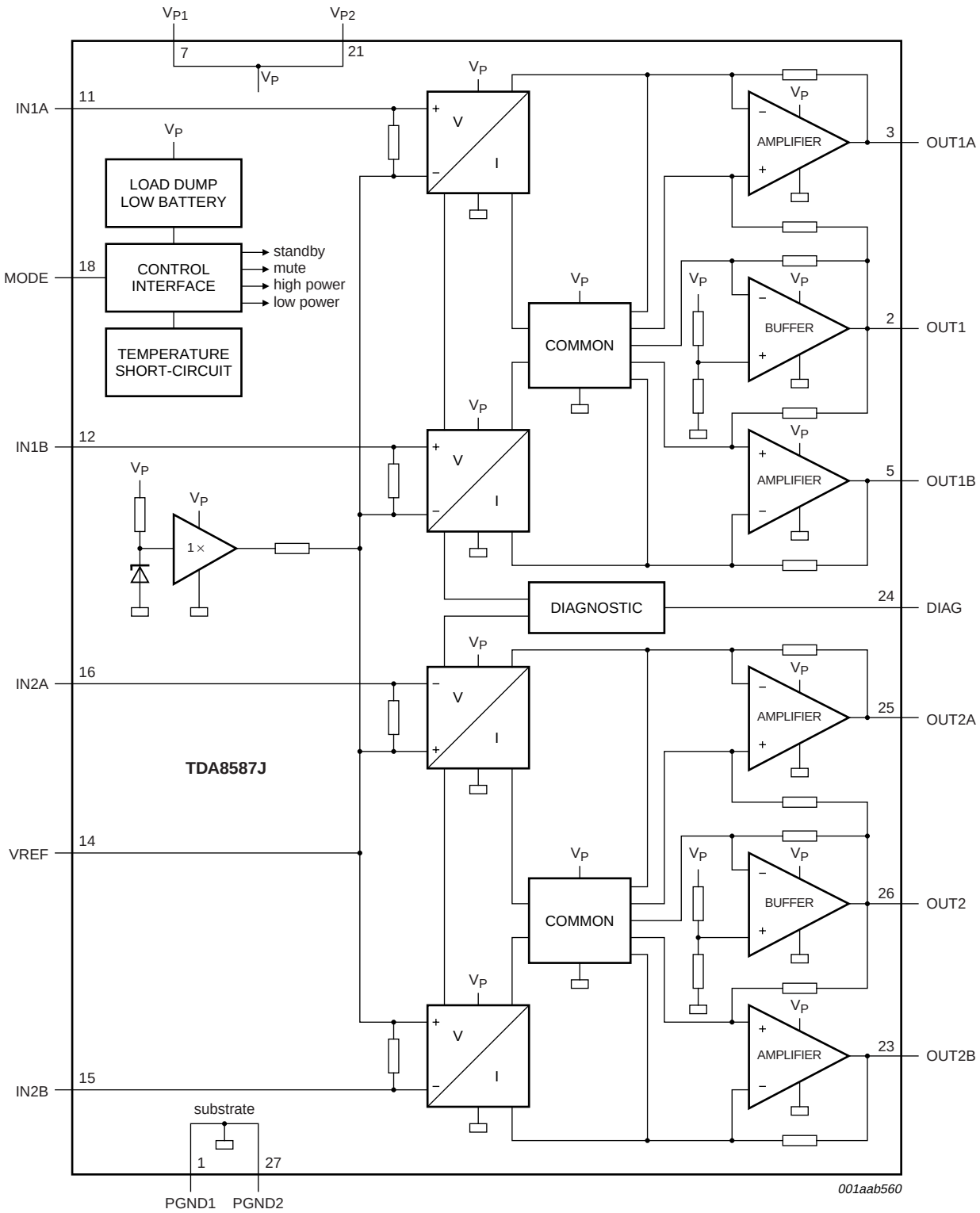


Fig 2. Block diagram (amplifier part)

6. Pinning information

6.1 Pinning

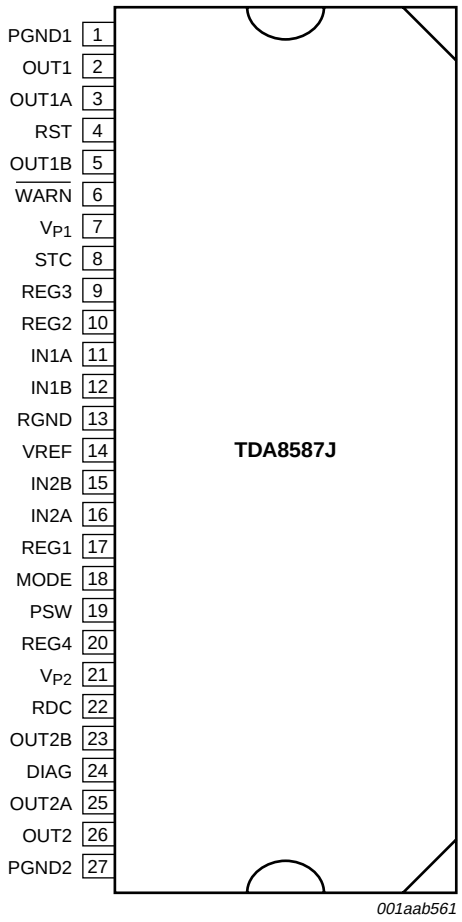


Fig 3. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
PGND1	1	power ground 1
OUT1	2	common audio output 1
OUT1A	3	audio output 1A
RST	4	reset output
OUT1B	5	audio output 1B
$\overline{\text{WARN}}$	6	warning output (active LOW)
V_{P1}	7	supply voltage 1
STC	8	storage capacitor
REG3	9	regulator 3 output (5 V / 900 mA)
REG2	10	regulator 2 output (5 V standby)
IN1A	11	audio input 1A
IN1B	12	audio input 1B
RGND	13	regulator ground
VREF	14	audio reference voltage
IN2B	15	audio input 2B
IN2A	16	audio input 2A
REG1	17	regulator 1 output (8.5 V / 200 mA)
MODE	18	mode select input
PSW	19	power switch output
REG4	20	regulator 4 output (3.3 V / 200 mA)
V_{P2}	21	supply voltage 2
RDC	22	reset delay capacitor
OUT2B	23	audio output 2B
DIAG	24	diagnostic output (active HIGH)
OUT2A	25	audio output 2A
OUT2	26	common audio output 2
PGND2	27	power ground 2 [1]

[1] The heat tab is internally connected to pin PGND2.

7. Functional description

7.1 Mode select input

The mode select input pin (MODE) controls the operating mode of almost the entire device. The following functions are incorporated:

- Standby: all amplifier, regulator and power switch functions (except the standby regulator, storage and reset function) are completely switched off
- Operating: all functions are enabled
- Mute: the audio input signal is suppressed, so the amplifier outputs are only DC-adjusted
- On: complete AC functionality of the amplifier outputs.

When in the on condition ($V_{MODE} \leq V_{REG1}$) the amplifier outputs are capable of delivering full power to the loads (high-power mode). When $V_{MODE} > V_{REG1}$ the output power is internally limited (low-power mode).

The RC combination at pin MODE is obligatory for a correctly operating temperature foldback and a plop-free switch-on and switch-off behavior.

7.2 Switchable regulators (regulator 1, regulator 3 and regulator 4)

Each of these mode pin controlled regulators (REG1 = 8.5 V, REG3 = 5 V and REG4 = 3.3 V) has an overload and short-circuit (foldback) protection.

The regulators will be switched off during load dump or overtemperature conditions.

7.3 Standby regulator (regulator 2)

This 5 V standby regulator also has an individual overload and short-circuit (foldback) protection, but will not be switched off during load dump or overtemperature conditions.

Special design precautions have been taken in this regulator to guarantee a low quiescent current in Standby mode. It is not controlled by the mode pin but it is switched on when the voltage of the storage capacitor (STC) exceeds a certain threshold level and switches off when its own output voltage falls below a given level which is far below the minimum engine start level.

All regulator outputs have to be loaded with a ceramic and an electrolytic capacitor to guarantee stability and optimum noise performance over the complete ambient temperature range.

7.4 Storage capacitor

The storage capacitor is used as a back-up supply for the standby regulator, when the car battery cannot support the supply for this regulator anymore, e.g. in case of cold weather energization of the starter motor.

7.5 Reset output

The reset output pin (RST) is a push-pull output which is able to source and sink current. The output voltage can switch between the ground level and V_{REG2}. This function is also supplied from the storage capacitor in case of low battery.

The reset function is controlled by a low voltage detection circuit which pulls pin RST LOW when V_{REG2} is less than the reset threshold level. When V_{REG2} is greater than the reset threshold level the output goes HIGH.

The timing of this function can be influenced by a reset delay capacitor, e.g. to avoid oscillations when V_{REG2} passes the internal threshold level.

7.6 Reset delay capacitor

The reset delay capacitor is used to delay the reset pulse, starting from the time when the rising V_{REG2} voltage crosses the reset threshold level; this will ensure a clean reset signal to the microcontroller. An internal current source is used to charge the reset delay capacitor and the reset output will be released (go HIGH) when the V_{RDC} crosses the RDC threshold level.

The reset delay capacitor also provides a time constant for the current protection of the power switch (PSW).

7.7 Power switch

The power switch is a non-regulated high current output voltage, which is almost equal to the supply voltage but is clamped in overvoltage conditions to avoid damage to the connected circuitry. It will be switched off during load dump and in overtemperature conditions.

The power switch has three output current modes depending on its output voltage, the reset delay capacitor voltage and the junction temperature, i.e. high current, low current and foldback mode. The power switch can be loaded with light bulbs, relays or electrical motors and therefore, momentarily, excessive currents can flow at the start-up transition. It can operate in the high current mode for a selected time fixed by the reset delay capacitor. After this time-out the PSW output voltage has to be close to the battery voltage otherwise an overload or a short-circuit condition will be present and the power switch will be switched to the low current mode or to the foldback mode.

The power switch can also operate in the low current mode when the standby regulator is overloaded or during excessive junction temperatures, but still below the overtemperature condition.

7.8 Warning output

The output of the warning pin ($\overline{\text{WARN}}$) is an open-collector and therefore must have an external pull-up resistor (e.g. to the standby regulator). This output is active LOW.

The warning output will be activated during the following conditions:

- When the output voltage of one (or more) switched regulator is out of regulation (due to overload during normal operation, supply voltage drops or charging the output capacitors during start-up)
- When the power switch operates in the foldback mode (due to short-circuit during normal operation and the time-out has finished)
- When during operation the overtemperature protection is activated ($T_j \geq 150$ °C)
- When during any mode condition (i.e. standby, mute and on) the load dump protection is activated
- When the circuit is in Standby mode and the battery voltage is very low, to indicate that it is not possible to get all switched regulators into regulation if the circuit is switched on.

7.9 Audio inputs and reference voltage

The audio reference voltage acts with the four signal inputs to provide quasi-differential inputs. The ground side of the capacitor, connected to the audio reference voltage, should be tied to the ground at the signal source, usually the ground at an audio processor.

It should be noted that for design reasons the inputs IN2A and IN2B have the opposite phase compared to inputs IN1A and IN1B. Care should be taken to ensure correct speaker polarity connection.

7.10 Amplifier and buffer outputs

Although there are only six output pins available, this device incorporates four BTL power amplifiers with a unique internal configuration. The system performs in an optimum manner (maximum BTL output power) when two related channels (IN1A and IN1B or IN2A and IN2B) have the same phase. In general, this will be the case for front and rear signals. Therefore it is recommended to use channels IN1A and IN1B for e.g. front and rear right and channels IN2A and IN2B for e.g. front and rear left.

All amplifier and buffer outputs are protected against short-circuit to ground, and across the speakers. The amplifier outputs are also protected against short-circuit to the supply lines.

7.11 Diagnostic output

The output of the diagnostic pin (DIAG) is open-collector and therefore must have an external pull-up resistor (e.g. to regulator 3). This pin is active HIGH.

The diagnostic output will be activated during the following conditions:

- Clip detection: when the amplifier is AC operating (low or high power), the diagnostic output will indicate when clipping occurs at one or more outputs; this information can be used to drive a sound processor to attenuate the input signal and so limit the level of distortion
- Short-circuit diagnosis: the diagnostic output will indicate when one or more amplifier outputs have a short-circuit to ground, supply lines or across the speaker
- Thermal foldback pre-warning: before the thermal foldback starts to affect the amplifier output signal, the diagnostic pin will give a pre-warning.

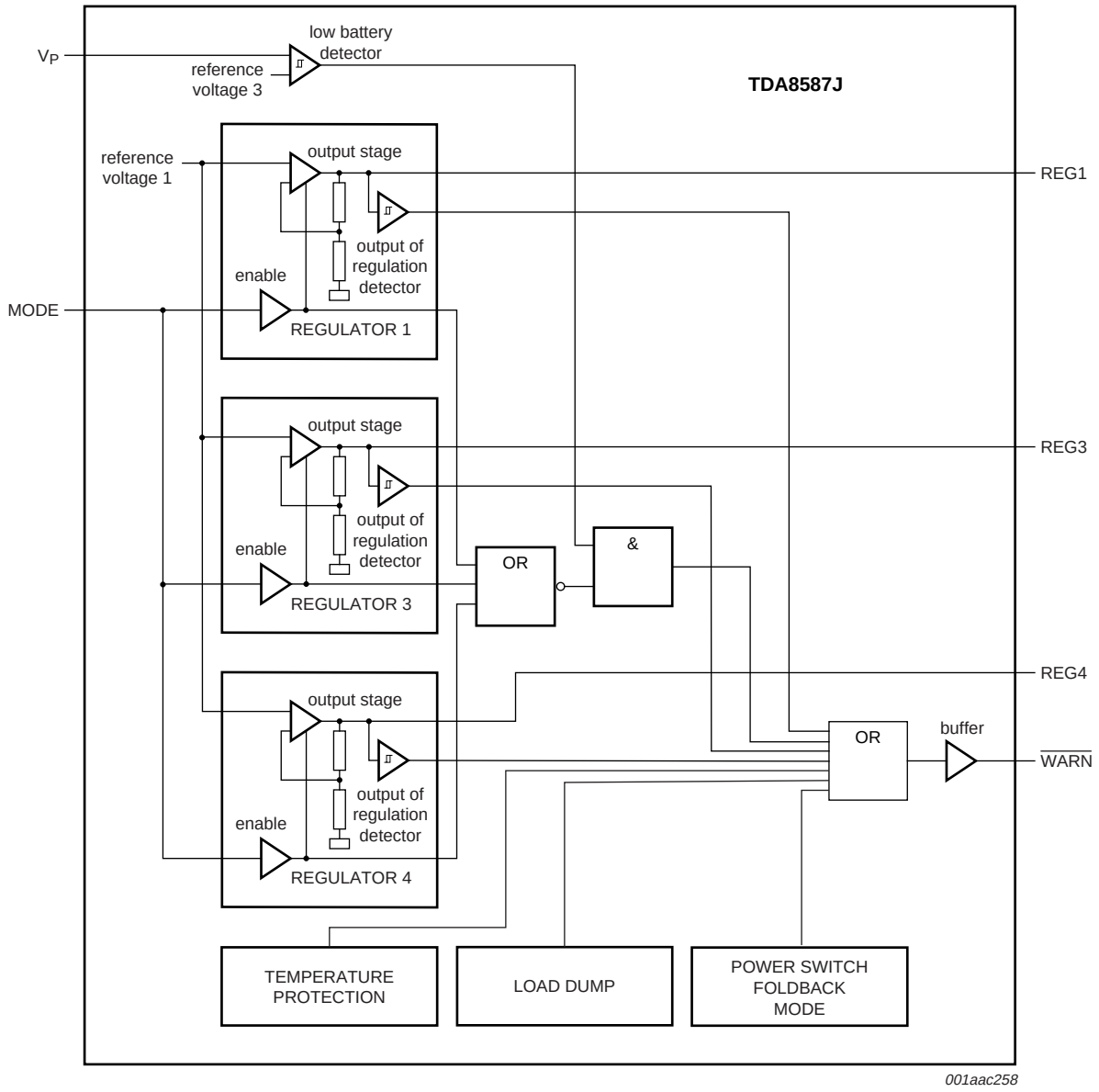


Fig 4. Block diagram of the warning circuit

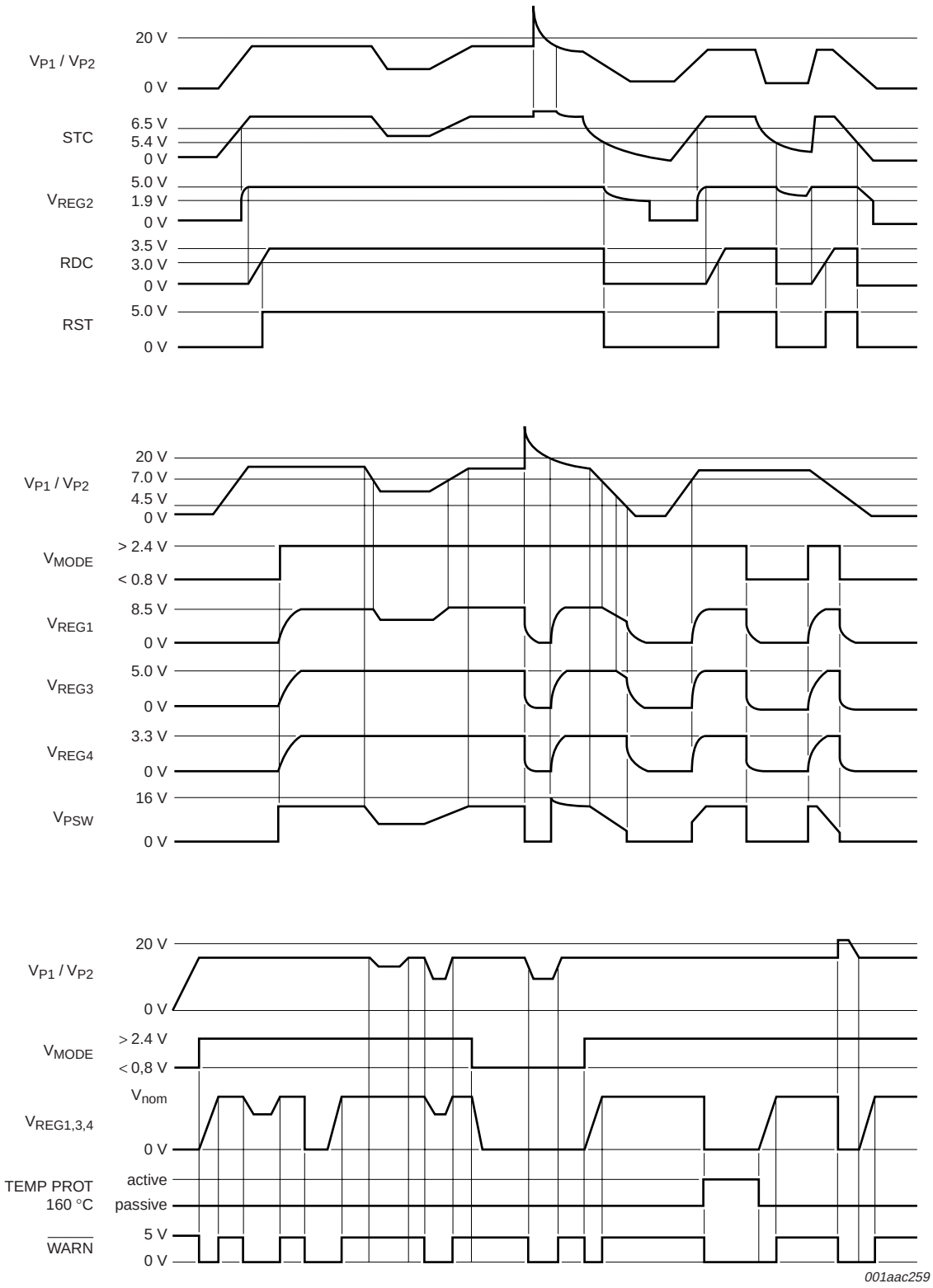


Fig 5. Timing diagrams

8. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage					
	operating			-	18	V
	jump start	t ≤ 10 minutes		-	30	V
	load dump protection	t ≤ 50 ms; $t_r \geq 2.5$ ms		-	50	V
V_{DIAG}	output voltage on pin DIAG			-	18	V
V_{WARN}	output voltage on pin $\overline{WARN}$			-	18	V
V_{MODE}	input voltage on pin MODE			-	18	V
I_{OSM}	non-repetitive peak output current of amplifier			-	6	A
I_{ORM}	repetitive peak output current of amplifier			-	4	A
V_{rp}	reverse polarity voltage		[1]	-	6	V
P_{tot}	total power dissipation			-	75	W
T_{stg}	storage temperature	non-operating		–55	+150	°C
T_{amb}	ambient temperature	operating		–40	+85	°C
T_j	junction temperature	operating		-	+150	°C

[1] This implies that a large current will flow when the battery is reverse connected, therefore external measures are needed to protect against this fault condition (reverse power diode and fuse).

9. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

10. Characteristics

Table 6: Characteristics general

V_P = V_{MODE} = 14.4 V; T_{amb} = 25 °C; measured in test circuits of Figure 8 and Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_P	operating supply voltage	all modules	[1]	8	14.4	18	V
		standby regulator (REG2)		4	14.4	50	V
$V_{P(oth)}$	supply overvoltage threshold		[2]	18	20	22	V
$I_{q(stby)}$	standby quiescent current	V_{MODE} < 0.8 V; no loads		-	105	135	µA
$I_{q(oper)}$	operating quiescent current	V_{MODE} > 2.4 V; no loads		-	200	350	mA
Mode select input; pin MODE							
$V_{i(MODE)}$	mode select input voltage						
		standby mode	[3]	0	-	0.8	V
		operating mode	[4]	2.4	-	V_P – 2	V
		mute mode	[5]	2.4	-	4.5	V
		on mode		7.4	-	V_P – 2	V
		high output power mode	[6]	7.4	-	V_{REG1}	V
		low output power mode	[7]	V_{REG1} + 0.5	-	V_P – 2	V
I_{sink}	input sink current	V_{MODE} = 10 V		0	10	20	µA
Temperature foldback or shutdown							
I_{fb}	foldback current		[8]	150	200	-	µA
$T_{j(pw)}$	foldback pre-warning junction temperature		[9] [10]	145	155	165	°C
$T_{j(fb)}$	foldback junction temperature		[9] [11]	150	160	170	°C
$T_{j(sd)}$	shutdown junction temperature		[9] [12]	160	170	180	°C

[1] Switched regulator (REG1) will be in regulation at $V_P \geq 9.5$ V.

[2] With increasing supply voltage at the overvoltage threshold, pin $\overline{WARN}$ goes HIGH-to-LOW.

[3] All modules are switched off, except the standby regulator (REG2), reset (delay) and warning function.

[4] All modules are enabled.

[5] Amplifiers are DC adjusted, but the input signal is suppressed.

[6] Amplifiers are capable of delivering maximum output power.

[7] Amplifiers are capable of delivering (internally) limited output power.

[8] The voltage drop across the external mode pin resistor (R1) at full foldback current should be sufficient to put the amplifiers in mute [$V_{MODE} \leq V_{MODE(mute)(max)}$].
Example 1: mode pin supplied from V_P = 14.4 V (low output power):
$R1 \geq [V_P - V_{MODE(mute)(max)}]/I_{MODE(fb)(min)}$ = (14.4 V – 4.5 V)/150 µA = 66.0 kΩ.
Example 2: mode pin supplied from V_{REG1} (high output power):
$R1 \geq [V_{REG1(max)} - V_{MODE(mute)(max)}]/I_{MODE(fb)(min)}$ = (8.9 V – 4.5 V)/150 µA = 29.3 kΩ.

[9] This parameter is only measured in Production Validation (PV) tests.

[10] Diagnostic output activated, pin DIAG goes LOW-to-HIGH

[11] Amplifier output signals will be gradually reduced to full mute at increasing junction temperature.

[12] All switchable regulators and power switch will be switched off, pin $\overline{WARN}$ goes HIGH-to-LOW.

Table 7: DC and AC characteristics regulator part

$V_P = V_{MODE}$ = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply enable function							
$V_{th(on)}$	supply enable on threshold voltage	V_P increasing	[2]	6.5	7.0	7.5	V
$V_{th(off)}$	supply enable off threshold voltage	V_P decreasing	[2]	4.0	4.5	5.0	V
V_{hyst}	supply threshold hysteresis voltage		[1]	2.1	2.5	3.3	V
Power supply warning function							
$V_{WARN(th)(on)}$	warning on threshold voltage	V_{MODE} = 0 V	[3]	9.0	9.4	9.8	V
$V_{WARN(th)(off)}$	warning off threshold voltage	V_{MODE} = 0 V	[4]	9.1	9.7	10.3	V
$V_{WARN(hyst)}$	warning threshold hysteresis voltage	V_{MODE} = 0 V	[1]	0.1	0.3	-	V
Warning output (open-collector)							
V_{OL}	LOW-level output voltage	I_O = 1 mA; warning active		-	0.6	0.8	V
$I_{OH(leak)}$	HIGH-level output leakage current	V_{OH} = 5 V; warning not active		-	0.1	5	µA
t_r	rise time	C_L = 50 pF	[1]	-	7	50	µs
t_f	fall time	C_L = 50 pF	[1]	-	1	50	µs
Reset output (push-pull stage)							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA; V_{RDC} = 0 V		-	0.6	0.8	V
$I_{OH(source)}$	HIGH-level output source current	V_{OH} = 4.5 V; V_{RDC} = 5 V		200	400	900	µA
t_r	rise time	C_L = 50 pF	[1]	-	7	50	µs
t_f	fall time	C_L = 50 pF	[1]	-	1	50	µs
Reset delay function							
I_{ch}	charge current	V_{RDC} = 0 V		2	4	8	µA
I_{dis}	discharge current	V_{RDC} = 3 V; V_P = 4.3 V		1.0	1.6	-	mA
$V_{RST(th)(on)}$	reset on threshold voltage		[5]	2.5	3.0	3.5	V
$V_{RST(th)(off)}$	reset off threshold voltage		[6]	1.0	1.2	1.4	V
Power switch							
$V_{o(PSW)(drop)}$	power switch drop-out voltage	I_o = 1.0 A; V_P = 13.5 V	[7]	-	0.45	0.7	V
		I_o = 1.4 A; V_P = 13.5 V	[7]	-	0.7	1.0	V
I_O	continuous output current	V_P = 16 V; V_o = 13.5 V		1.4	2.0	-	A
$I_{o(pulse)}$	pulsed output current	V_P = 16 V; V_o = 14.0 V	[8]	2.5	3.0	-	A
$I_{o(sc)}$	short-circuit output current	V_o = 1.0 V	[9]	0.5	1.0	-	A
$V_{o(clamp)}$	clamping output voltage	$V_P \geq 17$ V; 1 mA $\leq I_o \leq$ 1.4 A		13.5	15.0	16.0	V
$V_{o(fb)}$	flyback output voltage	I_o = –100 mA		-	V_P + 1	V_P + 2	V
$V_{o(ct)}$	crosstalk noise output voltage		[1] [10] [11]	-	25	150	µV
$V_{o(WARN)(th)}$	warning threshold output voltage		[12]	0.6	1.2	1.8	V

Table 7: DC and AC characteristics regulator part *...continued*

$V_P = V_{MODE}$ = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Storage capacitor switch							
I_O	continuous output current	V_o = 5 V	[13]	200	250	-	mA
$I_{o(rev)}$	reverse output current	V_P = 0 V; V_o = 12.4 V		-	150	900	µA
$V_{o(clamp)}$	output clamping voltage	$V_P \geq$ 16.7 V; 1 mA ≤ I_o ≤ 200 mA		13.5	15.0	16.0	V
$V_{o(th)(on)}$	regulator enable threshold output voltage		[1] [14]	5.5	6.5	7.5	V
Regulator 1: switched 8.5 V / 200 mA (I_o = 5 mA); unless otherwise specified							
$V_{o(REG1)}$	output voltage of regulator 1	1 mA ≤ I_o ≤ 200 mA		8.1	8.5	8.9	V
		9.5 V ≤ V_P ≤ 18 V		8.1	8.5	8.9	V
ΔV_{line}	line regulation voltage	9.5 V ≤ V_P ≤ 18 V		-	10	50	mV
ΔV_{load}	load regulation voltage	1 mA ≤ I_o ≤ 200 mA		-	10	50	mV
V_{drop}	dropout voltage	I_o = 200 mA; V_P = 8.5 V	[7]	-	0.4	0.7	V
I_m	current limit	V_o > 7 V	[9]	225	500	-	mA
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω	[9]	50	200	-	mA
SVRR	supply voltage ripple rejection	f_{ripple} = 3 kHz	[15]	60	70	-	dB
		f_{ripple} = 120 Hz	[1] [15]	55	65	-	dB
		f_{ripple} = 1 kHz	[1] [15]	55	65	-	dB
		f_{ripple} = 10 kHz	[1] [15]	45	60	-	dB
		f_{ripple} = 30 kHz	[1] [15]	40	50	-	dB
$V_{o(n)}$	peak noise output voltage	B = 40 Hz to 1 kHz	[1] [16]	-	-	1200	nV/√Hz
		B = 1 kHz to 4 kHz	[1] [16]	-	-	1000	nV/√Hz
		B = 4 kHz to 20 kHz	[1] [16]	-	-	550	nV/√Hz
		B = 20 kHz to 4 MHz	[1] [16]	-	-	200	nV/√Hz
		B = 4 MHz to 12 MHz	[1] [16]	-	-	110	nV/√Hz
		B = 12 MHz to 125 MHz	[1] [16]	-	-	220	nV/√Hz
V_{ct}	crosstalk noise voltage		[1] [17] [11]	-	25	150	µV
$V_{WARN(th)(on)}$	warning on threshold voltage		[18]	7.7	V_o – 0.35	-	V
$V_{WARN(th)(off)}$	warning off threshold voltage		[19]	-	V_o – 0.15	V_o – 0.08	V
$V_{WARN(hyst)}$	warning threshold hysteresis voltage			0.1	0.2	0.3	V
Regulator 2: standby 5 V / 200 mA (I_o = 5 mA); unless otherwise specified							
$V_{o(REG2)}$	output voltage of regulator 2	1 mA ≤ I_o ≤ 200 mA		4.75	5.0	5.25	V
		7 V ≤ V_P ≤ 45 V		4.75	5.0	5.25	V
ΔV_{line}	line regulation voltage	7 V ≤ V_P ≤ 18 V		-	10	50	mV
ΔV_{load}	load regulation voltage	1 mA ≤ I_o ≤ 100 mA		-	10	50	mV
		1 mA ≤ I_o ≤ 200 mA		-	30	100	mV

Table 7: DC and AC characteristics regulator part *...continued*

$V_P = V_{MODE}$ = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{drop}	dropout voltage	I_o = 100 mA; V_P = 4.75 V	[7]	-	0.3	0.6	V
		I_o = 200 mA; V_P = 5.25 V	[7]	-	0.8	1.2	V
		I_o = 100 mA; V_{STC} = 4.75 V	[20]	-	0.3	0.6	V
		I_o = 200 mA; V_{STC} = 5.25 V	[20]	-	0.8	1.2	V
I_m	current limit	V_o > 4.5 V	[9]	225	500	-	mA
I_{sc}	short-circuit current	$R_L \leq 0.5\ \Omega$	[9]	85	200	-	mA
SVRR	supply voltage ripple rejection	f_{ripple} = 3 kHz	[15]	50	55	-	dB
		f_{ripple} = 120 Hz	[1] [15]	60	65	-	dB
		f_{ripple} = 1 kHz	[1] [15]	55	60	-	dB
		f_{ripple} = 10 kHz	[1] [15]	45	50	-	dB
		f_{ripple} = 30 kHz	[1] [15]	40	45	-	dB
$V_{o(n)}$	peak noise output voltage	B = 40 Hz to 1 kHz	[1] [16]	-	-	1200	nV/√Hz
		B = 1 kHz to 4 kHz	[1] [16]	-	-	1000	nV/√Hz
		B = 4 kHz to 20 kHz	[1] [16]	-	-	550	nV/√Hz
		B = 20 kHz to 4 MHz	[1] [16]	-	-	200	nV/√Hz
		B = 4 MHz to 12 MHz	[1] [16]	-	-	110	nV/√Hz
		B = 12 MHz to 125 MHz	[1] [16]	-	-	220	nV/√Hz
V_{ct}	crosstalk noise voltage		[1] [21] [11]	-	25	150	µV
$V_{RST(th)(on)}$	reset on threshold voltage	I_o = 50 mA	[22]	4.43	V_o – 0.15	V_o – 0.1	V
$V_{RST(th)(on)}$	reset off threshold voltage	I_o = 50 mA	[23]	4.4	V_o – 0.25	V_o – 0.15	V
$V_{REG(th)(dis)}$	regulator disable threshold voltage		[24]	1.7	1.9	2.3	V
Regulator 3: switched 5 V / 900 mA (I_o = 5 mA); unless otherwise specified							
$V_{o(REG3)}$	output voltage of regulator 3	1 mA ≤ I_o ≤ 900 mA		4.75	5.0	5.25	V
		7 V ≤ V_P ≤ 18 V		4.75	5.0	5.25	V
ΔV_{line}	line regulation voltage	7 V ≤ V_P ≤ 18 V		-	25	50	mV
ΔV_{load}	load regulation voltage	1 mA ≤ I_o ≤ 900 mA		-	35	100	mV
V_{drop}	dropout voltage	I_o = 900 mA; V_P = 5.25 V	[7]	-	0.5	0.9	V
I_m	current limit	V_o > 4.5 V	[9]	1.0	2.0	-	A
I_{sc}	short-circuit current	$R_L \leq 0.5\ \Omega$	[9]	380	500	-	mA
SVRR	supply voltage ripple rejection	f_{ripple} = 3 kHz	[15]	60	70	-	dB
		f_{ripple} = 120 Hz	[1] [15]	55	65	-	dB
		f_{ripple} = 1 kHz	[1] [15]	55	65	-	dB
		f_{ripple} = 10 kHz	[1] [15]	45	60	-	dB
		f_{ripple} = 30 kHz	[1] [15]	40	50	-	dB

Table 7: DC and AC characteristics regulator part *...continued*

$V_P = V_{MODE}$ = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{o(n)}$	peak noise output voltage	B = 40 Hz to 1 kHz	[1] [16]	-	-	1200	nV/√Hz
		B = 1 kHz to 4 kHz	[1] [16]	-	-	1000	nV/√Hz
		B = 4 kHz to 20 kHz	[1] [16]	-	-	550	nV/√Hz
		B = 20 kHz to 4 MHz	[1] [16]	-	-	200	nV/√Hz
		B = 4 MHz to 12 MHz	[1] [16]	-	-	110	nV/√Hz
		B = 12 MHz to 125 MHz	[1] [16]	-	-	220	nV/√Hz
V_{ct}	crosstalk noise voltage		[1] [25] [11]		25	150	µV
$V_{WARN(th)(on)}$	warning on threshold voltage		[18]	4.3	V_o – 0.35	-	V
$V_{WARN(th)(off)}$	warning off threshold voltage		[19]	-	V_o – 0.15	V_o – 0.08	V
$V_{WARN(hyst)}$	warning threshold hysteresis voltage			0.1	0.2	0.3	V
Regulator 4: switched 3.3 V / 200 mA (I_o = 5 mA); unless otherwise specified							
$V_{o(REG4)}$	output voltage of regulator 4	1 mA ≤ I_o ≤ 200 mA		3.15	3.3	3.45	V
		7 V ≤ V_P ≤ 18 V		3.15	3.3	3.45	V
ΔV_{line}	line regulation voltage	7 V ≤ V_P ≤ 18 V		-	10	50	mV
ΔV_{load}	load regulation voltage	1 mA ≤ I_o ≤ 200 mA		-	10	50	mV
V_{drop}	dropout voltage	I_o = 200 mA; V_P = 5 V	[7]	-	1.7	2.0	V
I_m	current limit	V_o > 3 V	[9]	225	500	-	mA
I_{sc}	short-circuit current	R_L ≤ 0.5 Ω	[9]	130	200	-	mA
SVRR	supply voltage ripple rejection	f_{ripple} = 3 kHz	[15]	60	75	-	dB
		f_{ripple} = 120 Hz	[1] [15]	55	70	-	dB
		f_{ripple} = 1 kHz	[1] [15]	55	70	-	dB
		f_{ripple} = 10 kHz	[1] [15]	45	60	-	dB
		f_{ripple} = 30 kHz	[1] [15]	40	50	-	dB
$V_{o(n)}$	peak noise output voltage	B = 40 Hz to 1 kHz	[1] [16]	-	-	1200	nV/√Hz
		B = 1 kHz to 4 kHz	[1] [16]	-	-	1000	nV/√Hz
		B = 4 kHz to 20 kHz	[1] [16]	-	-	550	nV/√Hz
		B = 20 kHz to 4 MHz	[1] [16]	-	-	200	nV/√Hz
		B = 4 MHz to 12 MHz	[1] [16]	-	-	110	nV/√Hz
		B = 12 MHz to 125 MHz	[1] [16]	-	-	220	nV/√Hz
V_{ct}	crosstalk noise voltage		[1] [26] [11]		25	150	µV
$V_{WARN(th)(on)}$	warning on threshold voltage		[18]	2.7	V_o – 0.3	-	V
$V_{WARN(th)(off)}$	warning off threshold voltage		[19]	-	V_o – 0.15	V_o – 0.08	V
$V_{WARN(hyst)}$	warning threshold hysteresis voltage			0.1	0.15	0.2	V

[1] This parameter is only measured in product validation (PV) tests.

[2] Supply voltage enable function controls regulators 1, 3 and 4 and the power switch.

[3] Supply voltage is decreasing, pin $\overline{WARN}$ goes HIGH-to-LOW, indicates that V_P is too low for proper regulation.

[4] Supply voltage is increasing, pin $\overline{WARN}$ goes LOW-to-HIGH, indicates that V_P is sufficient for proper regulation.

[5] Reset delay capacitor voltage is increasing (see Regulator 2), at the threshold pin RST goes LOW-to-HIGH.

[6] Reset delay capacitor voltage is decreasing (see Regulator 2), at the threshold pin RST goes HIGH-to-LOW.

[7] Drop-out voltage is measured with respect to V_P.

[8] Pulse duration depends on value of the capacitor on pin RDC.

[9] For a typical shape of the foldback current protection; see Figure 6 and Figure 7.

[10] Power switch is loaded with a 1 kHz sine wave load current varying between 1 mA ≤ I_o ≤ 1.4 A.

[11] Crosstalk noise is selectively measured at the outputs of the other regulators and across the amplifier loads.

[12] With decreasing power switch output, pin $\overline{WARN}$ goes HIGH-to-LOW.

[13] Output current is not intended to be used for external circuitry (except for charging the storage capacitor).

[14] Standby regulator is enabled when the increasing storage capacitor voltage reaches this threshold at first power-up.

[15] Supply voltage ripple rejection is measured at output of the regulator; V_{ripple} = 0.7 V.

[16] Noise output voltage depends on the value of the regulator output capacitor.

[17] Regulator 1 is loaded with a 1 kHz sine wave load current varying between: 1 mA ≤ I_o ≤ 200 mA.

[18] Regulator output is decreasing and goes out of regulation, pin $\overline{WARN}$ goes HIGH-to-LOW.

[19] Regulator output is increasing and starts to regulate, pin $\overline{WARN}$ goes LOW-to-HIGH.

[20] Dropout voltage is measured with respect to V_{STC}; V_P pins connected to ground.

[21] Regulator 2 is loaded with a 1 kHz sine wave load current varying between: 1 mA ≤ I_o ≤ 200 mA.

[22] Regulator output voltage is increasing, at the threshold the reset delay capacitor will be charged.

[23] Regulator output voltage is decreasing, at the threshold the reset delay capacitor will be discharged.

[24] Standby regulator is disabled when the decreasing output voltage reaches this threshold.

[25] Regulator 3 is loaded with a 1 kHz sine wave load current varying between 1 mA ≤ I_o ≤ 900 mA.

[26] Regulator 4 is loaded with a 1 kHz sine wave load current varying between 1 mA ≤ I_o ≤ 200 mA.

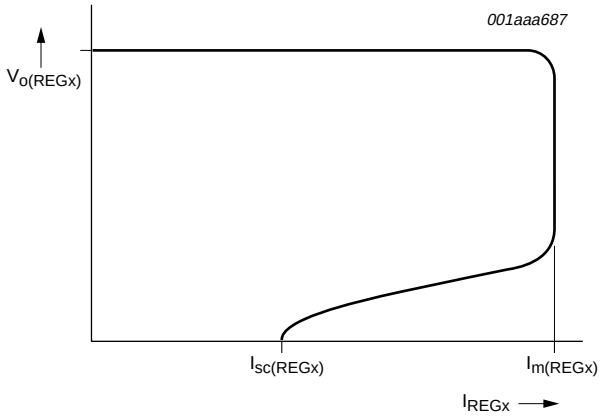


Fig 6. Typical foldback current protection curve for all regulators

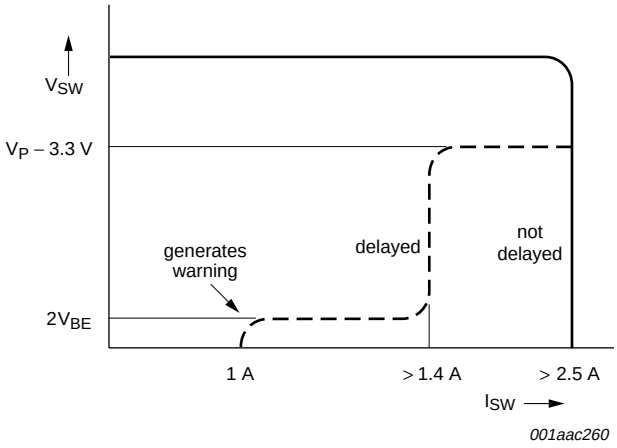


Fig 7. Current protection of the power switch

Table 8: DC characteristics amplifier part

V_P = V_{MODE} = 14.4 V; T_{amb} = 25 °C; measured in test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply mute function						
$V_{P(mute)(th)}$	supply mute threshold voltage	V_P decreasing	6.0	7.0	8.0	V
$V_{P(muteoff)(th)}$	supply unmute threshold voltage	V_P increasing	7.0	8.0	9.0	V
$V_{P(hys)}$	supply threshold hysteresis voltage	[1]	0.5	1.0	1.5	V
DC biasing voltages						
V_{ref}	DC reference voltage		3.5	4.0	4.5	V
V_I	DC input voltage		3.5	4.0	4.5	V
V_O	DC output voltage		6.5	7.0	7.5	V
V_{OO}	DC output offset voltage	mute	–20	0	+20	mV
		on	–100	0	+100	mV
Diagnostic output (open-collector)						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA; diagnostic not active	-	0.6	0.8	V
$I_{OH(leak)}$	HIGH-level output leakage current	V_{OH} = 5V; diagnostic active	-	0.1	5	µA

[1] This parameter is only measured in product validation tests.

Table 9: AC characteristics amplifier part

V_P = 14.4 V; V_{MODE} = V_{REG1}; P_o = 1 W; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Figure 9; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(h)}$	output power high	THD = 0.5 %	[1]	11	12.5	-	W
		THD = 10 %	[1]	15	17.5	-	W
		square wave; V_i = 2 V (p-p)	[1]	22	25	-	W
$P_{o(l)}$	output power low	THD = 0.5 %; V_{MODE} = 10 V	[1]	4	4.5	-	W
		THD = 10 %; V_{MODE} = 10 V	[1]	5	5.5	-	W
THD	total harmonic distortion		[2]	-	0.05	0.3	%
		f = 50 Hz to 10 kHz	[3] [2]	-	0.3	0.5	%
CLIP	clip detect THD level	V_{DIAG} > 4 V	[3]	7	10	13	%
G_v	voltage gain			25	26	27	dB
ΔG_v	channel unbalance			–0.7	0	+0.7	dB
f_h	high frequency roll-off (–1 dB)		[3]	20	-	-	kHz
Z_i	input impedance			40	60	90	kΩ
SVRR	supply voltage ripple rejection	on; R_s = 0 Ω	[4]	40	45	-	dB
		on; f = 100 Hz to 10 kHz	[3] [4]	30	35	-	dB
		mute	[4]	55	60	-	dB
		mute; f = 100 Hz to 10 kHz	[3] [4]	50	55	-	dB
		standby; f = 100 Hz to 10 kHz	[3] [4]	80	90	-	dB
ISRR	input signal rejection ratio	mute	[5]	100	120	-	dB
		mute; f = 100 Hz to 10 kHz	[3] [5]	90	100	-	dB
α_{ct}	crosstalk	R_s = 10 kΩ	[6]	60	70	-	dB
		f = 100 Hz to 10 kHz	[3] [6]	50	60	-	dB
$V_{o(n)}$	noise output voltage	on; R_s = 0 Ω	[7]	-	120	150	μV
		on; R_s = 10 kΩ	[3] [7]	-	200	250	μV
		mute	[3] [7]	-	5	20	μV

[1] Output power is measured across R_L directly on the pins of the IC.

[2] Total harmonic distortion is measured across R_L in a bandwidth: B = 20 Hz to 20 kHz.

[3] This parameter is only measured in product validation tests.

[4] Supply voltage ripple rejection is measured across R_L; V_{ripple} = 0.7 V.

[5] Input signal rejection ratio is measured across R_L; V_i = 1 V, ISSR [dB] = voltage gain (G_V) – mute attenuation (A_M).

[6] Crosstalk is measured at the regulator outputs and across R_L of the unrelated amplifier channels (OUT1A or 1B or OUT2A or 2B).

[7] Noise output voltage is measured across R_L in a bandwidth: B = 20 Hz to 20 kHz.

11. Application information

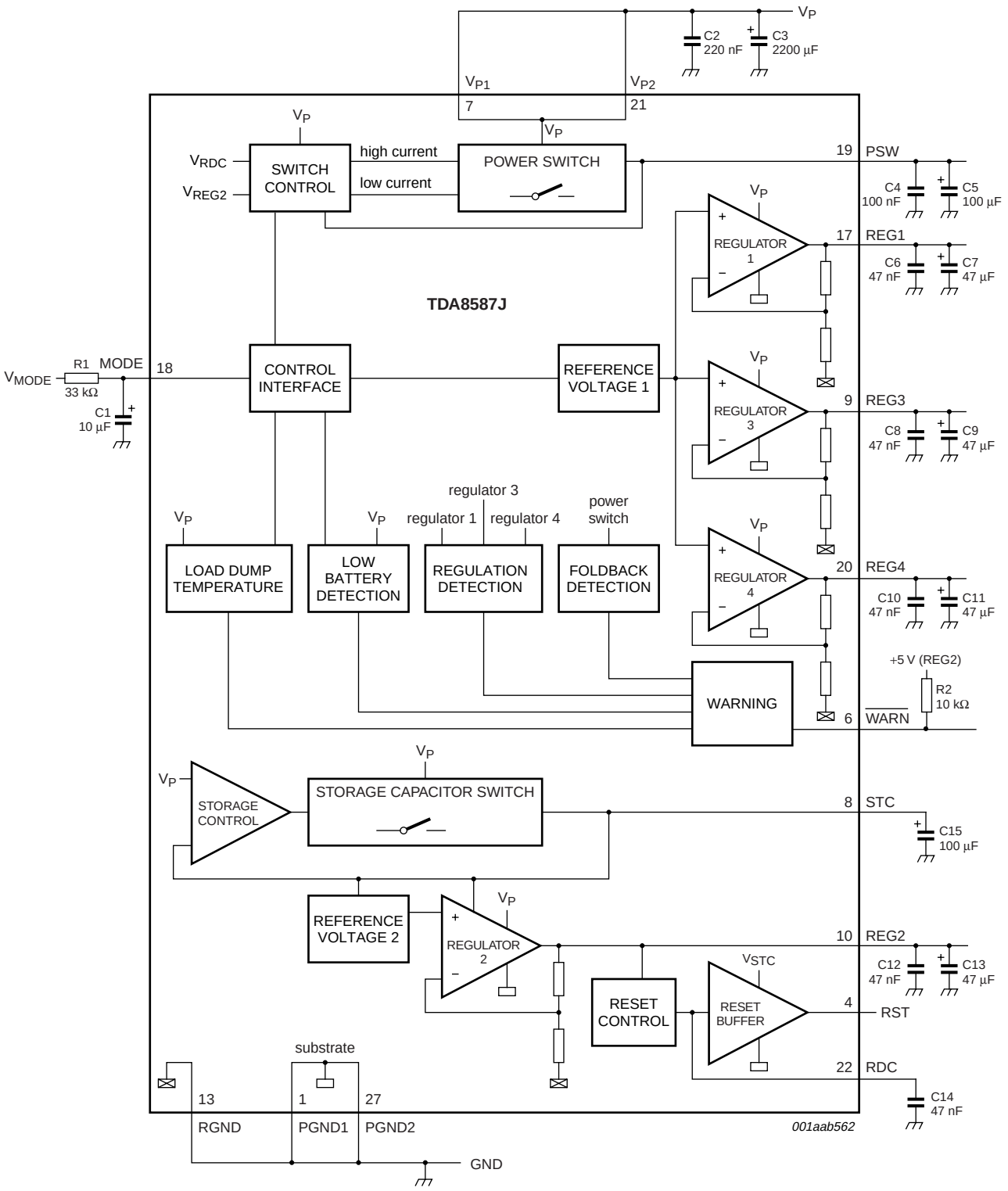


Fig 8. Application diagram regulator part

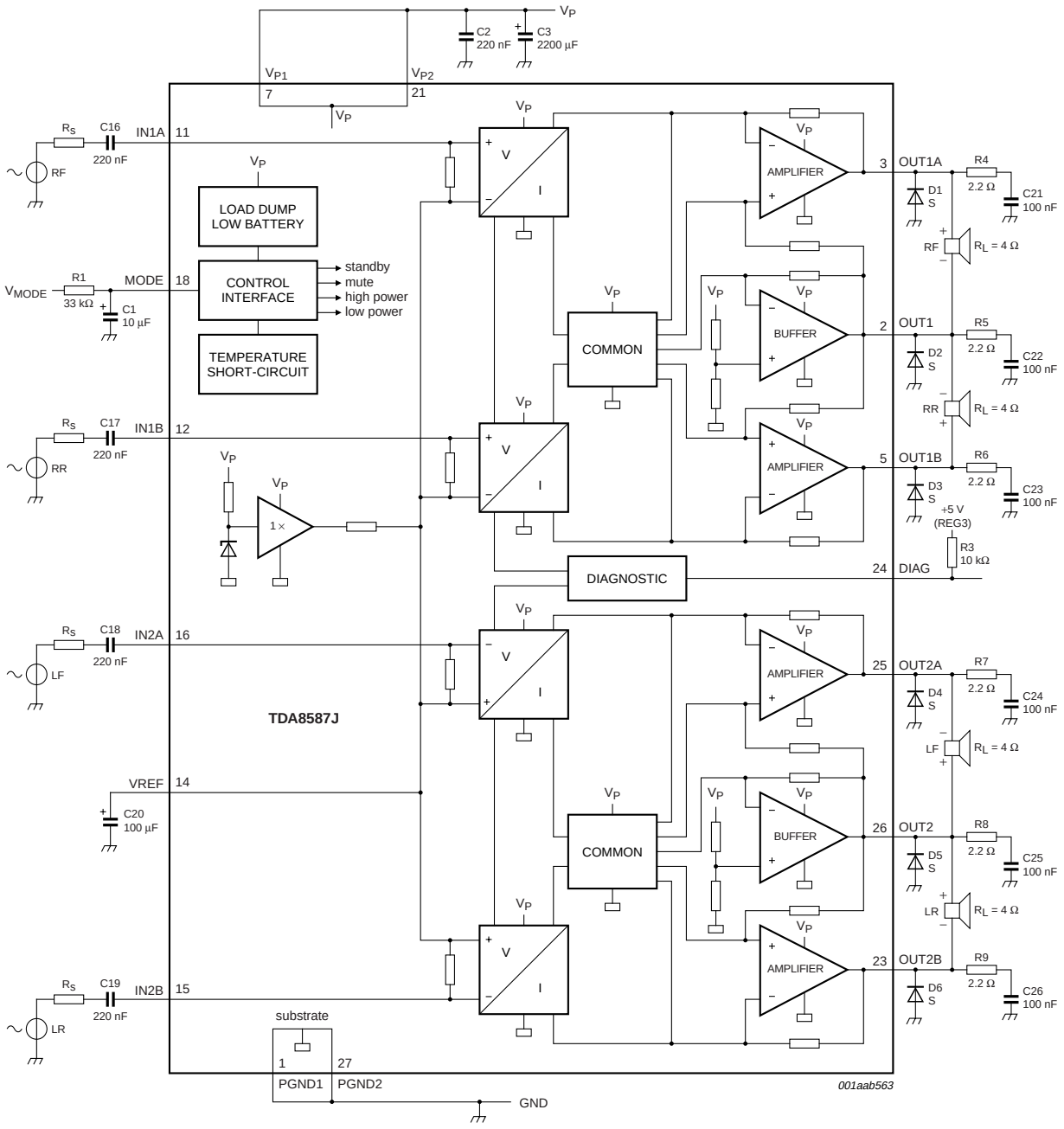


Fig 9. Application diagram amplifier part

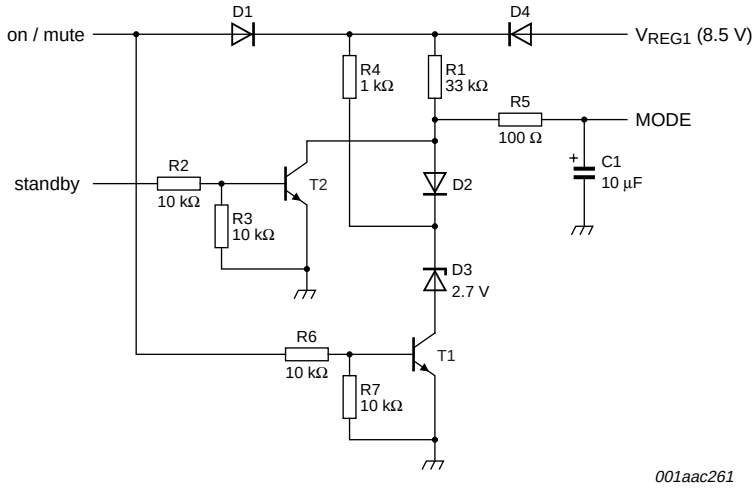
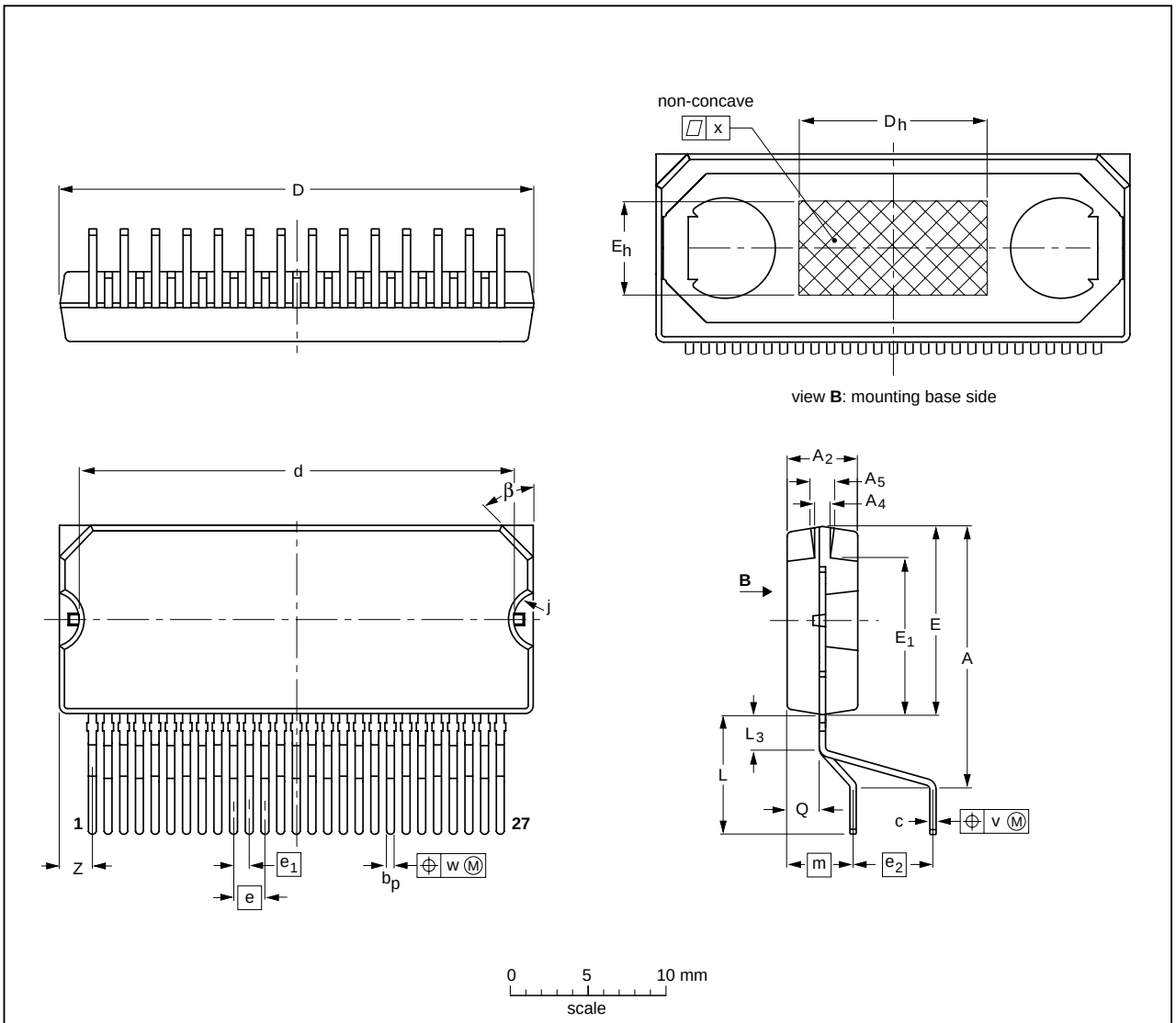


Fig 10. Typical external mode pin control circuit using two microcontroller pins

12. Package outline

DBS27P: plastic DIL-bent-SIL power package; 27 leads (lead length 7.7 mm) **SOT521-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	j	L	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	17.0 15.5	4.6 4.3	1.15 0.85	1.65 1.35	0.60 0.45	0.5 0.3	30.4 29.9	28.0 27.5	12	12.2 11.8	2	1	4	6	10.15 9.85	1.85 1.65	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	2.4 1.8

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT521-1						~~99-01-05~~ 02-04-24

Fig 11. Package outline SOT521-1 (DBS27P).

13. Soldering

13.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

13.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

13.4 Package related soldering information

Table 10: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable [1]
PMFP [2]	–	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TDA8587J_1	20041223	Preliminary data sheet	-	9397 750 13504	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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