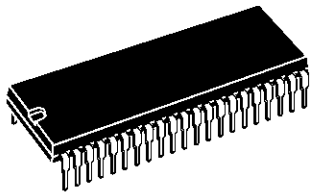
SGS-THOMSON MICROELECTRONICS

TDA9205

DC CONTROLLED 130MHz RGB PREAMPLIFIER

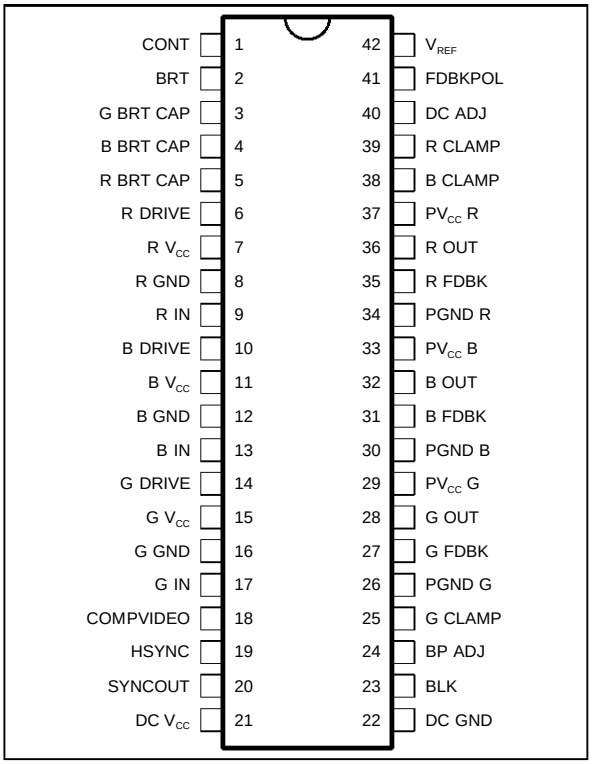
- 130MHz TYPICAL BANDWIDTH AT $1V_{PP}$
- 2.8ns TYP. RISE/FALL TIME ($3V_{PP}$/12pF LOAD)
- DC ADJUSTMENT : CONT, BRT, RGB DRIVE, RGB CUT-OFF
- COMP. VIDEO INPUT AND POSITIVE OR NEGATIVE SYNC INPUT
- INTERNAL BACKPORCH CLAMPING PULSE GENERATOR WITH 3 SELECTABLE WIDTH
- BLANKING STAGE
- INTERNAL PULSE GENERATOR FOR CUT-OFF LOOP GATING (INSIDE BLANKING)
- POSSIBILITY OF AC OR DC COUPLING TO HIGH VOLTAGE AMPLIFIER
- VOLTAGE REFERENCE GENERATOR
- POWERFULL OUTPUT DRIVE CAPABILITY
- BICMOS PROCESS



SHRINK42
(Plastic Package)

ORDER CODE : TDA9205

PIN CONNECTIONS



DESCRIPTION

The TDA9205 is a DC controlled wideband video amplifier intended for use in high resolution color monitor. DC (0 to 5V) contrast and brightness commands apply to the 3 channels. White balance adjustment is performed using 3 separated drive inputs. 3 feed-back inputs give a flexible DC level shift of the output signals. Cut-off adjustments can be easily performed with these 3 inputs.

Separated ground and supply for each channel and large swing output voltage (0.5 to 8V) make the TDA9205 suitable for AC or DC drive of discrete, hybrid or monolitic high voltage CRT amplifier.

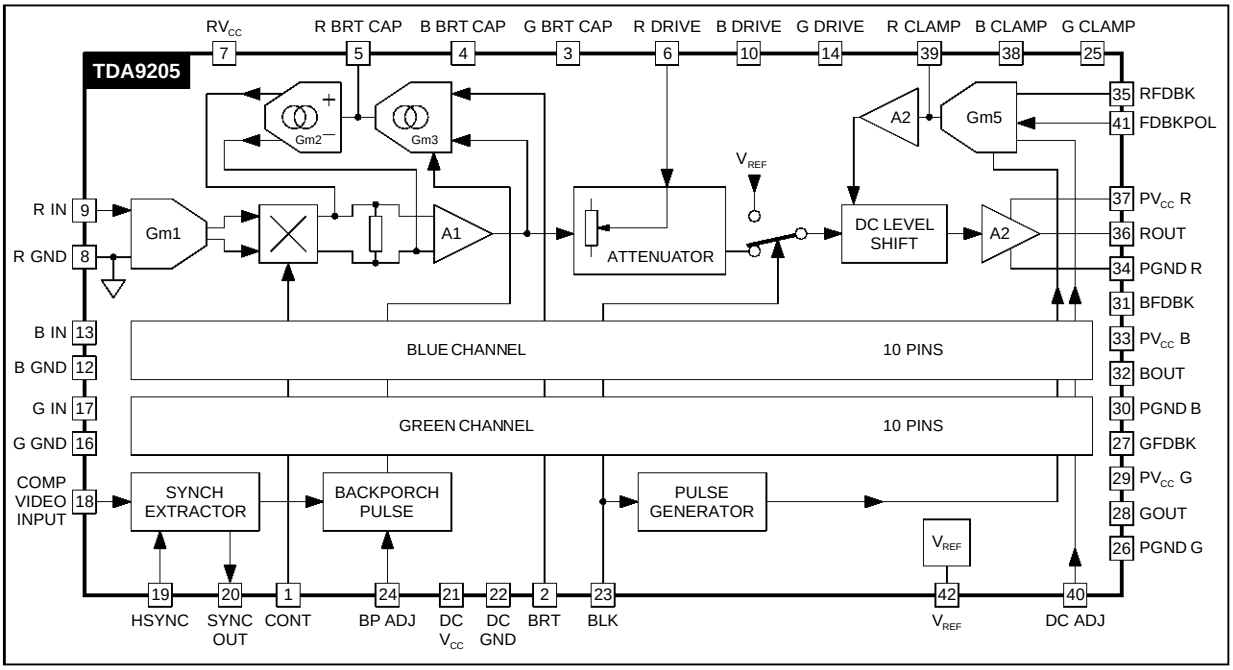
Attractive functions like sync separator, line blanking, backporch generator, voltage reference generator, feed-back polarity selection give to the TDA9205 efficient features for performant and cost effective application.

PIN DESCRIPTION

Pin Number	Symbol	I/O	Function
1	CONT	I	Contrast Adjustment (0 to 5V)
2	BRT	I	Brightness Adjustment (0 to 5V)
3-4-5	G,B,R, BRT CAP	I	G,B,R Capacitor for Brightness Loop
6-10-14	R,B,G DRIVE	I	R,B,G Drive Adjutment
7-11-15	R,B,G V_{CC}	S	Supply Voltage of Input Stage (12V)
8-12-16	R,B,G GND	GND	Signal Ground of Input Stage
9-13-17	R,B,G IN	I	Video Signal Inputs
18	COMPVIDEO	I	Composite Video Input (or Sync on Green)
19	HSYNC	I	Horizontal Synchronization Input
20	SYNCOUT	O	Composite Sync Output
21	DC V_{CC}	S	Supply Voltage (12V)
22	DC GND	GND	Ground
23	BLK	I	Blanking Input
24	BP ADJ	I	Backporch Clamping Pulse Width Adjustment
39-25-38	R,G,B CLAMP	I	R,G,B Capacitor Clamp for Output Stage
34-26-30	R,G,B PGND	GND	Ground of Output Stage
35-27-31	R,G,B FDBK	I	Feed-back Input of Output Stage
36-28-32	R,G,B OUT	O	Video Ouput Signals
37-29-33	R,G,B PV_{CC}	S	Supply Voltage of Output Stage (12V)
40	DC ADJ	I	DC Level ADjustment of Output Signals
41	FDBKPOL	I	Selection of the Signal Polarity of the Feed-back Inputs
42	V_{REF}	O	Voltage Reference Output (5V)

9205-01.TBL

BLOCK DIAGRAM



9205-02.EPS

QUIK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Signal Bandwidth ($1V_{PP}$/12pF laod)		130		MHz
t_R, t_F	Rise and Fall Time ($3.5V_{PP}$/12pF load)		3.8		ns
	Gain Matching		0.3		dB
	Contrast Tracking		0.2		dB
	Drive Adjustment Range on the 3 Channels Separately		6		dB
	Reference Voltage		5		V
	Nominal Output Voltage (V_{IN} = $0.7V_{PP}$)		2.8		V
	Output Voltage (AC + DC)			8	V

9205-02.TBL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pins 7-11-15-21-29-33-37)	13.5	V
I_S	Peak Video Output Sink/Source Current (Pins 28-32-36)	30	mA
V_{IN}	Voltage at any Input Pins	GND < V_{IN} < V_S	V
V_{ESD}	ESD Susceptability (Human body model ; 100pF discharge through 1.5kΩ)	2	kV
T_{stg}	Storage Temperature	-40, +150	^oC
T_j	Junction Temperature	150	^oC
T_{oper}	Operating Temperature	0, +70	^oC

9205-03.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	60	$^oC/W$

9205-04.TBL

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10.8	12	13.2	V
I_S	Supply Current	Addition of all V_S Pins Current		75		mA
V_{REF}	Reference Voltage	Pin 42		5		V
I_{REF}	Max. Sourced Current on Reference Voltage	Pin 42		4		mA
V_I	Input Voltage Amplitude	Pins 9-13-17		0.7	1	V
V_O	Typ. Output Voltage Range	Pins 28-32-36	0.5	-	8	V
V_{ADJ}	Typ. DC Control Voltage Range	Pins 1-2-6-10-14-40	0	-	5	V

9205-05.TBL

AC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{IN}	Video Input Resistance	Pins 9-13-17		15		kΩ
GM	Maximum Gain (20 log x $V_{OUT\ AC}$ / $V_{IN\ AC}$)	V_{CONT1} = 5V, $V_{DRIVE\ 6\text{-}10\text{-}14}$ = 5V		14		dB
GN	Nominal Gain	V_{CONT1} = 2.5V, $V_{DRIVE\ 6\text{-}10\text{-}14}$ = 5V		12.5		dB
GI	Minimum Gain	V_{CONT1} = 0V, $V_{DRIVE\ 6\text{-}10\text{-}14}$ = 5V			-18	dB
DAR	Typical Drive Attenuation Range	Pins 28-32-36 Amplitude vs Voltage on Pins 6-10-14		6.3		dB
BW	Bandwidth Large Signal Bandwidth Small Signal	At -3dB, Load = 12pF, V_{IN} = $1V_{PP}$ V_{OUT} = $3.5V_{PP}$ V_{OUT} = $1V_{PP}$		 100 130		 MHz MHz
DIS	Video Output Distorsion	f = 1MHz, V_{OUT} = $1V_{PP}$, V_{IN} = $1V_{PP}$		0.3		%
t_R, t_F	Video Output Rise and Fall Time	V_{OUT} = $3.5V_{PP}$, Load = 12pF, Measured at 10/90%		2.8		ns
CT1 CT2	Crosstalk	At 1MHz At 40MHz	50	 32		dB dB

9205-06.TBL

GENERAL DESCRIPTION

1- Input Stage

The R, G and B signals must be fed to the three RGB inputs through coupling capacitors (10µF). The maximum peak-to-peak video amplitude is 1V.

In case of synch on green or composite video input signal, the IC will operates normally.

2 - Contrast Adjustment

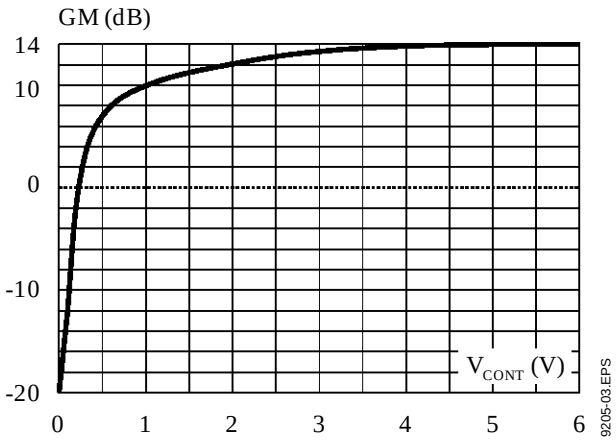
The contrast adjustment is made by controlling simultaneously the gain of three internal variable gain amplifiers, by the DC voltage on Pin 1.

The control voltage range as for all other DC controls on TDA9205 is 0 to 5V.

The contrast adjustment allows to cover a minimum range of 30dB.

The contrast tracking (when contrats is changed) is equal to 0.2dB. Typical curve is given in Figure 1.

Figure 1 : Contrast Adjustment versus Control Voltage



3 - Brightness Adjustment

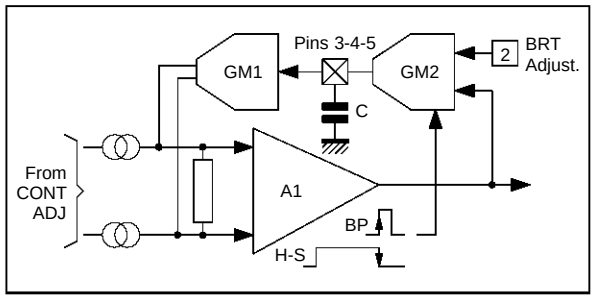
As for the contrast adjustment, the brightness is controlled by a DC voltage applied on Pin2.

The brightness function consits to add the same DC offset to the three RGB signals after contrast amplification.

First the DC level of A1 output is compared to the brightness command on Pin 2 by the comparator GM2. This comparison is made during the internally generated backporch clamping pulse (BP).

As shown on the Figure 2, this pulse occurs when the input video signals are at black level (after the end of sync pulse).

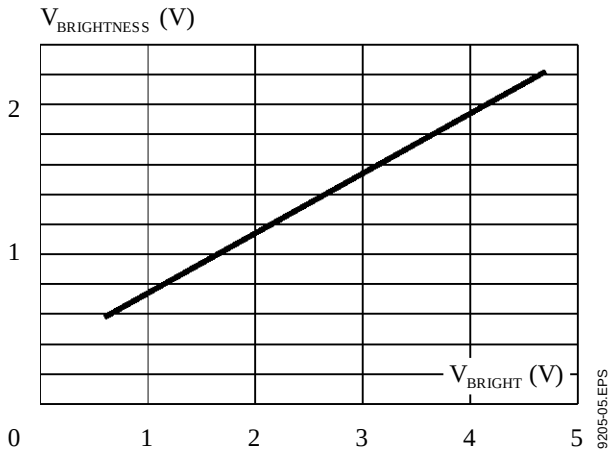
Figure 2



GM2 comparator have a current output which charge or discharge the memory capacitors (C), connected on the input of the transconductors (GM1).

The loop stabilize when the DC value on the output of A1 reaches the desired value setted by the DC voltage on Pin 2. The 3 Video channels works according to this description. Typical curve is given in Figure 3.

Figure 3 : Brightness Adjustment versus Control Voltage



4 - Drive Adjustment

In order to make the white balance, the TDA9205 offers the possibility to adjust separately the overall gain of each complete video channel.

The gain of each channel is controlled by the DC voltage on the Pins 6-10-14.

These pins are connected to the three internal attenuators located after the contrast and brightness processing.

The attenuation range is from 0dB to -6dB.

GENERAL DESCRIPTION (continued)

0dB is achieved for 5V on drive adjustment and -6dB for 0V. Typical curves are given in Figures 4 and 5.

Figure 4 : Drive Adjustment versus Frequency

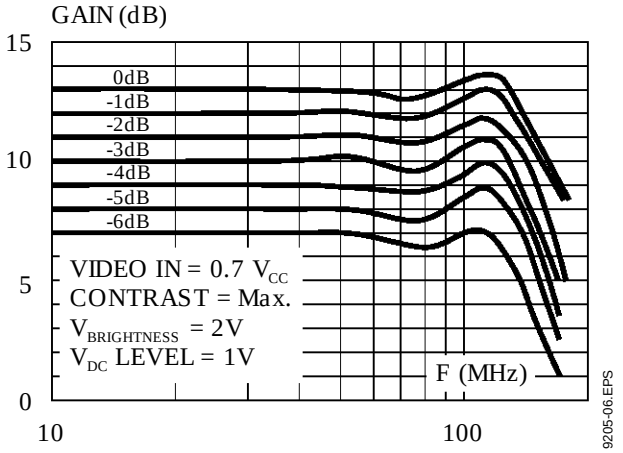
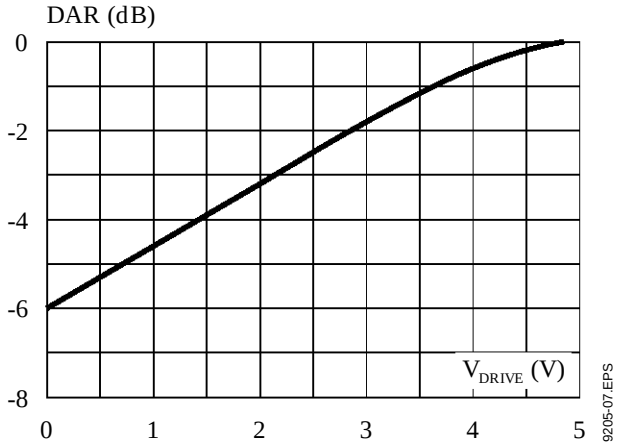


Figure 5 : Drive Adjustment versus Control Voltage



5 - Blanking

The blanking stage switches the outputs to the infra black level when a positive pulse is applied on the TTL BLK input (Pin 23).

The infra black level is defined as black level minus 400mV on the video outputs.

Black level is reached with minimal brightness and black level on video signal inputs.

6 - Output Stage

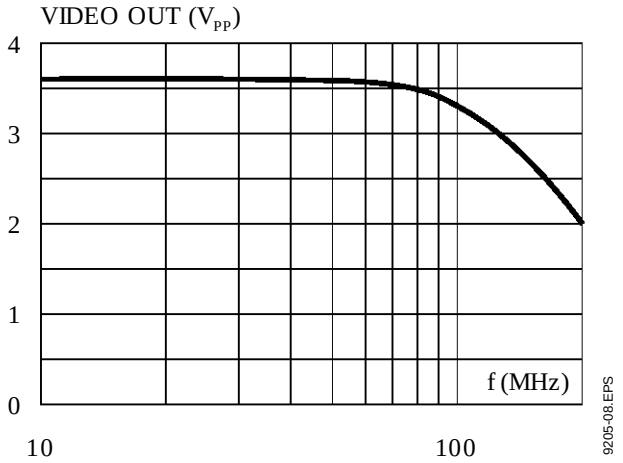
The output stage allows maximum voltage range (between 0.5 and 8V).

To allow the TDA9205 to drive either discrete (with cascade stage) or hybrid or monolitic high voltage amplifier, the output has been designed to be able to drive either capacitive or resistive load.

The three outputs are able to sink or source 30mA maximum current.

As can be seen in the electrical specifications, 3.8ns rise and fall time are possible to achieved with 3.5V_{PP} on 12pF load. Typical large bandwidth is given in Figure 6.

Figure 6 : Typical Large Signal Bandwidth



7 - Output Clamp

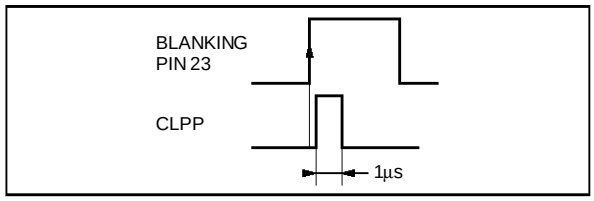
The output clamp centers the output voltages to the desired DC value. As for the brightness loop, the output clamp includes a sample and hold system (please refer to Figure 2).

The sampling is made by an internal pulse.

This pulse (CLPP) is located inside the blanking pulse.

Each blanking pulse will trigger a 1µs internal monostable (see Figure 7).

Figure 7



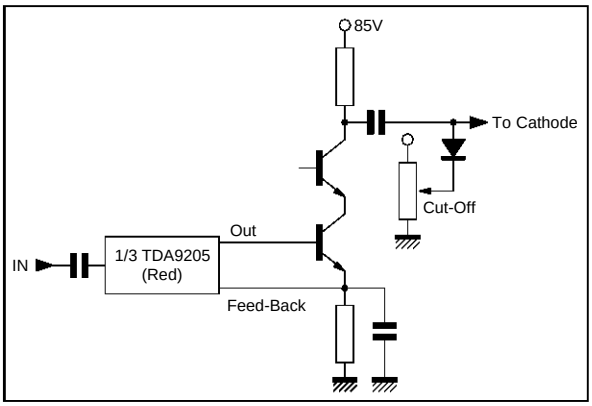
During CLPP, the DC voltage of Pin 40 will be compared to the Red, Green or Blue feed-back signals on Pins 35, 27 or 31.

In order to allow DC or AC coupling between high voltage amplifier and cathode, the polarity of this feed-back signal can be either positive or negative. The desired polarity is selectable by Pin 41.

If Pin 41 is at high level, the feed-back signals (Pins 27-31-35) must have positive polarity (See Figure 8a).

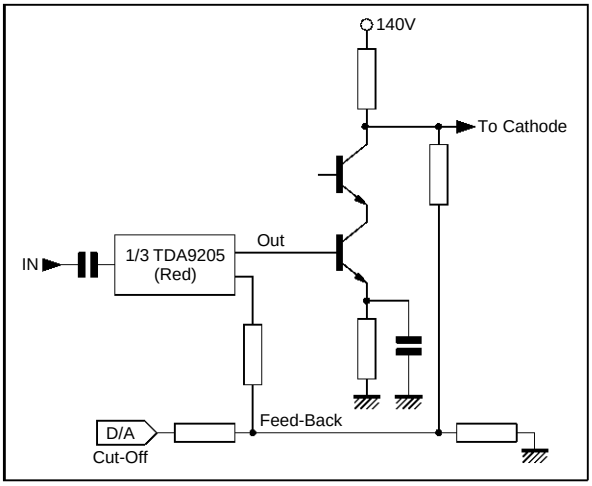
GENERAL DESCRIPTION (continued)

Figure 8a



If Pin 41 is grounded, than the feed-back signals (Pins 27-31-35) must have negative polarity (see Figure 8b).

Figure 8b



The result of the comparison is stored on the external capacitors (Pins 39-25-35). These voltages will then be used by the three internal amplifiers to control the DC level shifter blocks.

The system will stabilize when the output DC levels (on IC output or on the cathode) will reach the value selected by the voltage on Pin 40.

Of course individual DC settings (cut-off) are possible to achieve by inserting a potentiometer (or a system with D/A converter) on each feed-back Pin (see Figure 8b).

8 - Sync Processing

In order to generate the internal backporch clamping pulse, it is necessary to provide the IC with an horizontal sync signal.

This sync can be entered two ways, the first one is through the TTL horizontal synch input (positive or negative polarity, Pin 20), the second one is by using the internal synch extractor input (Pin 18).

This latter allows for example to cope with sync on green standards.

An internal OR function will take either the TTL synch or the composite synch extracted from the composite video input.

The extracted composite pulse is available on Pin 20.

During the vertical pulse, the brightness loop will stay in HOLD mode.

9 - Backporch Pulse Generator

As explained in chapter 3, the backporch clamping pulse which is used in the brightness adjustment loop, is internally generated.

It start just after the end of the sync pulse and its duration is adjustable by the voltage on Pin 24 as shown in the Table here below.

V_{24} (V)	Duration (Typ.) (µs)
0	1.0
$V_{REF}/2$	0.5
V_{REF}	0.35

10 - Voltage Reference

The IC also includes a 5V stable reference voltage (band gap type) which can be used for biasing external potentiometers or external reference voltage input of digital to analog converters.

INTERNAL SCHEMATICS

Figure 4

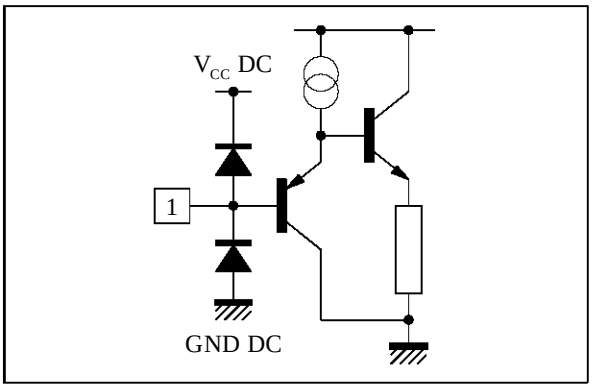


Figure 5

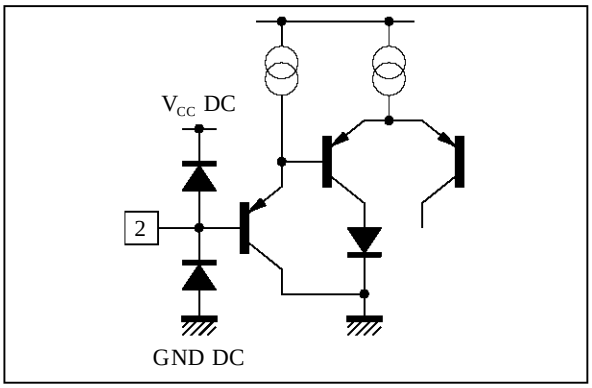


Figure 6

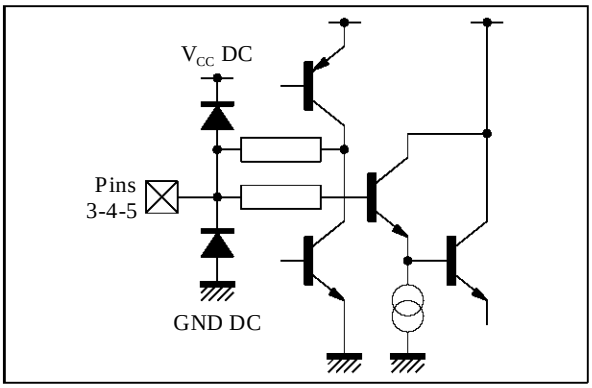


Figure 7

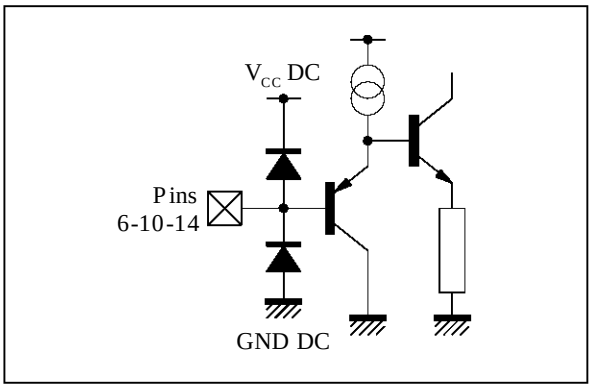


Figure 8

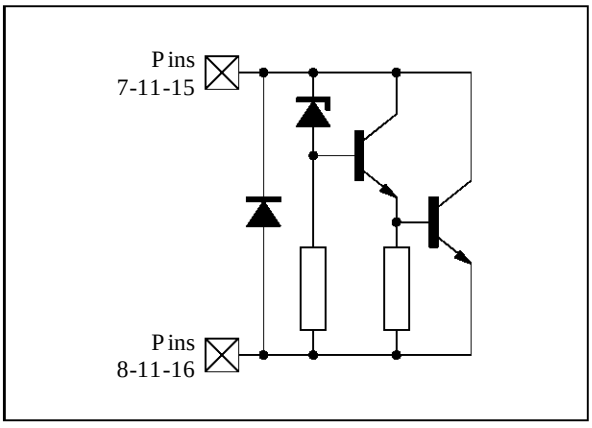
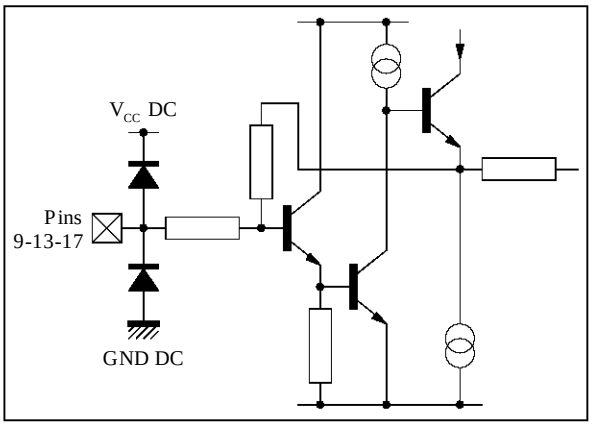


Figure 9



INTERNAL SCHEMATICS (continued)

Figure 10

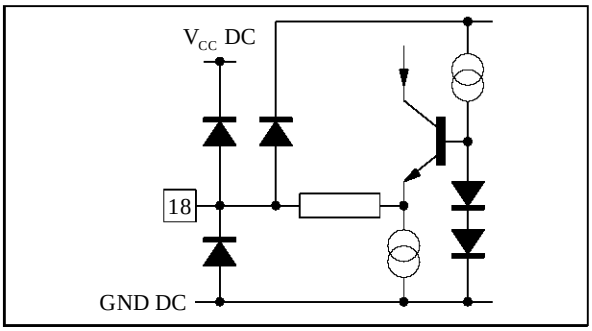


Figure 11

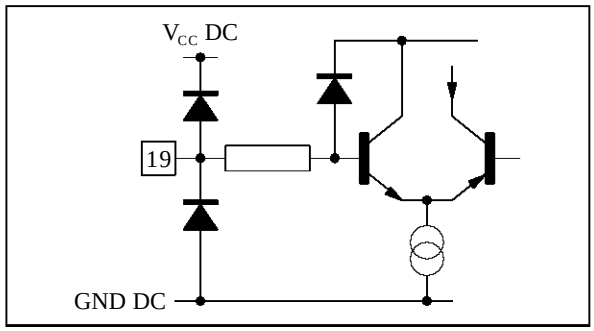


Figure 12

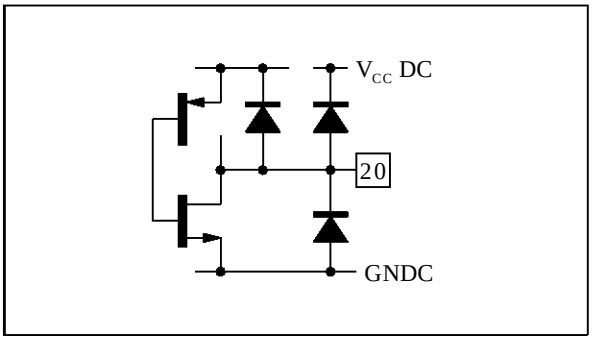


Figure 13

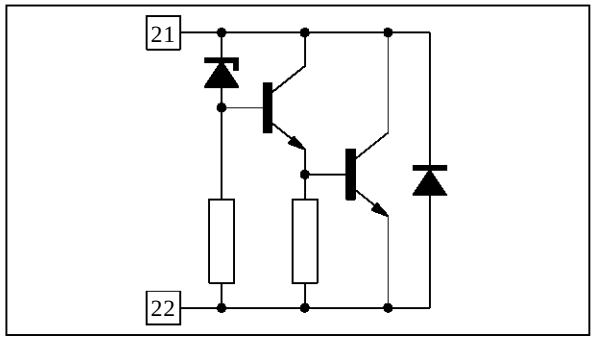


Figure 14

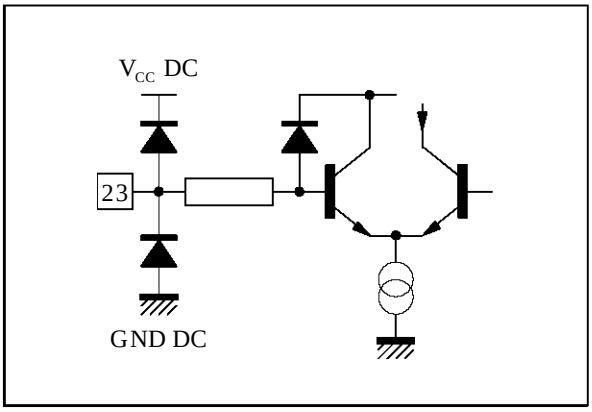


Figure 15

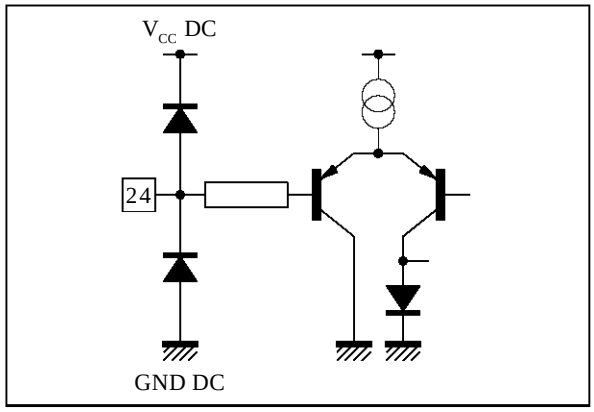


Figure 16

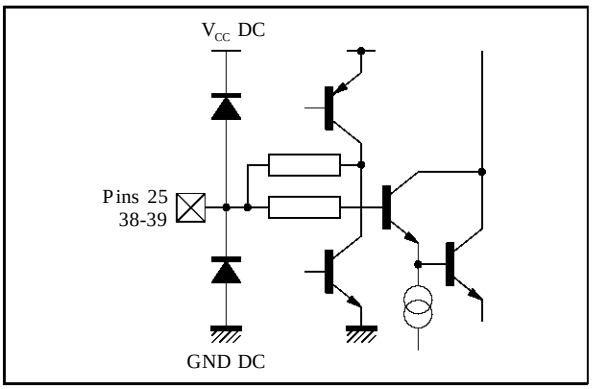
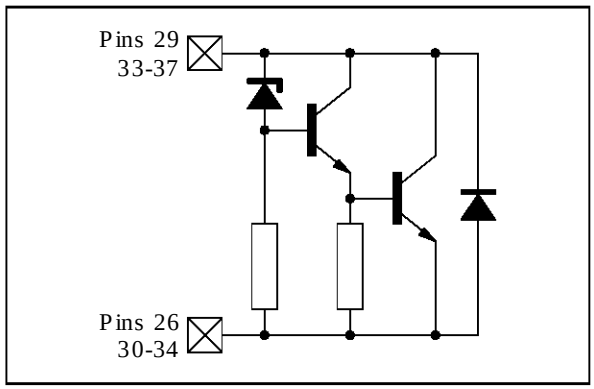


Figure 17



INTERNAL SCHEMATICS (continued)

Figure 18

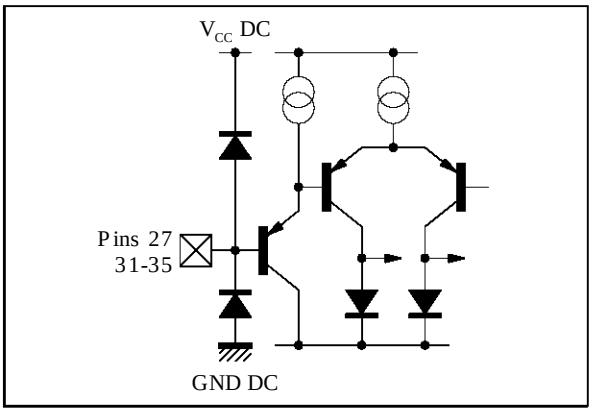


Figure 19

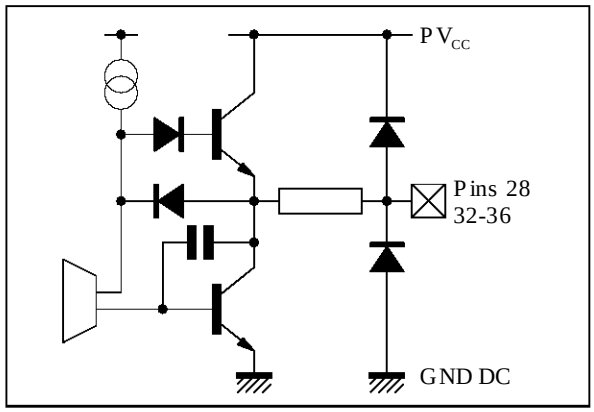


Figure 20

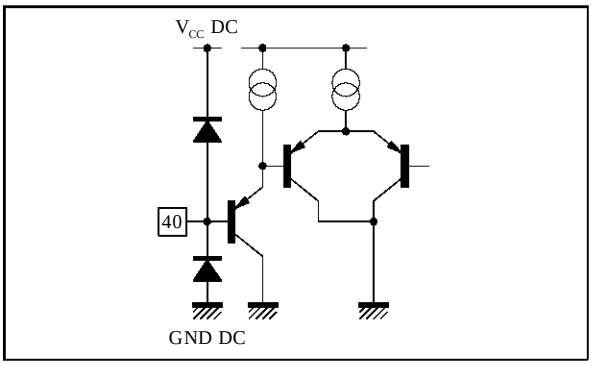


Figure 21

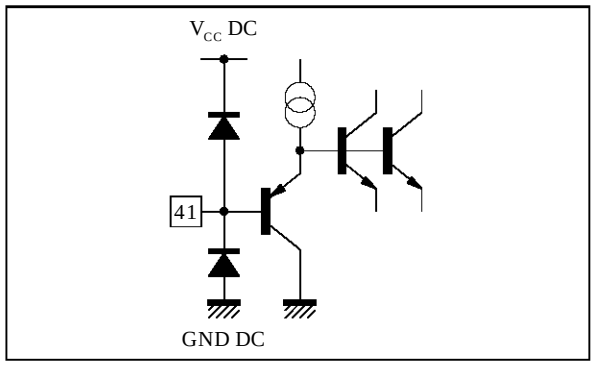
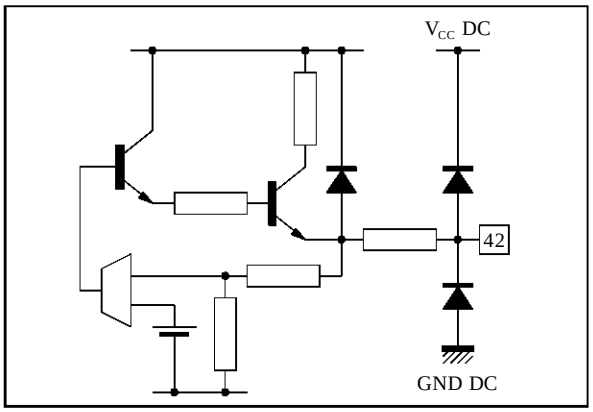
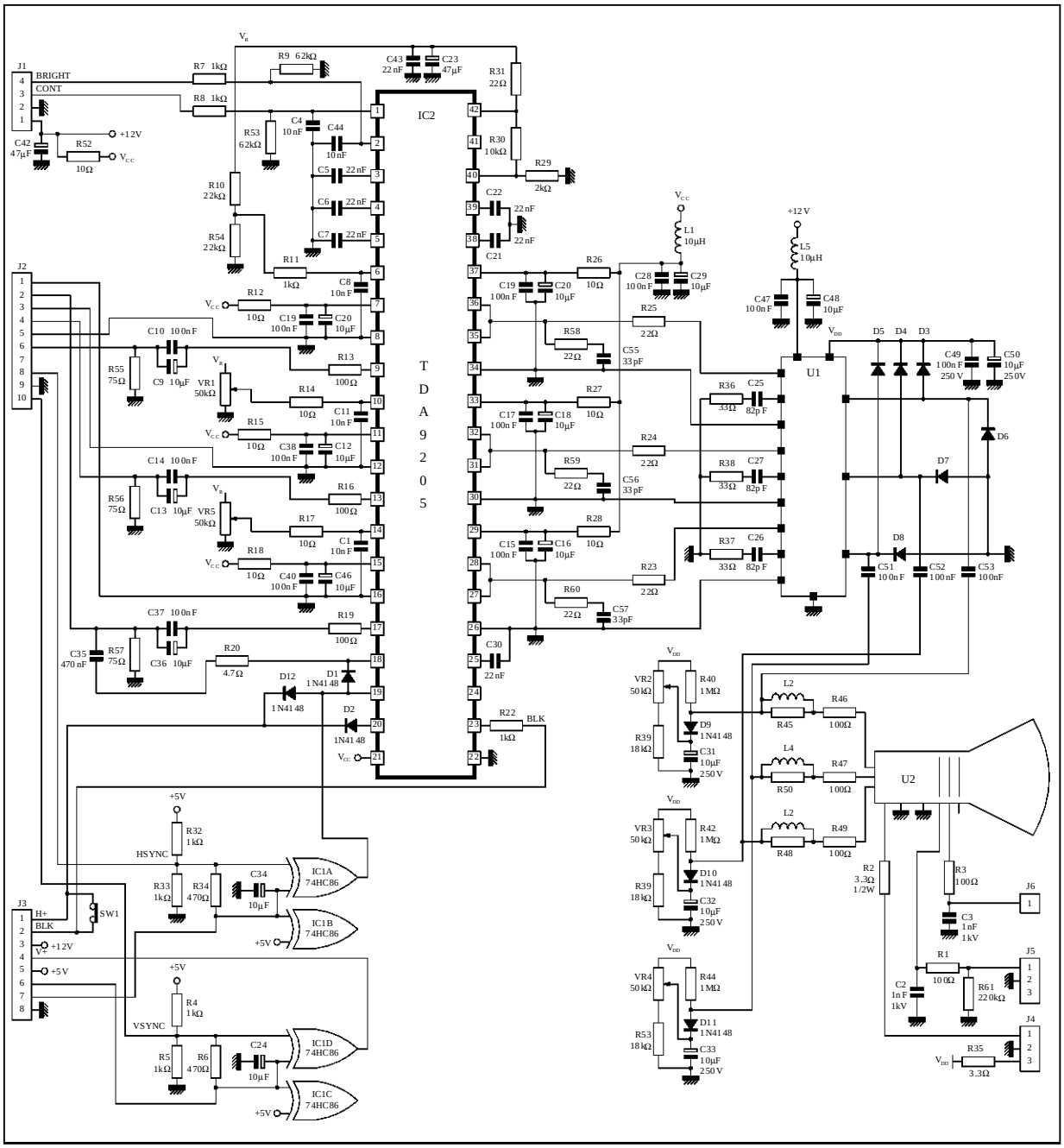


Figure 22

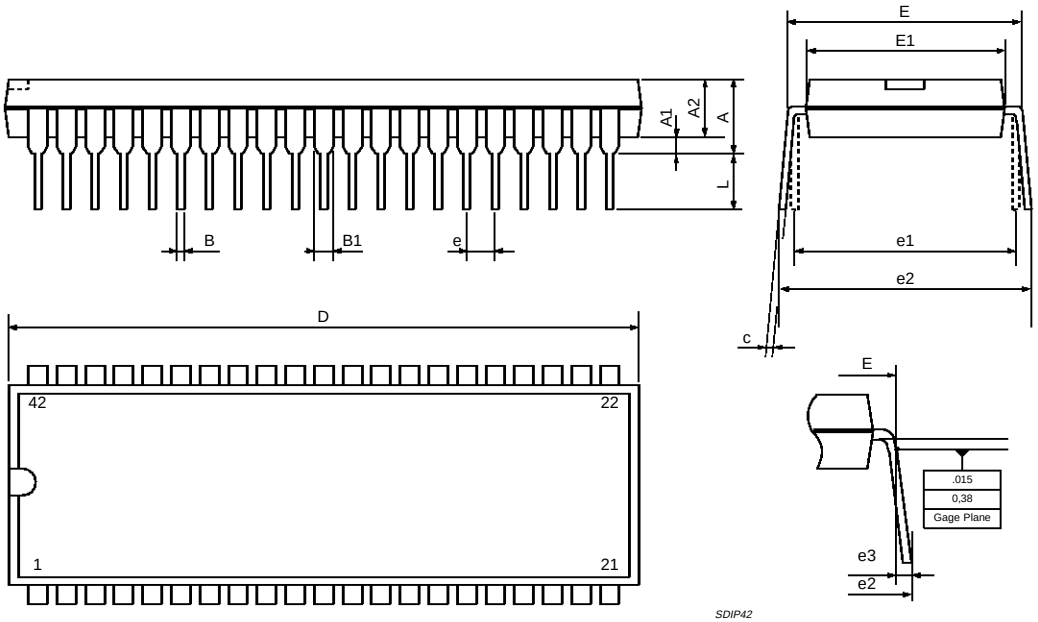


TYPICAL APPLICATION DIAGRAM



PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	37.85	38.10	38.35	1.490	1.5	1.510
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

SDIP42.TBL