TDA9917

8-bit, up to 250 Msample/s Analog-to-Digital Converter (ADC)

Rev. 01 — 9 June 2006 Objective data sheet

1. General description

The TDA9917 is a differential, high-speed, 8-bit Analog-to-Digital Converter (ADC) optimized for telecommunication transmission control systems and tape drive applications.

The TDA9917 offers the selection between Low-Voltage Differential Signals (LVDS) and 1.8 V Complementary Metal Oxide Semiconductor (CMOS) levels interface for the clock. The output data interface is 1.8 V CMOS levels. It allows to sample the signal up to 250 Msample/s. All static digital inputs (CLKSEL, CCSSEL, CE_N, OTC, DEL0 and DEL1) are 1.8 V CMOS compatible. The TDA9917 offers the most possible flexible acquisition control system thanks to its programmable Complete Conversion Signal (CCS) that allows to adjust the delay of the acquisition clock and its frequency.

The TDA9917 is released in HTQFP48 package.

2. Features

- 8-bit resolution
- High-speed sampling rate up to 250 Msample/s
- Maximum analog input frequency up to 450 MHz
- Programmable acquisition output clock (complete conversion signal)
- Differential analog input
- Integrated voltage regulator or external control for analog input full-scale
- Integrated voltage regulator for input common-mode reference
- Selectable 1.8 V CMOS or LVDS clock input
- 1.8 V CMOS digital outputs
- 1.8 V CMOS compatible static digital inputs
- Binary or two’s complement CMOS outputs
- Only 2 clock cycles latency
- Industrial temperature range from –40 °C to +85 °C
- HTQFP48 package

3. Applications

- 2.5G and 3G cellular base infrastructure radio transceivers
- Wireless access systems
- Fixed telecommunication
- Optical networking
- Wireless Local Area Network (WLAN) infrastructure

PHILIPS

- Tape drive

4. Ordering information

Table 1. Ordering information

Type number	Sampling frequency	Package		
		Name	Description	Version
TDA9917HW/12/C1	125 Msample/s	HTQFP48	plastic thermal enhanced thin quad flat package; 48 leads; body 7 × 7 × 1 mm; exposed die pad	SOT545-2
TDA9917HW/25/C1	250 Msample/s			

5. Block diagram

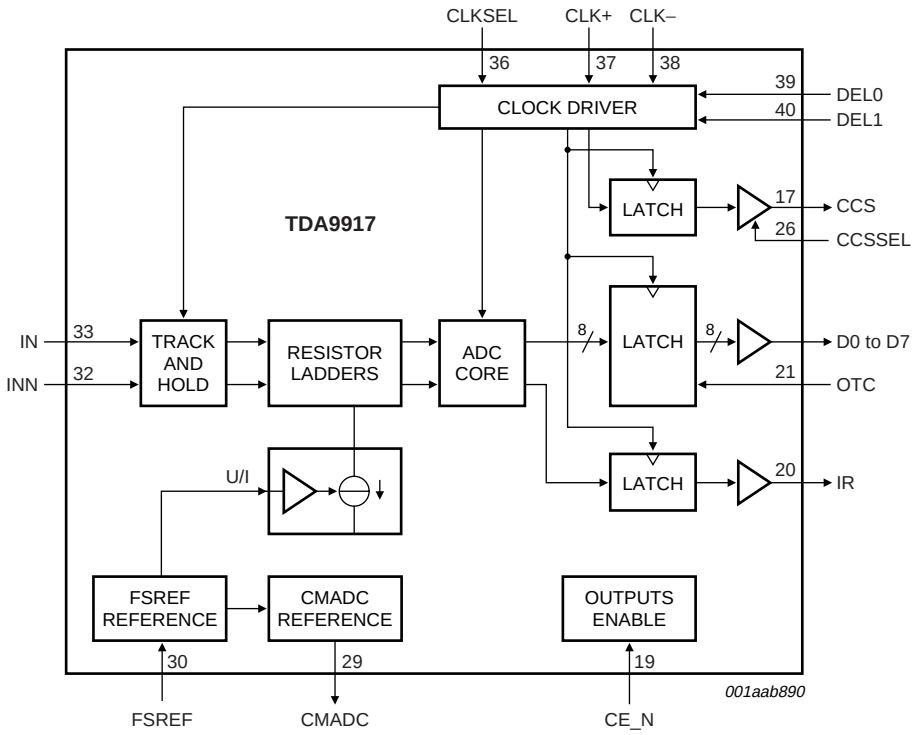


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

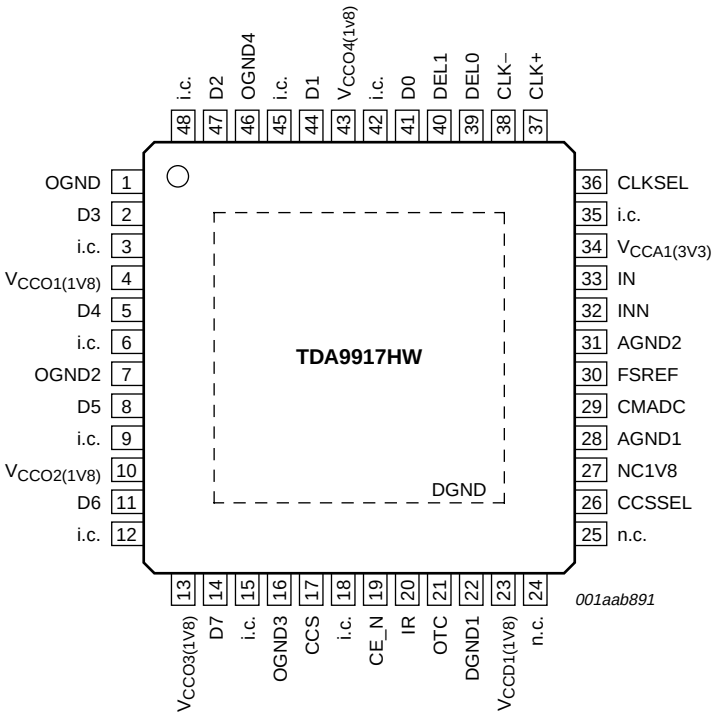


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
OGND1	1	G	data output ground 1
D3	2	O	data output bit 3
i.c.	3	-	internally connected; leave open
$V_{CCO1(1V8)}$	4	P	data output supply voltage 1 (1.8 V)
D4	5	O	data output bit 4
i.c.	6	-	internally connected; leave open
OGND2	7	G	data output ground 2
D5	8	O	data output bit 5
i.c.	9	-	internally connected; leave open
$V_{CCO2(1V8)}$	10	P	data output supply voltage 2 (1.8 V)
D6	11	O	data output bit 6
i.c.	12	-	internally connected; leave open
$V_{CCO3(1V8)}$	13	P	data output supply voltage 3 (1.8 V)
D7	14	O	data output bit 7

Table 2. Pin description *...continued*

Symbol	Pin	Type	Description
i.c.	15	-	internally connected; leave open
OGND3	16	G	data output ground 3
CCS	17	O	complete conversion signal output
i.c.	18	-	internally connected; leave open
CE_N	19	I(CMOS)	chip enable input (active LOW)
IR	20	O(CMOS)	in-range output
OTC	21	I(CMOS)	control input for two's complement output (active HIGH)
DGND1	22	G	digital ground 1
$V_{CCD1(1V8)}$	23	P	digital supply voltage 1 (1.8 V)
n.c.	24	-	not connected
n.c.	25	-	not connected
CCSSEL	26	I(CMOS)	control input for CCS frequency selection
NC1V8	27	I	not connected or connected to $V_{CCD1(1V8)}$
AGND1	28	G	analog ground 1
CMADC	29	O	regulator common-mode ADC output
FSREF	30	I	full-scale reference voltage input
AGND2	31	G	analog ground 2
INN	32	I	complementary analog input
IN	33	I	analog input
$V_{CCA1(3V3)}$	34	P	analog supply voltage 1 (3.3 V)
i.c.	35	-	internally connected; leave open
CLKSEL	36	I(CMOS)	control input for input clock selection
CLK+	37	I	clock input
CLK–	38	I	complementary clock input
DEL0	39	I(CMOS)	complete conversion signal delay input 0
DEL1	40	I(CMOS)	complete conversion signal delay input 1
D0	41	O	data output bit 0
i.c.	42	-	internally connected; leave open
$V_{CCO4(1V8)}$	43	P	data output supply voltage 4 (1.8 V)
D1	44	O	data output bit 1
i.c.	45	-	internally connected; leave open
OGND4	46	G	data output ground 4
D2	47	O	data output bit 2
i.c.	48	-	internally connected; leave open
DGND	-	G	digital ground; exposed die pad

Table 3. Pin type description

Type	Description
I	input
O	output
I(CMOS)	1.8 V CMOS level input

Table 3. Pin type description *…continued*

Type	Description
O(CMOS)	1.8 V CMOS level output
P	power supply
G	ground

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	<tbd>	<tbd>	V
V_{CCD}	digital supply voltage		[1]	<tbd>	<tbd>	V
V_{CCO}	output supply voltage		[2]	<tbd>	<tbd>	V
ΔV_{CC}	supply voltage difference					
	$V_{CCA} - V_{CCD}$			<tbd>	<tbd>	V
	$V_{CCD} - V_{CCO}$			<tbd>	<tbd>	V
	$V_{CCA} - V_{CCO}$			<tbd>	<tbd>	V
$V_{i(IN)}$	input voltage on pin IN	referenced to AGND		<tbd>	<tbd>	V
$V_{i(INN)}$	input voltage on pin INN	referenced to AGND		<tbd>	<tbd>	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage	referenced to DGND		<tbd>	<tbd>	V
I_O	output current			<tbd>	<tbd>	mA
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	150	°C

[1] The supply voltages V_{CCA} and V_{CCD} may have any value between –0.5 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

[2] The supply voltage V_{CCO} may have any value between –0.5 V and +5.0 V provided that the supply voltage differences ΔV_{CC} are respected.

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	<tbd>	K/W
$R_{th(c-a)}$	thermal resistance from case to ambient	in free air	<tbd>	K/W

9. Static characteristics

Table 6. Static characteristics

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; $V_{ref(fs)}$ = 0 V; typical values are measured at V_{CCA} = 3.3 V and $V_{CCD} = V_{CCO}$ = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			3.0	3.3	3.6	V
V_{CCD}	digital supply voltage			1.65	1.8	1.95	V
V_{CCO}	output supply voltage			1.65	1.8	1.95	V
I_{CCA}	analog supply current			-	56	<tbd>	mA
I_{CCD}	digital supply current			-	7	<tbd>	mA
I_{CCO}	output supply current	f_{clk} = 125 Msample/s; f_i = 1.25 MHz		-	9	<tbd>	mA
P_{tot}	total power dissipation	f_{clk} = 125 Msample/s; f_i = 1.25 MHz		-	215	<tbd>	mW
Clock inputs: pins CLK+ and CLK− [1]							
R_i	input resistance			-	10	-	kΩ
C_i	input capacitance			-	1	-	pF
LVDS clock input							
ΔV_I	input voltage range	V_I on pin CLK+ or CLK−; $\|V_{gpd}\|$ < 50 mV	[2]	825	-	1575	mV
V_{idth}	input differential threshold voltage	$\|V_{gpd}\|$ < 50 mV	[2]	−100	-	+100	mV
I_I	input current	825 mV < V_I < 1575 mV	[3]	-	-	<tbd>	µA
1.8 V CMOS clock input							
V_{IL}	LOW-level input voltage			DGND	-	$0.2V_{CCD}$	mV
V_{IH}	HIGH-level input voltage			$0.8V_{CCD}$	-	V_{CCD}	
I_{IL}	LOW-level input current	$V_{IL} = 0.2V_{CCD}$	[3]	<tbd>	<tbd>	-	µA
I_{IH}	HIGH-level input current	$V_{IH} = 0.8V_{CCD}$		-	<tbd>	<tbd>	µA
Analog inputs: pins IN and INN							
I_{IL}	LOW-level input current	$V_{ref(fs)}$ = 1.25 V		-	<tbd>	-	µA
I_{IH}	HIGH-level input current	$V_{ref(fs)}$ = 1.25 V		-	<tbd>	-	µA
R_i	input resistance		[3]	-	1.0	-	MΩ
C_i	input capacitance		[3]	-	1.0	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{i(IN)} = V_{i(INN)}$; output code = 127		-	0.95	-	V
Digital inputs pins: OTC, CE_N, DEL0, DEL1, CLKSEL and CCSSEL							
V_{IL}	LOW-level input voltage			DGND	-	$0.3V_{CCD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{CCD}$	-	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.2V_{CCD}$		<tbd>	<tbd>	-	µA
I_{IH}	HIGH-level input current	$V_{IH} = 0.8V_{CCD}$		-	<tbd>	<tbd>	µA

Table 6. Static characteristics *...continued*

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; $V_{ref(fs)}$ = 0 V; typical values are measured at V_{CCA} = 3.3 V and $V_{CCD} = V_{CCO}$ = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage controlled regulator output: pin CMADC						
$V_{O(cm)}$	common-mode output voltage		-	0.95	-	V
Reference voltage input: pin FSREF[4]						
$V_{ref(fs)}$	full-scale reference voltage	internal reference	-	0	-	V
		external reference	-	1.25	-	V
$I_{i(FSREF)}$	input current on pin FSREF		-	12	-	µA
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage		<tbd>	2.0	<tbd>	V
Digital outputs: pins D0 to D7, CCS and IR						
V_{OL}	LOW-level output voltage		OGND	-	0.4	V
V_{OH}	HIGH-level output voltage		$0.85V_{CCO}$	-	V_{CCO}	V

[1] The circuit has two clock inputs: CLK+ and CLK−. There are 2 modes of operation:
   a) LVDS mode: CLK+ and CLK− inputs are at differential LVDS levels. An external resistor between 80 Ω and 120 Ω is needed.
   b) 1.8 V CMOS mode: CLK+ input is at 1.8 V CMOS level and sampling is taken on the rising edge of the clock input signal. In that case pin CLK− has to be grounded.

[2] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltages.

[3] Guaranteed by design.

[4] The ADC input range can be adjusted with an external reference voltage supplied to pin FSREF. This voltage has to be referenced to AGND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; $V_{ref(fs)}$ = 0 V; typical values are measured at V_{CCA} = 3.3 V and $V_{CCD} = V_{CCO}$ = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock timing input: pins CLK+ and CLK−						
$f_{clk(min)}$	minimum clock frequency		-	-	<tbd>	Msample/s
$f_{clk(max)}$	maximum clock frequency					
	TDA9917HW/12		125	-	-	Msample/s
	TDA9917HW/25		250	-	-	Msample/s
$t_{w(clk)}$	clock pulse width	f_{clk} = 125 Msample/s	2	-	-	ns
		f_{clk} = 250 Msample/s	2	-	-	ns
Timing output: pins D0 to D7 and IR[1] (see Figure 3)						
$t_{d(s)}$	sampling delay time	1.8 V CMOS clock	-	1.2	<tbd>	ns
		LVDS clock	-	1.7	<tbd>	ns
$t_{h(o)}$	output hold time	1.8 V CMOS clock	3.5	4.4	-	ns
		LVDS clock	4.2	4.9	-	ns

Table 7. Dynamic characteristics *...continued*

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; $V_{ref(fs)}$ = 0 V; typical values are measured at V_{CCA} = 3.3 V and $V_{CCD} = V_{CCO}$ = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(o)}$	output delay time	1.8 V CMOS clock		-	5.7	6.9	ns
		LVDS clock		-	6.4	7.3	ns
Timing complete conversion signal: pin CCS (see Figure 4)							
$f_{CCS(max)}$	maximum CCS frequency			125	-	-	Msample/s
$t_{d(o)}$	output delay time	DEL0 = HIGH; DEL1 = LOW		-	0	-	ns
		DEL0 = LOW; DEL1 = HIGH		-	1	-	ns
		DEL0 = HIGH; DEL1 = HIGH		-	2	-	ns
3-state output delay time: pin CCS and IR							
t_{dZH}	float to active HIGH delay time			-	2.1	-	ns
t_{dZL}	float to active LOW delay time			-	2.2	-	ns
t_{dHZ}	active HIGH to float delay time			-	3.3	-	ns
t_{dLZ}	active LOW to float delay time			-	2.9	-	ns
Analog signal processing (50 % clock duty factor); see Section 11							
INL	integral non-linearity	f_{clk} = 20 Msample/s; f_i = 21.4 MHz		-	±0.9	<tbd>	LSB
DNL	differential non-linearity	f_{clk} = 20 Msample/s; f_i = 21.4 MHz; no missing code guaranteed		-	±0.4	<tbd>	LSB
E_O	offset error	V_{CCA} = 3.3 V; V_{CCD} = 1.8 V; T_{amb} = 25 °C; output code = 127		-	2.5	-	mV
E_G	gain error	spread from device to device; V_{CCA} = 3.3 V; V_{CCD} = 1.8 V; T_{amb} = 25 °C		<tbd>	2	<tbd>	%FS
B	bandwidth	f_{clk} = 125 Msample/s; −3 dB; full-scale input	[2]	-	560	-	MHz
THD	total harmonic distortion	f_{clk} = 125 Msample/s; f_i = 75 MHz	[3]	-	−50	-	dBFS
		f_{clk} = 250 Msample/s; f_i = 125 MHz		-	−50	-	dBFS
$N_{th(RMS)}$	RMS thermal noise	shorted input; f_{clk} = 125 Msample/s		-	0.6	-	LSB
S/N	signal-to-noise ratio	f_{clk} = 125 Msample/s; f_i = 75 MHz	[4]	-	49.5	-	dBc
		f_{clk} = 250 Msample/s; f_i = 125 MHz		-	49	-	dBc
SFDR	spurious free dynamic range	B = Nyquist		-	-	-	dBc
		f_{clk} = 125 Msample/s; f_i = 75 MHz		-	57	-	dBc
		f_{clk} = 250 Msample/s; f_i = 125 MHz		-	55	-	dBc
ACPR	adjacent channel power ratio			-	<tbd>	-	dB

Table 7. Dynamic characteristics *...continued*

V_{CCA} = 3.0 V to 3.6 V; V_{CCD} = 1.65 V to 1.95 V; V_{CCO} = 1.65 V to 1.95 V; pins AGND1, AGND2 and DGND1 shorted together; T_{amb} = −40 °C to +85 °C; $V_{i(IN)} - V_{i(INN)}$ = 2.0 V − 0.5 dB; $V_{I(cm)}$ = 0.95 V; $V_{ref(fs)}$ = 0 V; typical values are measured at V_{CCA} = 3.3 V and $V_{CCD} = V_{CCO}$ = 1.8 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IMD2	second-order intermodulation distortion	f_{i1} = 74 MHz; f_{i2} = 76 MHz; f_{clk} = 125 Msample/s	[5]	-	<tbd>	-	dBFS
		f_{i1} = 174 MHz; f_{i2} = 176 MHz; f_{clk} = 250 Msample/s		-	−52	-	dBFS
IMD3	third-order intermodulation distortion	f_{i1} = 74 MHz; f_{i2} = 76 MHz; f_{clk} = 125 Msample/s	[5]	-	−51	-	dBFS
		f_{i1} = 174 MHz; f_{i2} = 176 MHz; f_{clk} = 250 Msample/s		-	−59	-	dBFS
BER	bit error rate	f_i = <tbd> MHz; V_i = ±<tbd> LSB at code 127; f_{clk} = <tbd> Msample/s		-	−64	-	time/ sample

[1] Output data acquisition: the output data is available after the maximum delay of $t_{d(o)}$.

[2] The −3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.

[3] The total harmonic distortion is obtained with the addition of the first five harmonics.

[4] The signal-to-noise ratio takes into account all harmonics above five and noise up to Nyquist frequency.

[5] Intermodulation measured relative to either tone with analog input frequencies f_{i1} and f_{i2}. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (−6 dB below full-scale for each input signal). IMD3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.

Table 8. Output coding with differential inputs

$V_{I(p-p)}$ = 2.0 V; $V_{ref(fs)}$ = 1.25 V; typical values to AGND.

Code	Inputs		Output	Outputs D7 to D0	
	$V_{i(IN)}$	$V_{i(INN)}$	IR	Binary	Two's complement
Underflow	< 0.45	> 1.45	LOW	0000 0000	1000 0000
0	0.45	1.45	HIGH	0000 0000	1000 0000
1	-	-	HIGH	0000 0001	1000 0001
...	...	...	...	...	...
127	0.95	0.95	HIGH	0111 1111	1111 1111
...	...	...	...	...	...
254	-	-	HIGH	1111 1110	0111 1110
255	1.45	0.45	HIGH	1111 1111	0111 1111
Overflow	> 1.45	< 0.45	LOW	1111 1111	0111 1111

Table 9. Output format selection

Two's complement outputs	Chip enable	Output data
Pin OTC	**Pin CE_N**	**Pins D0 to D7, CCS and IR**
LOW	LOW	active; binary
HIGH	LOW	active; two's complement
X [1]	HIGH	high-impedance

[1] X = don't care.

Table 10. Input clock format selection

Control input for input clock selection	Input clock
Pin CLKSEL	**Pins CLK+ and CLK–**
HIGH or not connected	LVDS
LOW	1.8 V CMOS; do not connect pin CLK–

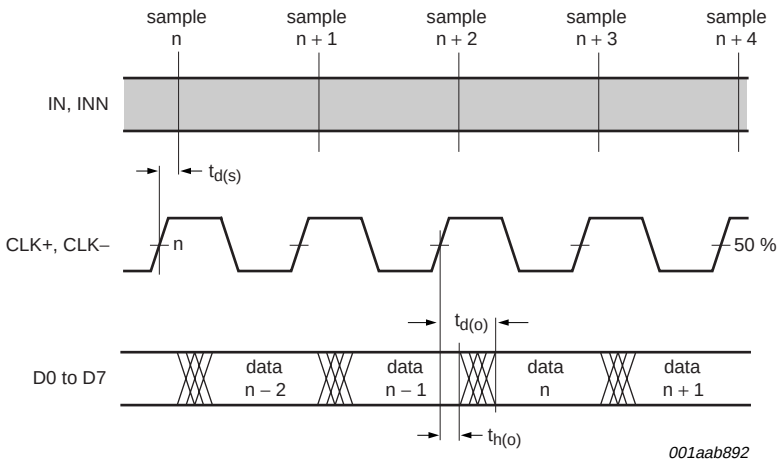


Fig 3. Output timing diagram, standard mode

Table 11. Full-scale input selection

Full-scale fixed voltage $V_{ref(fs)}$	Common-mode output voltage $V_{O(cm)}$	Maximum input voltage amplitude $V_{i(p-p)}$
1.15 V	0.8 V	1.82 V
1.20 V	0.86 V	1.91 V
1.25 V	0.94 V	1.99 V
1.30 V	1.01 V	2.08 V
1.35 V	1.09 V	2.16 V

The TDA9917 has an internal reference circuit which can be overruled by an external reference voltage. This could be done with the full-scale reference voltage ($V_{ref(fs)}$) according to Table 11. When pin FSREF is connected to ground, the circuit will switch to its internal reference. Then the input common-mode will be 0.95 V and the full-scale input will be 2.0 V.

The ADC provides the required common-mode voltage on pin CMADC. In case of internal regulation, the regulator output voltage on pin CMADC is 0.95 V.

Table 12. Complete conversion signal selection

Pin DEL1	Pin DEL0	Pin CCS
LOW	LOW	high-impedance
LOW	HIGH	active
HIGH	LOW	
HIGH	HIGH	

The TDA9917 generates an adjustable clock output called Complete Conversion Signal (CCS), which can be used to control the acquisition of converted output data by the digital circuit connected to the TDA9917 output data bus.

Two logic input pins DEL0 and DEL1 allow to adjust the delay of the edge of the CCS signal to achieve an optimal position in the stable, usable zone of the data. Pin CLKSEL allows the selection of the CCS frequency; see Table 13.

Table 13. Complete conversion signal frequency selection

Control input for CCS frequency selection (pin CCSSEL)	CCS frequency (f_{CCS})
HIGH or not connected	f_{clk}
LOW	$f_{clk}/2$

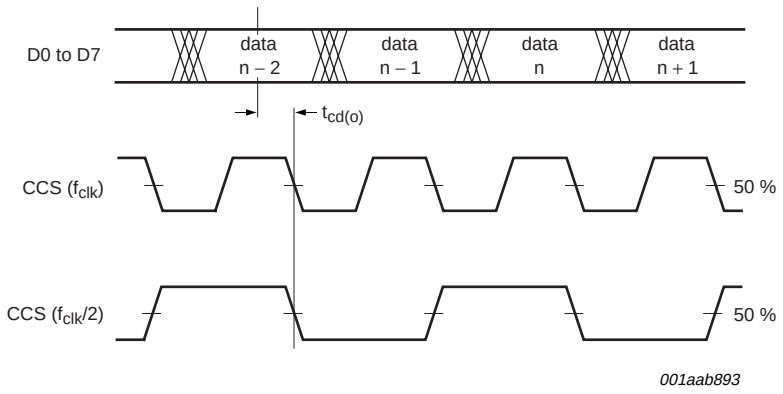


Fig 4. Complete conversion signal timing diagram, standard mode

11. Definitions

11.1 Static parameters

11.1.1 INL (integral non-linearity)

It is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of the code i is obtained from the equation:

$$INL(i) = \frac{V_I(i) - V_I(ideal)}{S}$$

where:

S = corresponding to the slope of the ideal straight line (code width)

i = corresponding to the code value.

11.1.2 DNL (differential non-linearity)

It is the deviation in code width from the value of 1 LSB.

$$DNL(i) = \frac{V_I(i+1) - V_I(i)}{S}$$

where:

$$i = 0x(2^n - 2)$$

11.2 Dynamic parameters

Figure 5 shows the spectrum of a single tone full-scale input sine wave with frequency f_t, conforming to coherent sampling (f_t/f_s = M/N, with M number of cycles and N number of samples, M and N being relatively prime), and digitized by the ADC under test.

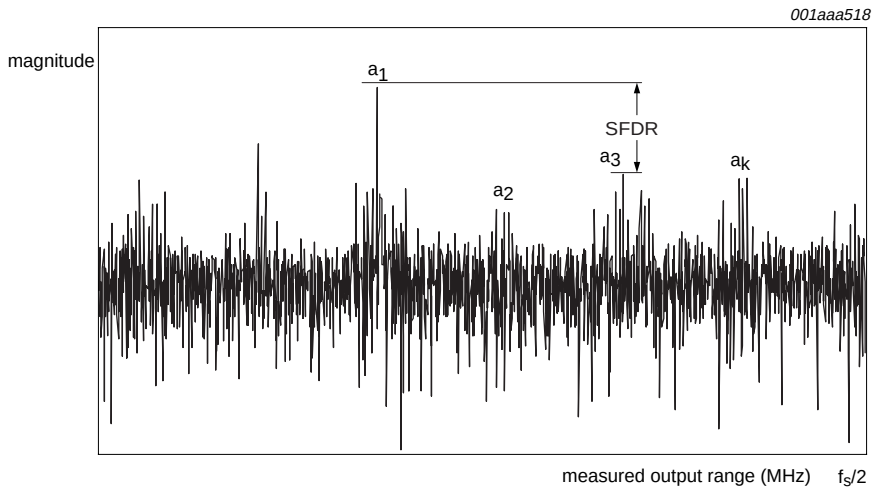


Fig 5. Single tone spectrum of full-scale input sine wave with frequency f_t

Remark: in the following equations, P_{noise} is the power of the terms which include the effects of random noise, non-linearities, sampling time errors, and 'quantization noise'.

11.2.1 SINAD (signal-to-noise and distortion)

The ratio of the output signal power to the noise plus distortion power for a given sample rate and input frequency, excluding the DC component:

$$SINAD[dB] = 10 \times log_{10}\left(\frac{P_{signal}}{P_{noise+distorsion}}\right)$$

11.2.2 ENOB (effective number of bits)

It is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

11.2.3 THD (total harmonic distortion)

The ratio of the power of the harmonics to the power of the fundamental.

For k–1 harmonics the THD is:

$$THD(dB) = 10log_{10}\left(\frac{P_{harmonics}}{P_{signal}}\right)$$

where:

$$P_{harmonics} = a_2^2 + a_3^2 + ... + a_k^2$$

$$P_{signal} = a_1^2$$

The value of k is usually 6 (i.e. calculation of THD is done on the first 5 harmonics).

11.2.4 S/N (signal-to-noise ratio)

The ratio of the output signal power to the noise power, excluding the harmonics and the DC component is:

$$S/N[dB] = 10log_{10}\left(\frac{P_{signal}}{P_{noise}}\right)$$

11.2.5 SFDR (spurious free dynamic range)

The number SFDR specifies the available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious harmonic and non-harmonic, excluding DC component:

$$SFDR[dB] = 20 \times log_{10}\left(\frac{a_1}{max(S)}\right)$$

11.2.6 IMD2 and IMD3

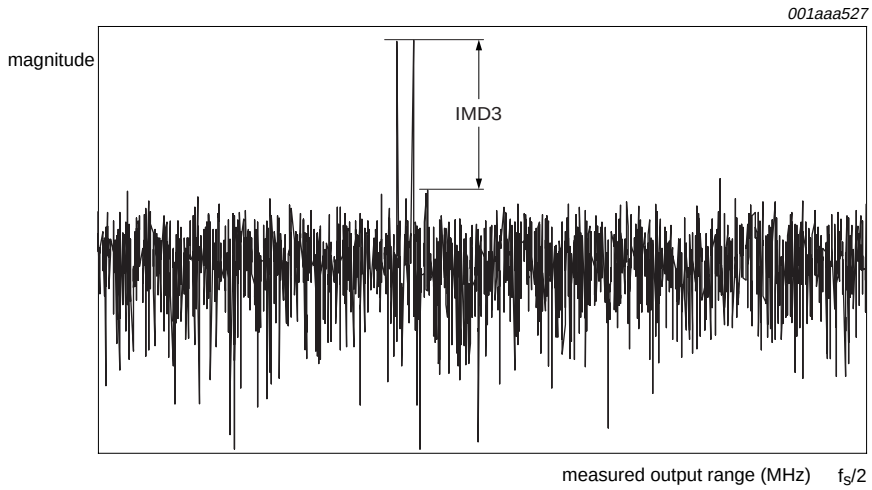


Fig 6. Spectral of dual tone input sine wave with frequency

From a dual-tone input sinusoid (f_{t1} and f_{t2}, these frequencies being chosen according to the coherence criterion), the intermodulation distortion products IMD2 and IMD3 (respectively, 2nd and 3rd order components) are defined as follows:

The ratio of the RMS value of either tone to the RMS value of the worst second (third) order intermodulation product.

The total intermodulation distortion IMD is given by:

$$IMD[dB] = 10log_{10}\left(\frac{P_{intermod}}{P_{signal}}\right)$$

where:

$$P_{intermod} = a^2_{im(f_{t1}-f_{t2})} - a^2_{im(f_{t1}+f_{t2})} + a^2_{im(f_{t1}-2f_{t2})} + a^2_{im(f_{t1}+2f_{t2})} + \ldots$$
$$\ldots + a^2_{im(2f_{t1}-f_{t2})} + a^2_{im(2f_{t1}+f_{t2})}$$

with:

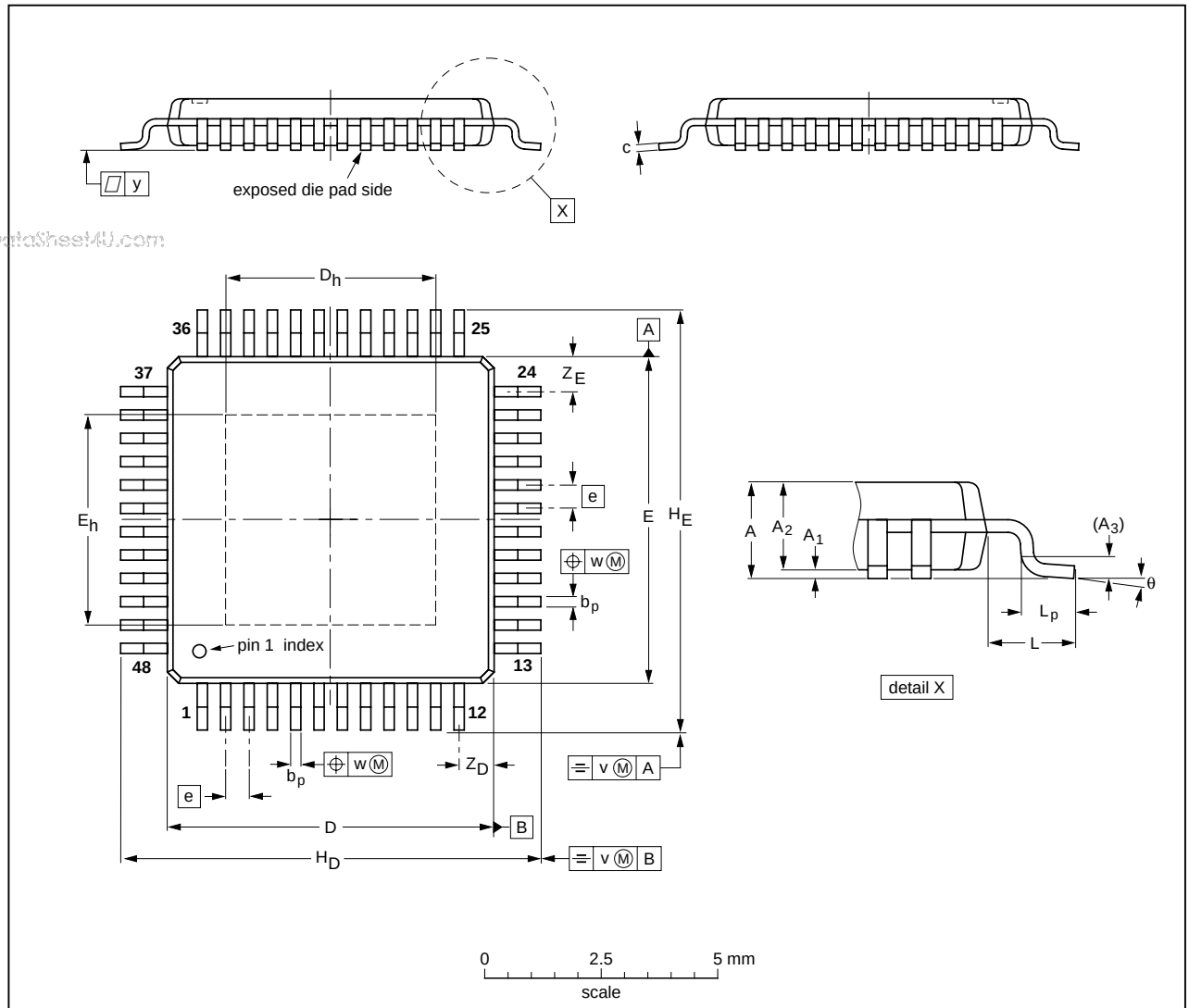
$a^2_{im(f_{t1})}$ corresponding to the power in the intermodulation component at frequency f_t.

$$P_{signal} = a^2_{f_{t1}} + a^2_{f_{t2}}$$

12. Package outline

HTQFP48: plastic thermal enhanced thin quad flat package; 48 leads; body 7 x 7 x 1 mm; exposed die pad

SOT545-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	7.1 6.9	4.6 4.4	7.1 6.9	4.6 4.4	0.5	9.1 8.9	9.1 8.9	1	0.75 0.45	0.2	0.08	0.08	0.9 0.6	0.9 0.6	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT545-2		MS-026				~~03-04-07~~ 04-01-29

Fig 7. Package outline SOT545-2 (HTQFP48)

13. Soldering

13.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 14. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume $mm^3 < 350$	Volume $mm^3 \geq 350$
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 15. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume $mm^3 < 350$	Volume mm^3 350 to 2000	Volume $mm^3 > 2000$
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 16. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9917_1	20060609	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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