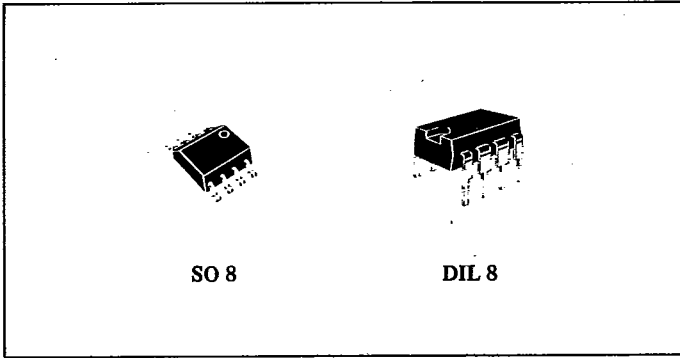




TD•0062

Low power dual BI-FET operational amplifiers.



The TD•0062, are high speed dual J-FET input operational amplifiers. Each of these incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rate, low input bias and offset currents, and low offset voltage temperature coefficient.

- Very low power consumption.
- Wide common-mode and differential voltage ranges.
- Low input bias and offset currents.
- Typical supply current 200 μ A.
- Output short-circuit protection.
- High impedance J-FET input stage.
- Internal frequency compensation.
- Latch-up free operation.
- High slew rate 3.5 V/ μ s typ.

BI-FET OPERATIONAL AMPLIFIERS

CHARACTERISTIC	SYMBOL	UNIT	SINGLE								DUAL				QUAD			
			1	2	3	4	5	6	7	8	1	2	3	4	1	2	3	4
Supply voltage	V_{CC} max.	V	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	± 18	
Input offset voltage	V_{IO} max.	mV	10	15	10	10	10	10	15	10	15	10	15	10	15	10	15	
Input offset current	I_{IO} max.	nA	0.05	0.2	0.05	0.05	0.05	0.1	0.2	0.05	0.2	0.1	0.2	0.05	0.2	0.1	0.2	
Input impedance	Z_I typ.	$10^6 \Omega$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Input bias current	I_B max.	nA	0.2	0.4	0.2	0.2	0.2	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	0.2	0.4	
Slew rate	S_{VO} typ.	V/ μ s	13	13	5	12	50	13	3.5	13	13	13	3.5	13	13	13	13	
Supply voltage rejection ratio	S_{VR} min.	dB	70	70	80	80	80	70	70	70	70	70	70	70	70	70	70	
Gain x bandwidth	B typ.	MHz	3	3	2.5	4.5	20	4	1	3	3	4	1	3	3	4	1	
Voltage gain	A_{V} min.	V/mV	25	25	25	25	25	25	3	25	25	25	3	25	25	25	25	
Input voltage range	(V_I) max. min.	V	± 11	± 10	± 10	± 10	± 10	± 11	± 10	± 11	± 10	± 11	± 10	± 11	± 10	± 11	± 11	

TD•0071 TD•0081 TD•0155 TD•0156 TD•0157 TD•0351 TD•0062 TD•0072 TD•0082 TD•0353 TD•0084 TD•0074 TD•0084 TD•0347

	Ⓢ																Plastic SO 8-14
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		●	●												●		Chip carrier
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