

I.F. LIMITING AMPLIFIER, FM DETECTOR AND AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDB1080 is a bipolar integrated circuit comprising a limiting amplifier, a balanced FM detector and a class-B audio amplifier. It is intended for frequencies up to 500 kHz with either narrow-band or wide-band FM. The circuit is especially suited for use in portophone sets, where a low supply voltage, a low supply current and a high sensitivity are of paramount importance.

QUICK REFERENCE DATA

Supply voltage range		
I.F. part	V_{CC1}	2,3 to 3,5 V
A.F. part	V_{CC2}	2,3 to 10 V
Supply current at $V_{CC1} = V_{CC2} = 2,5$ V, no signal	$I_{CC1} + I_{CC2}$	typ. 3 mA
Input voltage at onset of limiting	$V_{i1lim(rms)}$	typ. 30 μ V
AM rejection at $V_i = 1$ mV	k_{AMR}	typ. 50 dB
Open-loop voltage amplification of audio amplifier	A_{vd}	typ. 200
Output power of audio amplifier at $V_{CC2} = 9$ V	P_o	typ. 65 mW
Operating ambient temperature range	T_{amb}	-20 to + 70 °C

PACKAGE OUTLINES

TDB1080: 16-lead DIL; plastic (SOT38WBE).

TDB1080T: 16-lead mini-pack; plastic (SO16; SOT109A).



PINNING

1	V _{CC1}	positive supply, limiting amplifier
2	I1	limiting amplifier input
3	REF	reference input, limiting amplifier
4	BIAS	input biasing output
5	RCX1	external RC network
6	RCX2	external RC network
7	RCX3	external RC network
8	RCX4	external RC network
9	QD	FM detector output
10	I2-	out-of-phase input, audio amplifier
11	I2+	in-phase input, audio amplifier
12	CX	external capacitor
13	BS	bootstrap
14	V _{EE}	ground
15	QA	audio amplifier output
16	V _{CC2}	positive supply, audio amplifier

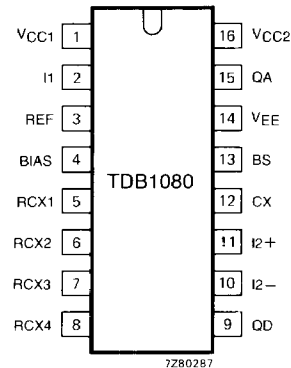


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TDB1080 consists of two parts that may be used independently, viz. a limiting i.f. amplifier with balanced FM detector, and a class-B audio amplifier.

Supply

The two parts of the circuit have a common-ground pin V_{EE} but separate supply pins V_{CC1} and V_{CC2}. The limiting amplifier and detector may be used with a supply voltage up to 3,5 V, the audio amplifier up to 10 V. The circuit is built to a large extent on the basis of long-tailed pairs with current sources in their tails. Thanks to the stabilizer diodes (D7, D8 and D9) the supply current of the audio amplifier varies little with the supply voltage. This permits the circuit to be used over a wide supply voltage range without an excessive battery drain as a result.

Limiting amplifier inputs I1 and REF and biasing output BIAS (pins 2, 3 and 4)

The limiting amplifier has differential inputs I1 and REF. I1 is intended to be used as an input; it should be biased externally by connecting it to the input biasing output BIAS via a resistor or an inductor. The reference input REF is biased internally; it should be decoupled by connecting a capacitor from REF to ground.

The onset of limiting is specified as the input voltage giving 3 dB gain reduction.

External RC network pins RCX1 to RCX4 (pins 4 to 8)

The TDB1080 contains a quadrature detector which requires an RC phase shifting network. This has to be connected to RCX1, RCX2, RCX3 and RCX4 as shown in Fig. 4. The component values have to be chosen in accordance with the i.f. centre frequency.

Audio amplifier inputs I2+ and I2- (pins 11 and 10)

The audio amplifier has differential inputs I2+ and I2- which are biased internally.

FUNCTIONAL DESCRIPTION (continued)

External capacitor pin CX (pin 12)

The internal biasing network for input I2 + should be decoupled by connecting an external capacitor between CX and ground.

Audio amplifier output QA and bootstrap pin BS (pins 15 and 13)

The audio amplifier has a class-B output stage. The maximum output voltage swing is obtained by connecting a capacitor between the bootstrap pin BS and the output QA and the load from BS to V_{CC2} (see Fig. 4).

The maximum output power varies from typ. 15 mW at $V_{CC2} = 2,5$ V to typ. 65 mW at $V_{CC2} = 9$ V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages, d.c.	V_{CC1}	max.	5 V
	V_{CC2}	max.	10 V
Supply current	$I_{CC1} + I_{CC2}$	max.	50 mA
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	—55 to + 125 °C	
Operating ambient temperature range	T_{amb}	—20 to + 70 °C	

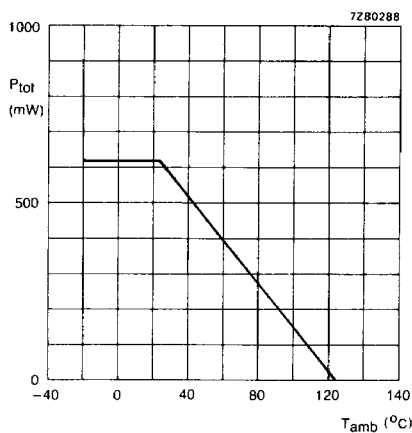


Fig. 3 Power derating curve.

CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2,5 \text{ V}$; $f_i = 95 \text{ kHz}$; $\Delta f = \pm 50 \text{ kHz}$; $f_m = 1 \text{ kHz}$; $T_{amb} = 25^\circ \text{C}$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies V_{CC1} and V_{CC2} (pins 1 and 16)					
Supply voltages	V_{CC1}	2,3	2,5	3,5	V
	V_{CC2}	2,3	2,5	10	V
Supply currents					
at $V_{CC1} = 2,5 \text{ V}$	I_{CC1}	—	1,5	2	mA
at $V_{CC2} = 2,5 \text{ V}$, no signal	I_{CC2}	—	1,5	2	mA
at $V_{CC2} = 9 \text{ V}$, no signal	I_{CC2}	—	3,5	—	mA
Limiting amplifier input I1 (pin 2)					
Input impedance	$ z_{id} $	15	—	—	$k\Omega$
Input voltage for onset of limiting (3 dB gain reduction)	$V_{I1lim(rms)}$	—	30	—	μV
Source impedance (between I1 and REF)	$ Z_S $	—	—	5	$k\Omega$
A.M. suppression					
at $\Delta f_i = 70 \text{ Hz}$; $f_m = 1 \text{ kHz}$; $m = 0,3$; $R_S = 50 \Omega$					
at $V_{I1(rms)} = 300 \mu\text{V}$	k_{AMR}	—	40	—	dB
at $V_{I1(rms)} = 1 \text{ mV}$	k_{AMR}	—	50	—	dB
at $V_{I1(rms)} = 10 \text{ mV}$	k_{AMR}	—	50	—	dB
$R_S = 5 k\Omega$					
at $V_{I1(rms)} = 300 \mu\text{V}$	k_{AMR}	—	30	—	dB
at $V_{I1(rms)} = 1 \text{ mV}$	k_{AMR}	—	40	—	dB
at $V_{I1(rms)} = 10 \text{ mV}$	k_{AMR}	—	50	—	dB
FM Detector output QD (pin 9)					
Output voltage at $d_{tot} = 0,5\%$; at $f_i = 95 \text{ kHz}$; $\Delta f = \pm 50 \text{ kHz}$	$V_{QD(rms)}$	100	—	—	mV
at $f_i = 250 \text{ kHz}$; $\Delta f = \pm 50 \text{ kHz}$	$V_{QD(rms)}$	100	—	—	mV
Signal-to-noise ratio					
at $f_i = 95 \text{ kHz}$; $\Delta f = \pm 50 \text{ kHz}$	S/N	70	—	—	dB
at $f_i = 250 \text{ kHz}$; $\Delta f = \pm 50 \text{ kHz}$	S/N	70	—	—	dB

The diagram illustrates a two-stage radio receiver circuit. The first stage is an **I.F. LIMITING AMPLIFIER AND FM DETECTOR**, which is a monolithic IC with pins for BIAS, RCX2, RCX3, RCX1, RCX4, VCC1, REF, VEE, and QD. It is powered by a +2.5V supply and has a 10μF capacitor connected to its BIAS pin. The input signal is coupled through a 0.22μF capacitor and a 50Ω resistor to the REF pin. The output of the QD pin is coupled to the input of the second stage, an **AUDIO AMPLIFIER**, through a 20kΩ resistor. The audio amplifier is a monolithic IC with pins for VCC2, BS, QA, CX, and 12. It is powered by a +2.5V to -9V supply (with RL = 15Ω) and has a 100μF capacitor connected to its VCC2 pin. The input of the audio amplifier is coupled through a 1μF capacitor and a 15nF capacitor to the BS pin. The output of the audio amplifier is coupled through a 1μF capacitor and a 470pF capacitor to the QA pin. The output of the QA pin is coupled through a 100μF capacitor and a 2.7Ω resistor to the load RL (24 to 600Ω, with VCC2 = 2.5V). The circuit also includes a 64μF capacitor connected to the +2.5V supply and a 10μF capacitor connected to the -9V supply.

Fig. 4 Test circuit and typical application of the TDB1080. For $f_i = 95$ kHz $R = 100$ k Ω and $C = 82$ pF, for $f_i = 250$ kHz $R = 33$ k Ω and $C = 47$ pF.