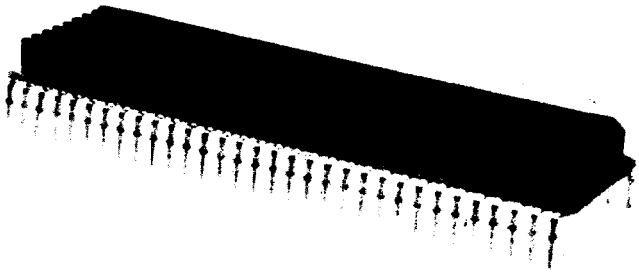
TRW

MULTIPLIER-ACCUMULATOR
PARALLEL 12 BIT

Model: TDC1003J

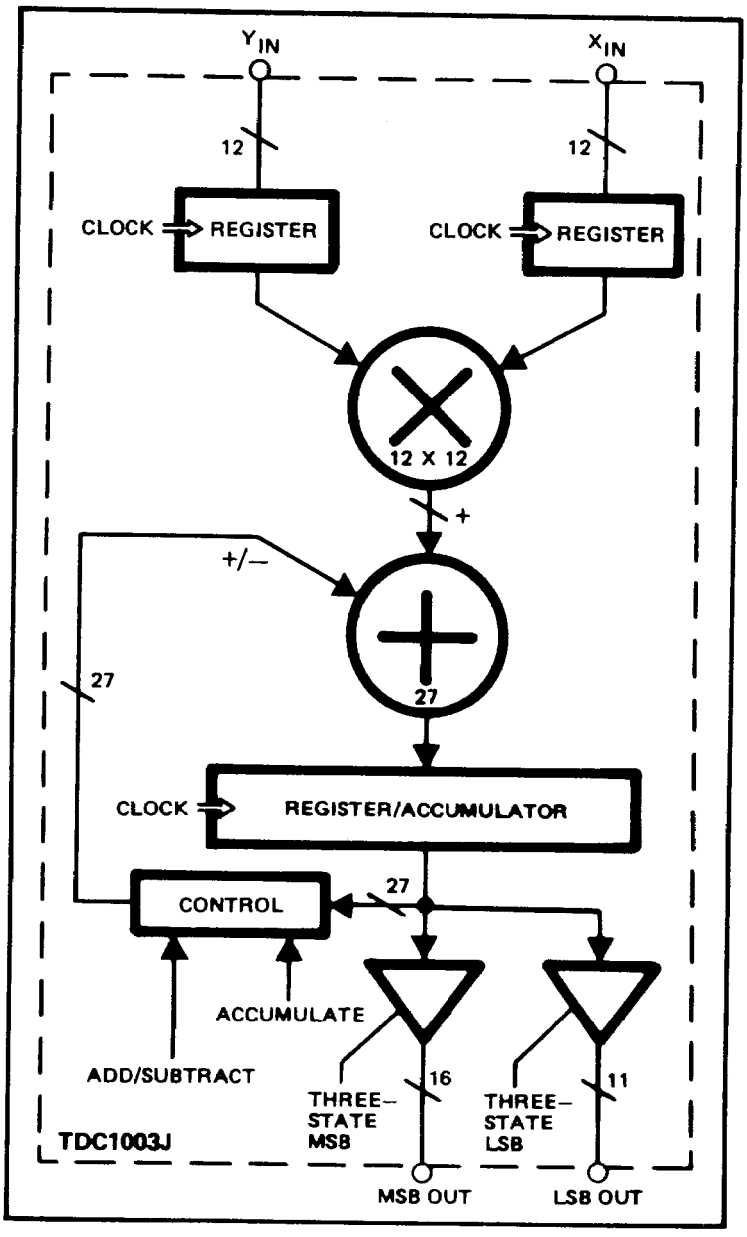


The TDC1003J is a multifunction arithmetic unit capable of performing 12 x 12 multiplication as well as product accumulation. It has an additional feature of permitting the accumulator contents to be subtracted from the next product instead of being added, if desired. Input registers are provided in addition to the product accumulation register.

The TDC1003J is directly implementable as the central building block for digital filters (particularly FFTs), complex multipliers, and recursive and nonrecursive filter elements.

FEATURES

- 12 x 12 bit parallel, two's complement multiplication
- Controllable accumulation either + or –
- 175 nsec typical multiply and accumulate time
- Much lower power/faster speed than equivalent MSI multiplication–accumulation systems
- Round control
- 27 bit accumulation capacity
- Single chip, bipolar technology
- Asynchronous mode multiply
- Radiation hard
- TTL input and output
- Three-state outputs
- Single power supply, +5 volts
- Dual in-line package or flatpack
- 2.5 watts power consumption



96 ORIG

004336

Y336 TRW

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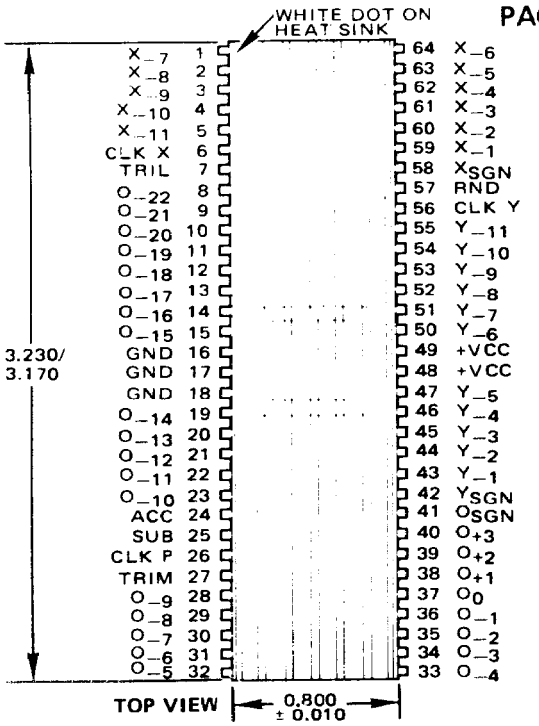
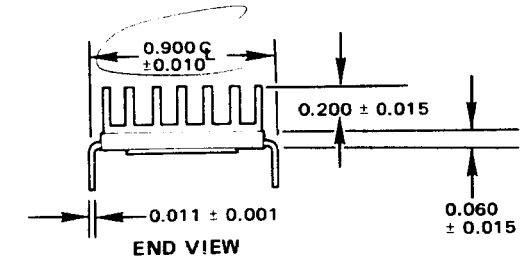
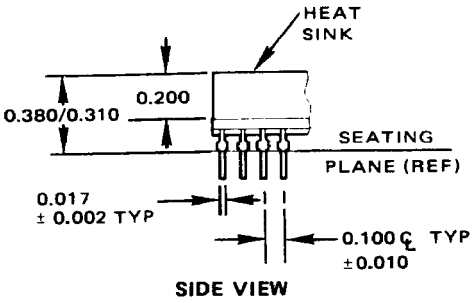
40G00273-a 2/82

PACKAGE INFORMATION



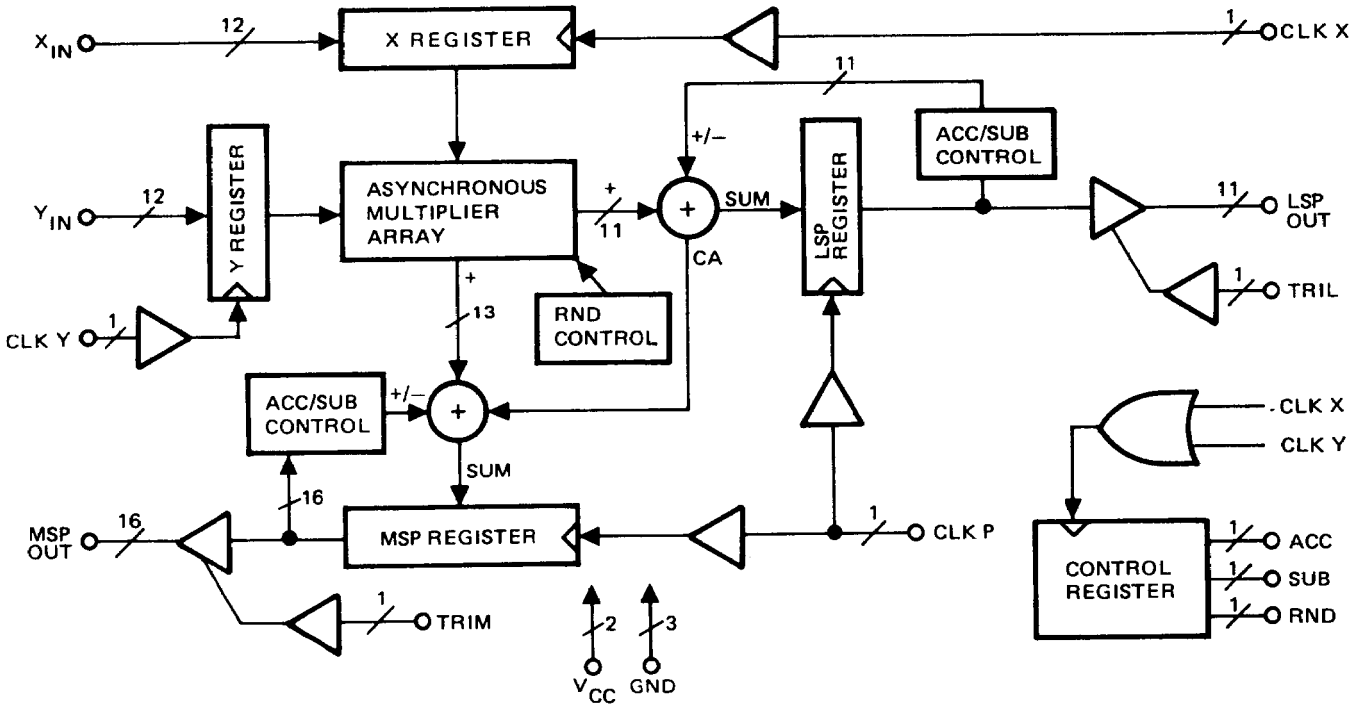




NOTES:

- DIMENSIONS IN INCHES
- ALL V_{CC} AND GND PINS MUST BE CONNECTED.

LOGICAL BLOCK



CONTROLS

CLKX, X_{IN} REGISTER CLOCK
CLKY, Y_{IN} REGISTER CLOCK
} REGISTER CLOCK FOR RND, ACC, AND SUB IS (CLK X + CLK Y)

CLK P, OUTPUT REGISTER CLOCK
TRIL, LSP THREE STATE CONTROL
TRIM, MSP THREE STATE CONTROL

RND, ADDS 2^{-12} TO PRODUCT (FRACTIONAL 2S COMPLEMENT FIELD)
ACC, ENABLES ACCUMULATOR MODE
SUB, CONTROLS ADDITION/SUBTRACTION OF ACCUMULATOR CONTENTS

absolute maximum ratings over operating temperature range

Supply voltage . . . . . -0.5 to 7.0 V
Input voltage . . . . . .0 to 5.5 V
Output voltage . . . . . 0 to 5.5 V
Operating temperature range . . . . . .0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C
Lead temperature (10 seconds) . . . . . 300°C
Junction temperature . . . . . 175°C

recommended operating conditions

	TDC1003			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5.0	5.5	V
Clock pulse width (measured at 1.5 V level)	25			ns
Input register setup time, τ_S (see Figure 1)	5			ns
Input register hold time, τ_H (see Figure 1)	15			ns
Operating ambient temperature	0		70	°C

electrical characteristics over recommended temperature range

PARAMETER		TEST CONDITIONS	TDC1003			UNIT
			MIN	TYP	MAX	
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
V_{OH}	High–level output voltage	V_{CC} = NOM, I_{OH} = –0.4 mA	2.4	2.7		V
V_{OL}	Low–level output voltage	V_{CC} = MIN, I_{OL} = 4.0 mA		0.3	0.5	V
I_{IH}	High–level input current	V_{CC} = MAX, V_{IH} = 2.4		–2	75	μA
I_{IL}	Low–level input current	V_{CC} = MAX, V_{IL} = 0.4		–5	–75	μA
I_{IN}	Clocks*	V_{CC} = MAX, V_{IH} = 2.4			75	μA
I_{IL}	Clocks*	V_{CC} = MAX, V_{IL} = 0.4			–0.75	mA
I_{CC}	Supply current	V_{CC} = NOM		500	750	mA

At $T_{ambient}$ = 25°C, V_{CC} = NOM. * Clock P is two equivalent clock input loads.

switching characteristics, V_{CC} = 5.0, T_A = 25°C (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multiply accumulate time, input register clock To output register clock, τ_{mA}	See Figure 5		175	200	ns
Output delay τ_D	Load 1, see Figures 3, 6		40	50	ns
Three state output delay					
Output enable	Load 2, see Figures 4, 6		40	50	ns
Output disable	Load 2, see Figures 4, 6		30	40	ns

12 X 12 BIT PARALLEL MULTIPLIER–ACCUMULATOR

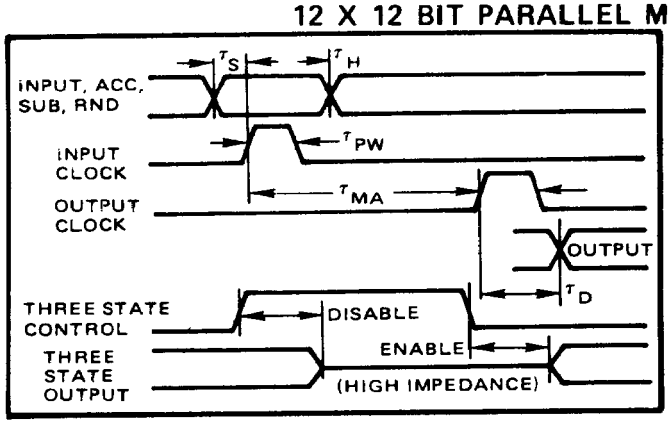


Figure 1. Timing Diagram

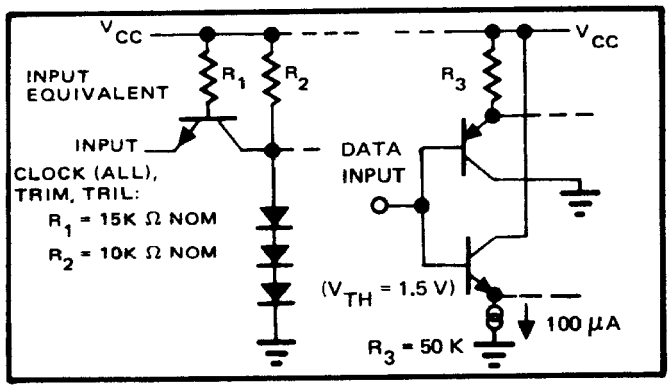


Figure 2. Input Schematics

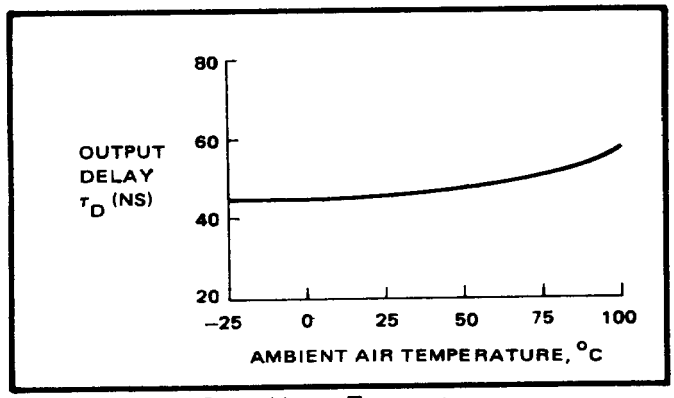


Figure 3. Output Delay Versus Temperature

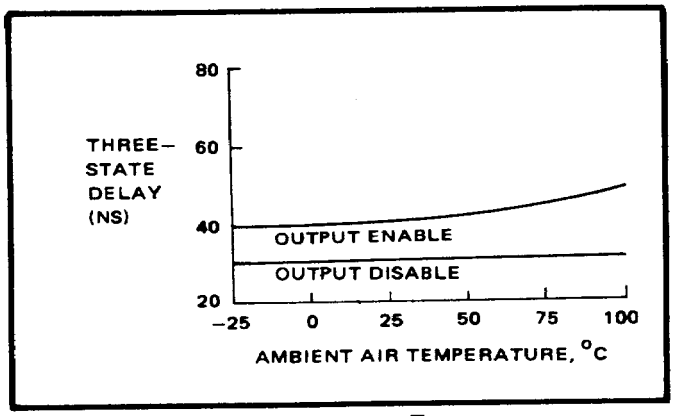


Figure 4. Three State Delay Versus Temperature

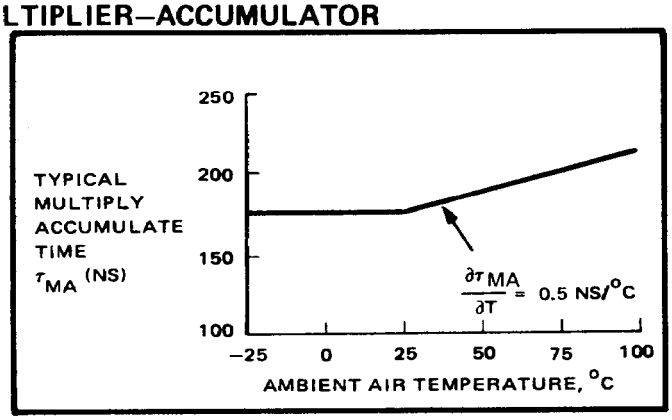


Figure 5. Multiply and Accumulate Time Versus Temperature

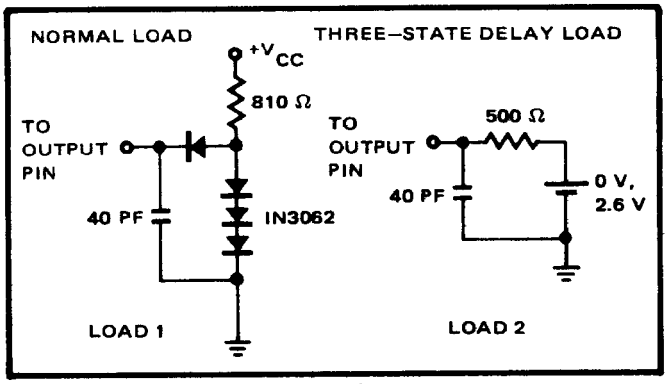


Figure 6. Test Loads for Delay Measurements

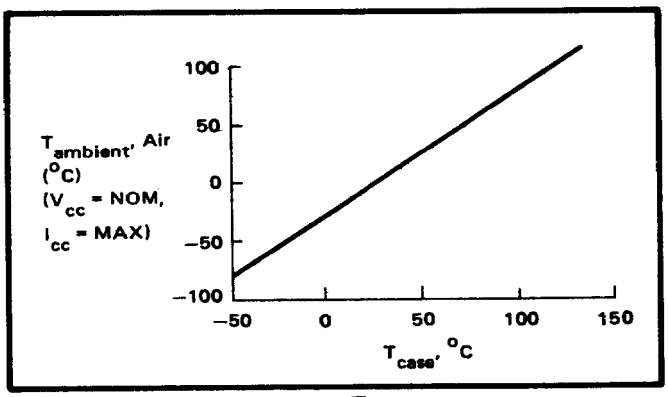


Figure 7. $T_{ambient}$, Air Versus T_{case}

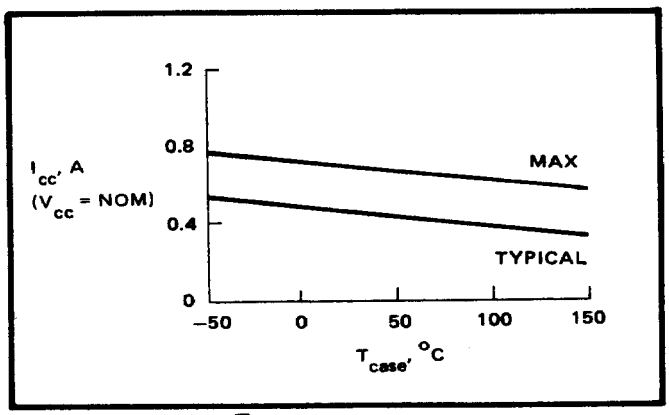


Figure 8. I_{cc} Versus T_{case}

CONTROLS DESCRIPTION: TDC1003J

ACC, SUB, and RND are loaded into registers by either CLKX or CLKY.

ACC: When the ACC signal is low, the next product clocked into the MSP and LSP accumulating registers has zero added to it, i.e., it is the first product in a series to be summed. The ACC signal is then brought high. Subsequent products are then accumulated in the product registers. If accumulation is not desired, the ACC is placed in the low position: the TDC1003J then functions as a standard multiplier.

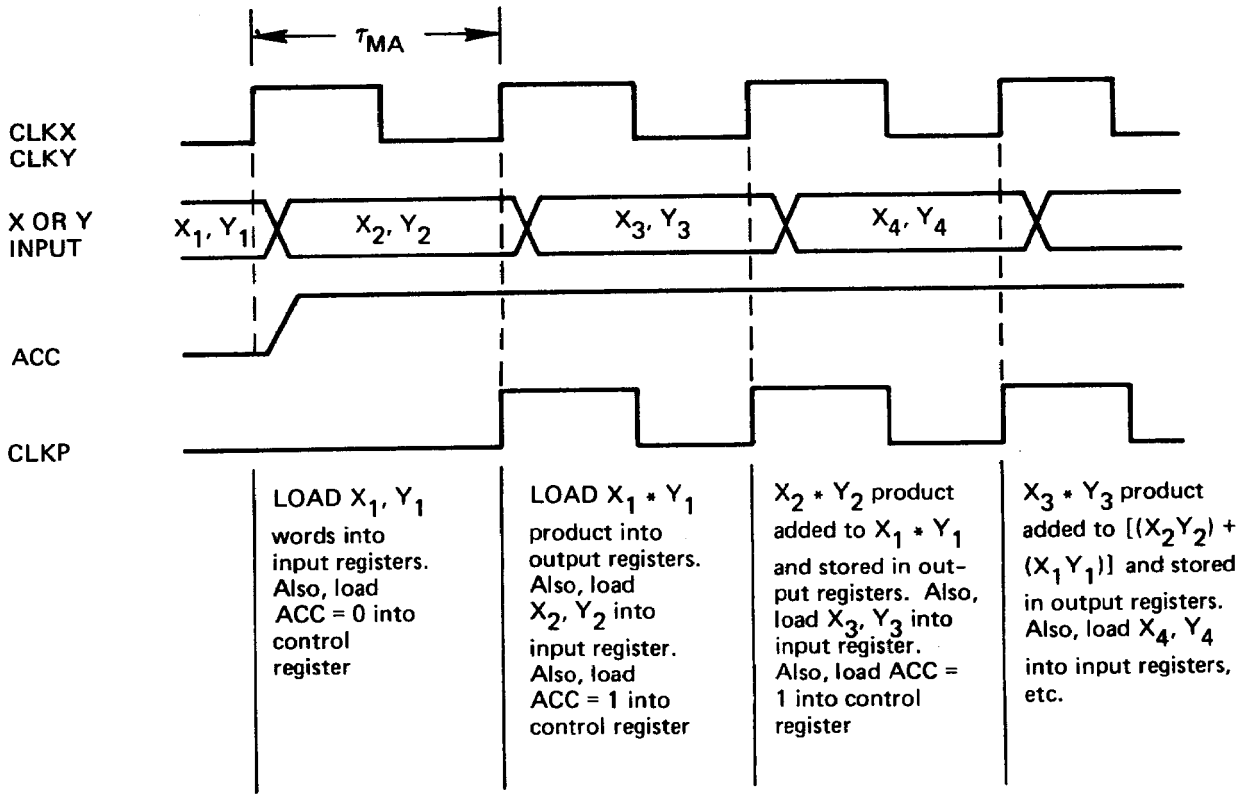
SUB: When the SUB signal is high, the accumulator contents are subtracted from the next product and the difference is then stored in the output registers. When low, the accumulator contents are added to the next product (straight accumulation). The SUB control is enabled by ACC. SUB' = (SUB * ACC).

RND: When RND is high, the quantity 2^{-12} (for fractional 2s complement field, see FORMAT page 6) is added to the next product.

TRIM, TRIL: Non-registered three state buffer controls: '0' = enable, '1' = disable.

TYPICAL OPERATING SEQUENCE

SUM OF PRODUCTS



NOTES:
1. SUB = 0 for sequence above.
2. X_n, Y_n are 12-Bit Two's Complement Numbers.

FORMAT: (NOTE 3) **2'S COMPLEMENT FRACTIONAL NOTATION**

X INPUT	X_{SGN}	X_{-1}	X_{-2}	X_{-3}	X_{-4}	X_{-5}	X_{-6}	X_{-7}	X_{-8}	X_{-9}	X_{-10}	X_{-11}
	SGN	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}
Y INPUT	Y_{SGN}	Y_{-1}	Y_{-2}	Y_{-3}	Y_{-4}	Y_{-5}	Y_{-6}	Y_{-7}	Y_{-8}	Y_{-9}	Y_{-10}	Y_{-11}

OUTPUT FORMAT WHEN NONACCUMULATING PRODUCTS (ACC = 0) FOR PINOUT DIAGRAM $O_n = PR_n$

PR SGN +4	PR SGN +3	PR SGN +2	PR SGN +1	PR 0	PR -1	PR -2	PR -3	PR -4	PR -5		PR -16	PR -17	PR -18	PR -19	PR -20	PR -21	PR -22
-2^4 SGN	2^3 SGN	2^2 SGN	2^1 SGN	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}		2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

NOTE 1

OUTPUT FORMAT WHEN ACCUMULATING PRODUCTS (ACC = 1) FOR PINOUT DIAGRAM $O_n = S_n$

SUM SGN +4	S +3	S +2	S +1	S 0	S -1	S -2	S -3	S -4	S -5		S -16	S -17	S -18	S -19	S -20	S -21	S -22
SGN -2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}		2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

NOTE 2

NOTE 1. When nonaccumulating, all four MSB will indicate the sign of the product. The PR-0 term will also indicate the sign except for the one exceptional case when multiplying $-1 * -1$. Note that, with the additional significant bits available on this multiplier, $-1 * -1$ is a valid operation yielding a +1 product.

NOTE 2. There is no change in the format whether one is accumulating the sum of products or simply doing single products. However, the three additional most significant bits are provided to allow valid summation beyond that available for a single multiplication product. For further clarification, no difference exists between this organization and one which would have the product accumulation off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position guarantees that the largest number field will be used. In operation the sign will be extended into the lesser significant bit positions when the accumulated sum only occupies a right-hand portion of the accumulator. As an example, when the sum only occupies the least three bit positions then the sign will be extended through the 24 most significant positions.

The latter factor allows one to detect imminent overflow/underflow should this be desired. Using an off-chip exclusive-OR gate connected to the sign and the next most significant bit will flag imminent overflow/underflow. When the two inputs are different, the exclusive-OR gate goes to a logic one state. In this case four more multiply-accumulate cycles would be allowable without overflow/underflow, but a fifth could possibly cause overflow/underflow depending upon the magnitude of the sum steps.

NOTE 3. Format is shown using a 2s complement fractional notation. In this notation the location of the binary point signifying separation of the integer and fractional fields is just after the sign, between the sign and the next most significant bit for the multiplier inputs. This scheme is carried over to the output format, except that an extended significance to the integer field is provided (to extend the utility of the accumulator). Consistent with the input notation the output binary point is located between the PR-0 and PR-1 bit positions (for the nonaccumulate mode). For the accumulate mode the binary point position is the same between the S+0 and S-1 bit positions.

It is arbitrary where the binary point is considered located as long as one is consistent with both input and output formats. One can consider the number field entirely integer, i.e., with the binary point just to the right of the least significant bit for input, product, and accumulated sum.

TYPICAL APPLICATIONS OF TDC1003J

DIGITAL FILTER FOR NUMERICAL INTEGRATION OF SAMPLED DATA

Based on the area under a parabolic arc, Simpson's rule is an accepted method for numerical integration of a sampled data sequence.

Let a function y(t) be sampled at n + 1 points, such that $y_0, y_1, \ldots, y_n$ are equally spaced at an incremental interval T. Assume that n is even. Then according to Simpson's rule (see almost any calculus textbook), the area A_S under the curve y(t), given by

$$A_S = \int_{t_1}^{t_1 + nT} y(t)dt, \qquad (1)$$

may be approximated by

$$A_S = \frac{T}{3}(y_0 + 4y_1 + 2y_2 + 4y_3 + 2y_4 + \ldots + 4y_{n-1} + y_n). \qquad (2)$$

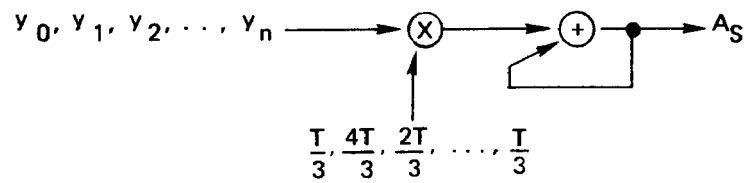
This is generally more accurate than the so-called trapezoidal rule

$$A_T = \frac{T}{2}(y_0 + 2y_1 + 2y_2 + \ldots + 2y_{n-1} + y_n), \qquad (3)$$

which approximates the function y(t) by straight-line segments and therefore fails to take account of curvature.

An accumulation of the terms in Equation (2), therefore, implements Simpson's rule explicitly, where it is necessary only to input the sequence of sampled points and the appropriate sequence of weighing coefficients. After any step m, where m<n, the contents of the accumulator are $\tilde{A}_m$, which is an approximation to the running integral up to that point. When m = n and the accumulation is terminated with the proper weighting coefficient (see Note), the evaluation is complete and $\tilde{A}_n = A_S$.

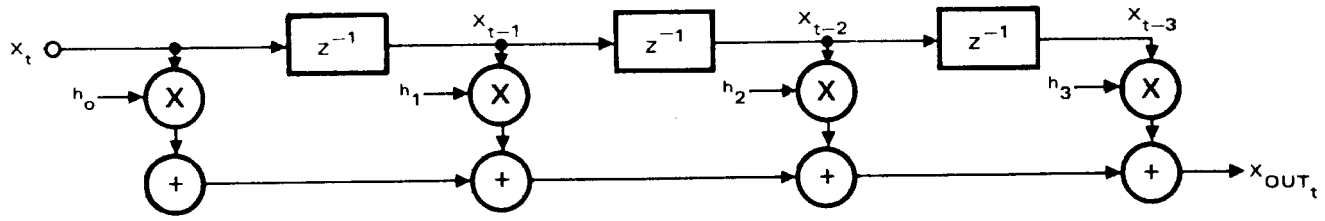
BLOCK DIAGRAM (Uses one TDC 1003J)



Operation Sequence					Contents of Output Registers At End of Operation	Cumulative Time at Completion of Operation (ns)
Step	Load	ACC	SUB	RND		
1	$y_0, \frac{T}{3}$	0	0	0	$y_0 * \frac{T}{3} = \tilde{A}_1$	200
2	$y_1, \frac{4T}{3}$	1	0	0	$\tilde{A}_1 + y_1 * \frac{4T}{3} = \tilde{A}_2$	400
3	$y_2, \frac{2T}{3}$	1	0	0	$\tilde{A}_2 + y_2 * \frac{2T}{3} = \tilde{A}_3$	600
4	$y_3, \frac{4T}{3}$	1	0	0	$\tilde{A}_3 + y_3 * \frac{4T}{3} = \tilde{A}_4$	800

NOTE: To avoid termination error, based on Simpson's rule outlined above, the integration should terminate on an odd number of samples (n even) with a weight of T/3, as shown. If it is necessary to terminate on an even number of samples (n odd), then it is a good approximation to keep the sequence up to that point and terminate with a weight of 2T/3.

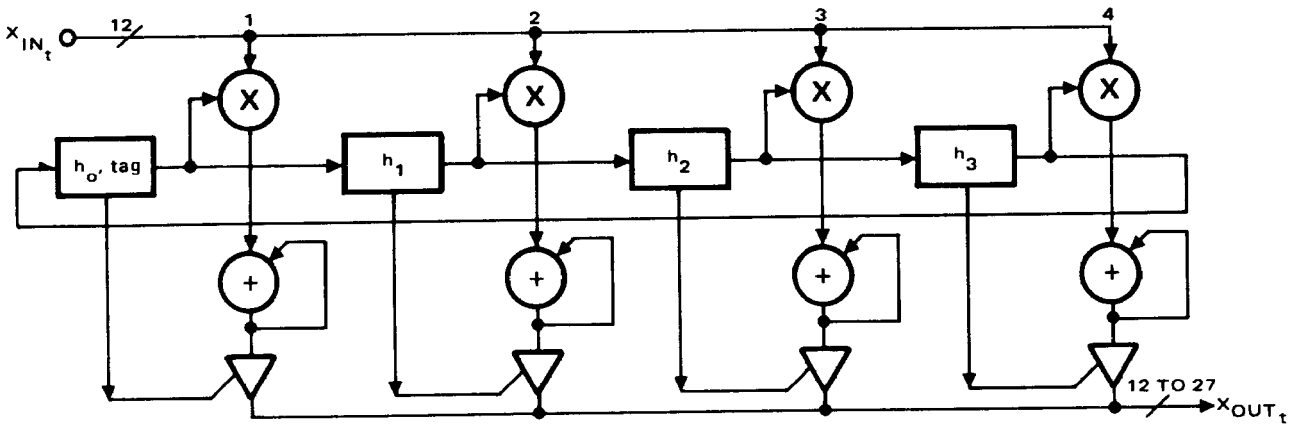
NONRECURSIVE FILTER



Using one TDC1003J in time sequenced operation.

Operation Sequence					Contents of Output Registers at Completion of Operation	Cumulative Time At Completion of Operation (ns)
Step	Load	ACC	SUB	RND		
1	X_t, h_0	0	0	0	$X_t * h_0$	200
2	X_{t-1}, h_1	1	0	0	$X_t * h_0 + X_{t-1} * h_1$	400
3	X_{t-2}, h_2	1	0	0	$X_t * h_0 + X_{t-1} * h_1 + X_{t-2} * h_2$	600
4	X_{t-3}, h_3	1	0	0	$X_t * h_0 + X_{t-1} * h_1 + X_{t-2} * h_2 + X_{t-3} * h_3 = X_{OUT_t}$	800 cycle complete
5	X_{t+1}, h_0	0	0	0	$X_{t+1} * h_0$	1000
6	X_t, h_1	1	0	0	$X_{t+1} * h_0 + X_t * h_1$	1200
7	X_{t-1}, h_2	1	0	0	$X_{t+1} * h_0 + X_t * h_1 + X_{t-1} * h_2$	1400
8	X_{t-2}, h_3	1	0	0	$X_{t+1} * h_0 + X_t * h_1 + X_{t-1} * h_2 + X_{t-2} * h_3 = X_{OUT_{t+1}}$	1600 cycle complete

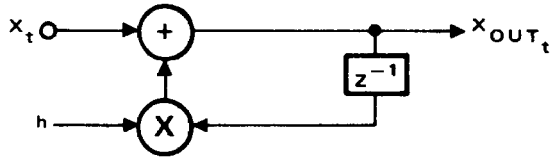
PIPELINED NONRECURSIVE FILTER USING FOUR TDC1003J, 5 MHz



In this method, four TDC1003J parts are used in a parallel-out kind of connection. An external four-stage circulating shift register holds the weighting functions, h. A tag bit is also circulated in the h shift registers which operates the 3-state control, thereby busing the accumulator contents to the output in sequence. Input register clocking, output register clocking and h shift register are all operated directly from the 5 MHz system clock. The control ACC is also operated from the tag bit as well as the 3-state control. As can be traced from the block diagram, each TDC1003J accumulates four products and then is gated to the output bus. On the next clock period the adjacent TDC1003J is outputted, etc. By these means, steady outputs at the 5 MHz rate are sustained. The latency period is four clock periods or 800 ns. The internal operation sequence for any one TDC1003J is the same as shown in the previous implementation.

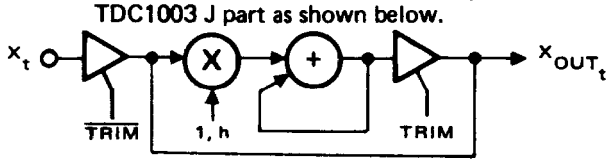
RECURSIVE DIGITAL FILTER IMPLEMENTED WITH TDC1003

The usual block diagram for the simplest recursive digital filter is shown below.



SIMPLE RECURSIVE FILTER

This can be implemented with a single TDC1003 J part as shown below.

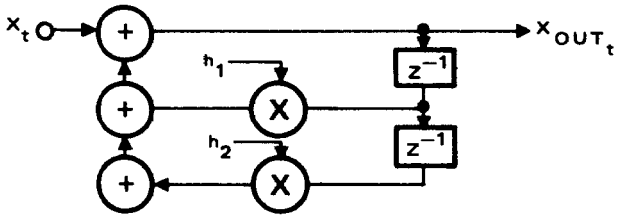


SINGLE TDC1003 J PART IMPLEMENTATION OF SINGLE POLE FILTER

In this case, two-step operation is used where the operand into the multiplier is alternated between 1 and h and the output is read out on alternate clock cycles. Operation is shown below, assuming initial output accumulator contents of value υ.

Operation Sequence						Contents of Output Registers at Completion of Operation	Cumulative Time of Completion of Operation
Step	Load	ACC	SUB	RND	TRIM		
	Initial state t_0					$X_{OUT_{t_0}} = \upsilon$	0
1	$X_{OUT_{t_0}}$, h	1	0	0	0	$h\upsilon$	200
2	X_{t+1}, 1	1	0	0	1	$X_{OUT_{t+1}} = X_{t+1} + h\upsilon$ (read out to destination)	400 Cycle complete
3	$X_{OUT_{t+1}}$, h	1	0	0	0	$h(X_{t+1} + h\upsilon)$	600
4	X_{t+2}, 1	1	0	0	1	$X_{OUT_{t+2}} = X_{t+2} + h(X_{t+1} + h\upsilon$ (read out to destination)	800 Cycle complete

For a two or more pole filter we have the following diagram:



$$X_{OUT_{t_0}} = \upsilon$$

$$X_{OUT_{t+1}} = X_{t+1} + h_1\upsilon$$

$$X_{OUT_{t+2}} = X_{t+2} + h_1 (X_{t+1} + h_1\upsilon) + h_2\upsilon$$

$$X_{OUT_{t+3}} = X_{t+3} + h_1 [X_{t+2} + h_1 (X_{t+1} + h_1\upsilon) + h_2\upsilon] + h_2 (X_{t+1} + h_1\upsilon)$$

$$X_{OUT_{t+4}} = X_{t+4} + h_1 X_{t+3} + h_1 [X_{t+2} + h_1 (X_{t+1} + h_1\upsilon) + h_2\upsilon] + h_2 (X_{t+1} + h_1\upsilon) + h_2 [X_{t+2} + h_1 (X_{t+1} + h_1\upsilon) + h_2\upsilon]$$

In general

$$X_{OUT_t} = X_t + h_1 (X_{OUT_{t-1}}) + h_2 (X_{OUT_{t-2}}) + \ldots h_n (X_{OUT_{t-n}})$$

$$X_{OUT_t} = X_t + \sum_{i=1}^{n} h_i (X_{OUT_{t-i}})$$

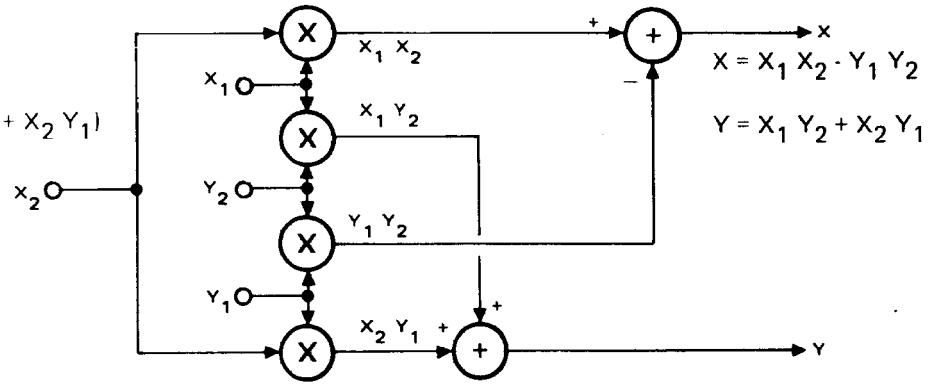
Using the methods shown for the other example, the two pole filter can be stepped at 600 ns intervals using one TDC1003.

COMPLEX MULTIPLICATION

$Z = (X_1 + j\,Y_1) * (X_2 + j\,Y_2)$

$= X_1 X_2 - Y_1 Y_2 + j\,(X_1 Y_2 + X_2 Y_1)$

$= X + j\,Y$



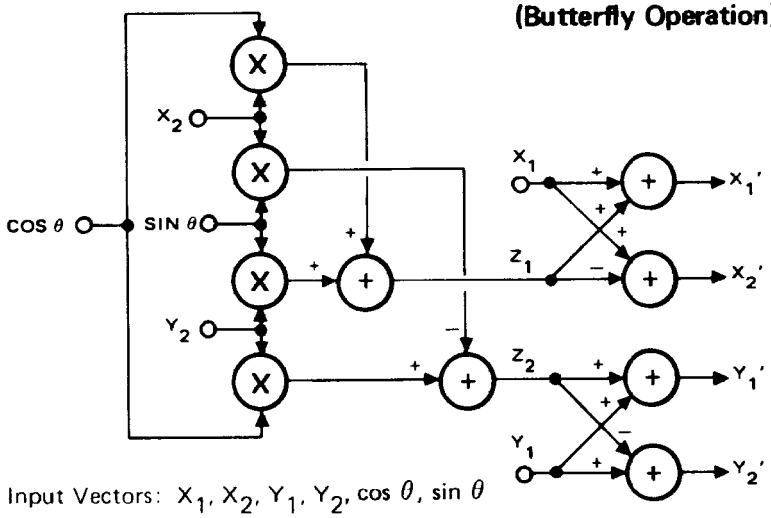
Using one TDC1003J in time sequenced operation.

Operation Sequence					Contents of Output Registers at Completion of Operation	Cumulative Time at Completion of Operation (ns)
Step	Load	ACC	SUB	RND		
1	Y_1, Y_2	0	0	0	$Y_1 * Y_2$	200
2	X_1, X_2	1	1	0	$X_1 * X_2 - Y_1 * Y_2 = X$ (transfer to destination)	400
3	X_1, Y_2	0	0	0	$X_1 * Y_2$	600
4	X_2, Y_1	1	0	0	$X_1 * Y_2 + X_2 * Y_1 = Y$ (transfer to destination)	800

Using two TDC1003s, it is obvious that the above complex multiplication can be performed in 400 nsec.

FFT DECIMATION-IN-TIME KERNEL SEQUENCE

(Butterfly Operation)



Input Vectors: $X_1, X_2, Y_1, Y_2, \cos\theta, \sin\theta$

Principal Equations:

$$F_K = \sum_{n=0}^{N-1} f_n W^{nK},\ K = 0, 1, 2, \ldots N-1,$$

$$W \equiv e^{-j2\pi/N}$$

$$W^K \equiv e^{-j2\pi K/N} = e^{-j\theta} = \cos\theta - j\sin\theta$$

Implementation Solution:

$X_1' = X_1 + X_2\cos\theta + Y_2\sin\theta = X_1 + Z_1$

$Y_1' = Y_1 - X_2\sin\theta + Y_2\cos\theta = Y_1 + Z_2$

$X_2' = X_1 - X_2\cos\theta - Y_2\sin\theta = X_1 - Z_1$

$Y_2' = Y_1 + X_2\sin\theta - Y_2\cos\theta = Y_1 - Z_2$

FFT points represented by

$X_1 + j\,Y_1,\ X_2 + j\,Y_2$

Transformed Vectors

X_1', X_2', Y_1', Y_2'

$\theta \equiv 2\pi K/N$

$Z_1 \equiv X_2\cos\theta + Y_2\sin\theta$

$Z_2 \equiv -X_2\sin\theta + Y_2\cos\theta$

FFT DECIMATION-IN-TIME KERNEL SEQUENCE (CONTINUED)

Using one TDC1033J in time sequence operation.

Operation Sequence					Contents of Output Registers at Completion of Operation (Note 1)	Cumulative Time at Completion of Operation (ns) (Note 3)
Step	Load/Hold (L/H)	ACC	SUB	RND		
1	L X_2, $\cos\theta$	0	0	0	$X_2 \cos\theta$	200
2	L Y_2, $\sin\theta$	1	0	0	$X_2 \cos\theta + Y_2 \sin\theta = Z_1$	400
3	L X_1, 1(Note 4)	1	0	0	$X_1 + Z_1 = X_1'$ (transfer to destination)	600
4	H X_1, 1(Note 2)	1	1	0	$-Z_1$	800
5	H X_1, 1	1	0	0	$X_1 - Z_1 = X_2'$ (transfer to destination)	1000
6	L X_2, $\sin\theta$	0	0	0	$X_2 \sin\theta$	1200
7	L Y_2, $\cos\theta$	1	1	0	$-X_2 \sin\theta + Y_2 \cos\theta = Z_2$	1400
8	L Y_1, 1	1	0	0	$Y_1 + Z_2 = Y_1'$ (transfer to destination)	1600
9	H Y_1, 1	1	1	0	$-Z_2$	1800
10	H Y_1, 1	1	0	0	$Y_1 - Z_2 = Y_2'$ (transfer to destination)	2000

Note 1. The outputs are stable within τ_D time after clocking the output registers, typically 30 ns. Outputs are held stable until the next step in the sequence is clocked at the end of the step. Consequently output contents are available to bus to the destination for $\tau_m - \tau_D$ period, approximately 170 ns for τ_m = 200 ns.

Note 2. At steps 4 and 9, if the constant loaded is +2 instead of +1, the above sequence can be shortened by two steps or to 1600 ns. Some loss in accuracy may result using this shortened sequence since the number field would have to include +2 and a quantity such as $\cos\theta$ could only be represented with one less significant binary bit.

Note 3. Using two TDC1003J parts instead of one will allow the kernel operation in one-half the time given above.

Note 4. The absence of a true +1 in the fractional 2s complement number field causes a small error to be introduced. An alternative is to arrange the algorithm so that -1 is used as the operator since this is a valid 2s complement number having unity absolute value. Another alternative which avoids the error is to use a one bit integer field with $\sin\theta$ and $\cos\theta$ scaled accordingly.