



TDE1707DF

Intelligent power switch

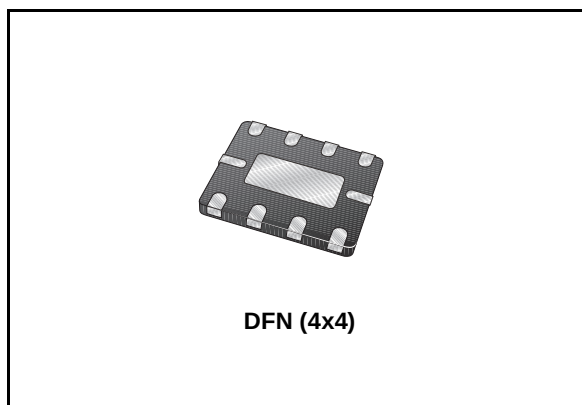
Features

- 0.5A Output current
- Low side or high side switch configuration
- 6V to 48V supply voltage range
- Overload and short circuit protections
- Internal voltage clamping
- Supply and output reversal protection
- Thermal shutdown
- GND and V_S open wire protection
- Adjustable delay at switch on
- Indicator status LED driver
- +5V regulated AUX. voltage
- High burst immunity

Description

The TDE1707DF is a 0.5A Integrated Power Switch with up to 48V Power supply capability. Two output configurations are possible:

- Load to Gnd. (High Side Mode)
- Load to V_S (Low side Mode)



Especially dedicated to proximity detectors, its internal +5V supply can be used to supply external circuits (See also AN495/0692). A signal is internally generated to block the In signal, and prevent activation of the output switch, as long as an abnormal condition is detected. The power-on transition, as well as the chip over temperature and the output overcurrent, concur to the generation of such signal. A minimum delay of 25ms (Typ.value) is added to the trailing edge of such signal to ensure that a stable normal situation is present when the signal disappears. The delay (of the disappearance of the block signal; no delay at its on set) can be further increased connecting a capacitor between pin3 and ground. It can drive resistive or inductive loads..

Order codes

Part number	Temp range, °C	Package	Packing
TDE1707DF	-25°C to +85°C	DFN(4x4)	Tube
TDE1707DFT	-25°C to +85°C	DFN(4x4)	Tape & Reel

Contents

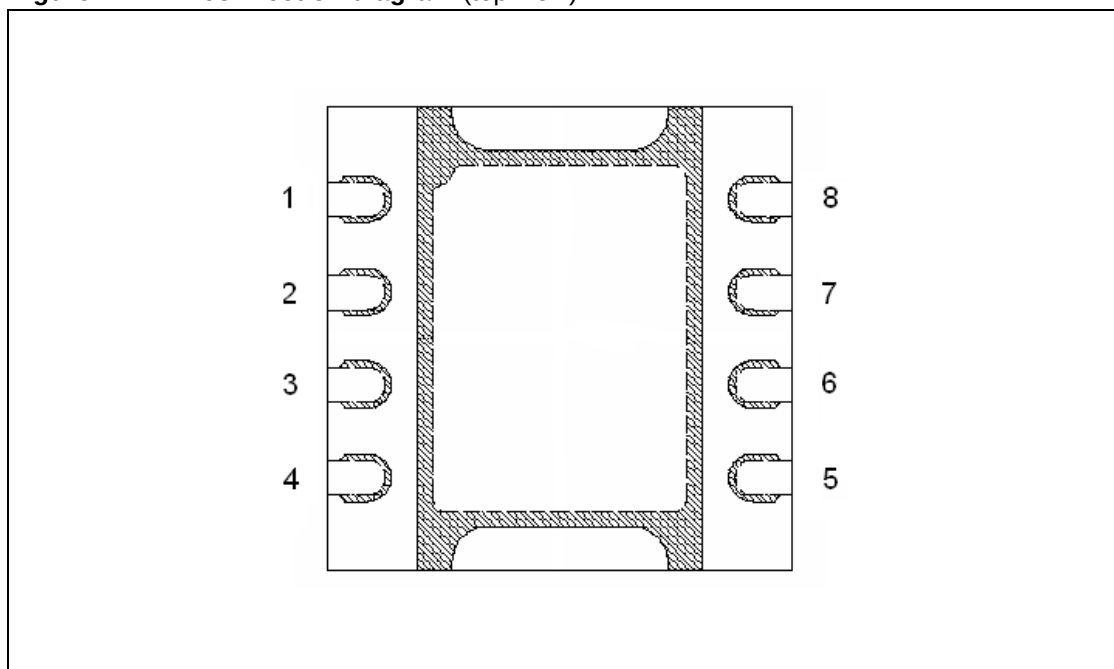
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The schematic diagram illustrates the internal circuitry of the LED driver. It includes a VREG +5V supply, an IN pin, a DELAY pin, and a +Vs supply. The circuit features several operational amplifiers, a 5V battery, a 1MΩ resistor (R1), a 2.4V battery, a 4V battery, a 5V battery, a 70V diode, a THERMAL SHUTDOWN block, and an LED DRIVER block. The circuit is designed to drive an LED and provide L.S. OUT and H.S. OUT signals.

Table 1. Pin Functions

Pin No	Function
1	Led Driver
2	High Side Output
3	Delay Capacitance Source
4	Ground
5	Input
6	Reg. Voltage Source
7	Supply Voltage
8	Low Side Output

Note: Lead frame can be connected to ground.

Figure 2. Pin connection diagram (top view)

2 Electrical specifications

2.1 Thermal data

Table 2. Thermal data

Symbol	Description	Value	Unit
R_{thJA}	Thermal Resistance Junction-ambient Max.	32 ⁽¹⁾	°C/W
R_{thJC}	Thermal Resistance Junction-case Max.	1.2	°C/W

1. Soldered to a 4 layer board with 4 vias in the pad.

2.2 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	50	V
V_S	Supply Reverse Voltage	50	V
I_o	Output Current	internally limited	
V_{reg}	Regulated Voltage Pin	0 to 7	V
V_{delay}	Delay Cap. Surce Pin	0 to 5	V
V_o	Output Diff. Voltage	55	V
V_i	Input Voltage	-10 to 50	V
T_j	Operating Temperature Range	-25 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C
P_{tot}	Power Dissipation	internally limited	mW
E_i	Energy Induct. Load	100	mJ

2.3 Electrical characteristics

Table 4. Electrical Characteristics

($V_S = 24V$; $T_j = -25$ to $+85^\circ\text{C}$ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S 7	Supply Voltage		6		48	V
I_{sr} 7	Supply Reverse Current	$V_{SR} = -48V$			1.5	mA
I_q 7	Quiescent Current	$I_{reg} = I_{led} = 0$; $V_i < 2V$; $V_S = 6$ to $48V$			1.5	mA
I_o 8/2	Output Current	$V_S = 6V$ to $32V$			500	mA
		$V_S = 32V$ to $48V$			300	mA

Table 4. Electrical Characteristics (continued)
($V_S = 24V$; $T_J = -25$ to $+85^\circ C$ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{sat} 8/2	Output Voltage Drop V_{8-2}	$I_O = 500mA$		1.1	1.6	V
I_{sc} 8/2	Short Circuit Current		0.7		1.5	A
V_{cl} 8/2	Internal Voltage Clamp	$I_{CL} = 10mA$	55		70	V
I_{olk} 8/2	Output Leakage	(Pin 2) $V_i < 2V$; $V_O = 0$ to V_S (Pin 8)		100	300 100	μA μA
V_{ith} 5	Input Voltage Threshold		2		3	V
V_{ihis} 5	Input Threshold Hysteresis			300		mV
I_{lk} 5	Input Current	$V_i = 5V$		2	5	μA
V_{reg} 6	Regulated Output Voltage	$I_{reg} < 5mA$	4.5	5	5.5	V
I_{scr} 6	Short Circuit Regulated		6	30	50	mA
I_{reg} 6	Output Regulator Current	$V_S = 35V$ $V_S = 48V$			6 4	mA mA
I_{old} 1	Current Surce Sink Led Driver	Output ON ($\pm$)	2	3	4	mA
V_{old} 1	Voltage Drop Led Driver	$I_{os} = 2mA (\pm)$		1.2	1.6	V
I_{oldk} 1	Lead Driver (off) Leak.	$V_i < 2V$; $R_L < 1K\Omega$			10	μA
I_{dch} 3	Del. Cap. Charge Current	$T_J = 25^\circ C$	2	4	6	μA
V_{dth} 3	Delay Voltage Trigger			4		V

2.4 Dynamic information

Table 5. Dynamic information
($V_S = 24V$; $T_J = 25^\circ C$; $R_L = 48\Omega$).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}	Propagation Turn on Time	$V_i = 0$ to $5V$		15		μs
t_{off}	Propagation Turn off Time			15		μs
t_{don}	Delayed Turn on Time / nF Delay Capacitor		0.65	1	2	ms
$t_{d min}$	Minimum Delayed t_{on} Delay Capacitor = 0			25		μs

3 Application Information

The LED driver tells the output status. It can source or sink current ($I_{old\ typ} = 3mA$), according to the output configuration chosen. The thresholds, represented by the output comparator in the Block Diagram, are set at about 1.5V - 2V.

For instance, in the High Side Load case of the Application Circuit, when the voltage on pin 8 (the output) differs from V_{CC} less than 1.5V, the output is sensed in "OFF" state and the LED driver is disabled.

If instead pin 8 differs from V_{CC} more than 3V (the output comparator threshold value plus the drop voltage on the LED), then the output is sensed "ON" and the driver will force the current on the LED.

Figure 3. Low side driver topology

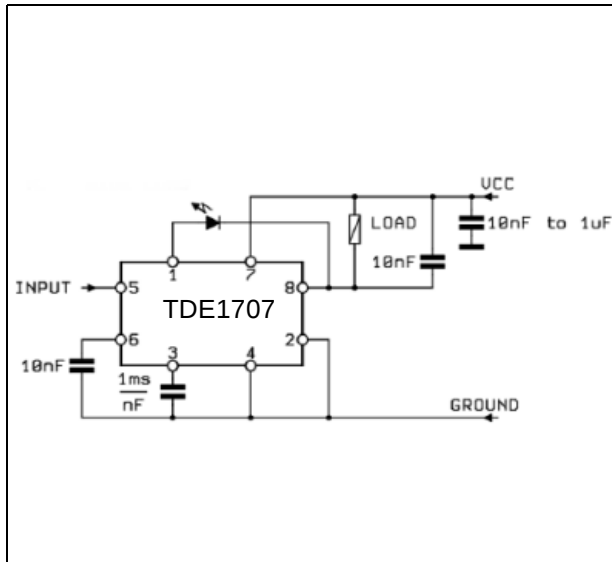
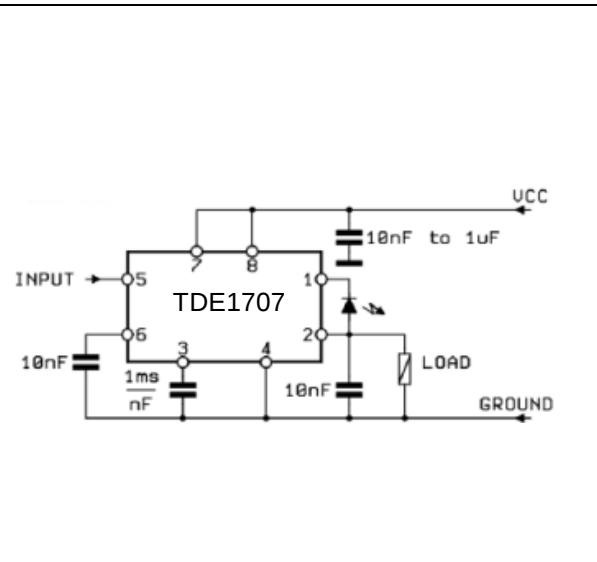


Figure 4. High side driver topology



3.1 Adjustable input hysteresis circuit

The TDE1708 is a device realized in bipolar technology and therefore it has the usual problems of temperature compensation that such technology involves; despite all it maintains an input dynamics within 1V over industrial temperatures range.

In all input voltage range it will guarantee a high impedance of 1Mohm determining an input current about 2uA.

Exploiting this input high impedance is possible connects a sensor directly on it and bypass the obstacle of active signal conditioning circuit using a voltage firm point as ground of sensor, the delay capacitor, connected on the pin 3, as low pass filter and capacitor on Vreg pin to minimize the noise on it and protect for errors the low-voltage internal circuits, according AN495.

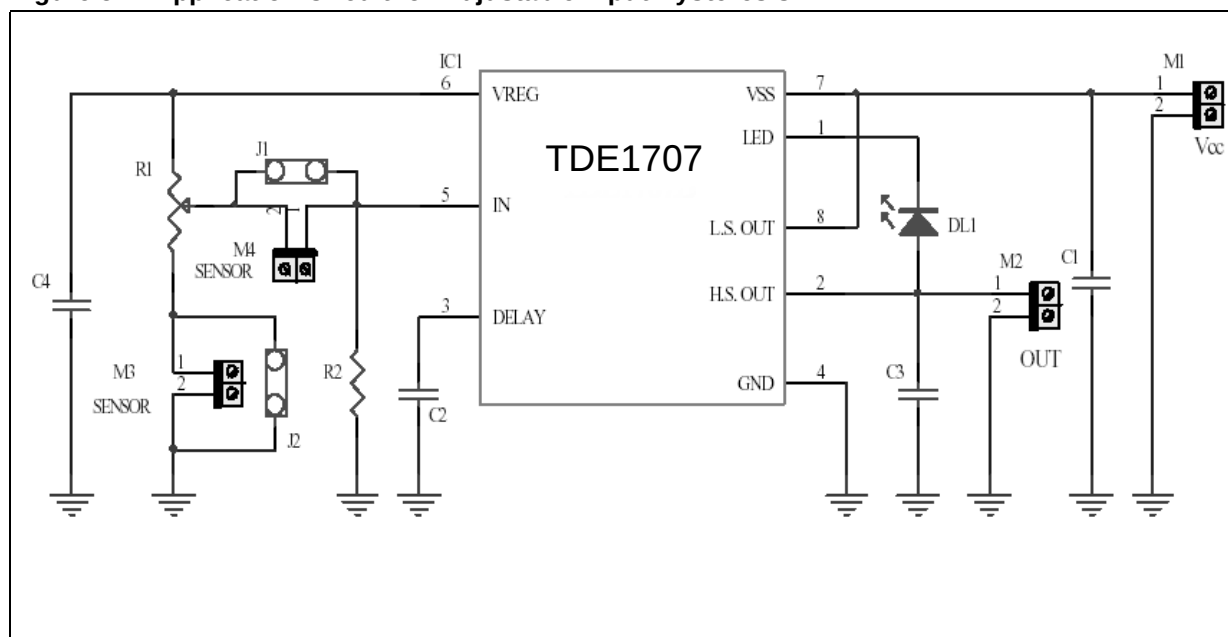
In [Figure 5](#), the input external network is optimized for accepting both a sensor with ground connected to the body and a sensor with independent ground.

In order to ground the body of the sensor, J1 has to be shorted, while J2 opened and connect the sensor on M3; in case of independent ground J1 must be opened, J2 shorted and the sensor connected on M4.

DL1 indicate commutation status of the device output and C3 realize a simple output filtering in case is used an inductive load. With C2 about 10nF we obtain a good filtering and immunity from input voltage noise. C4 is 4,7nF according AN495.

R2 is an optional resistor plugged only when the sensor needs to adapt its impedance with the input impedance of device.

Figure 5. Application Circuit for Adjustable Input Hysteresis



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 6. DFN (4x4) Mechanical data & package dimensions

Ref.	Dimensions		
	Millimeters		
	Typ	Min	Max
A	0.90	0.80	1
A1	0.02	0	0.05
A3	0.20		
b	0.30	0.23	0.38
D	4	3.90	4.10
D2	3	2.82	3.23
E	4	3.90	4.10
E2	2.20		2.30
e	0.80		
L	0.50	0.40	0.60

Figure 6. Package dimension

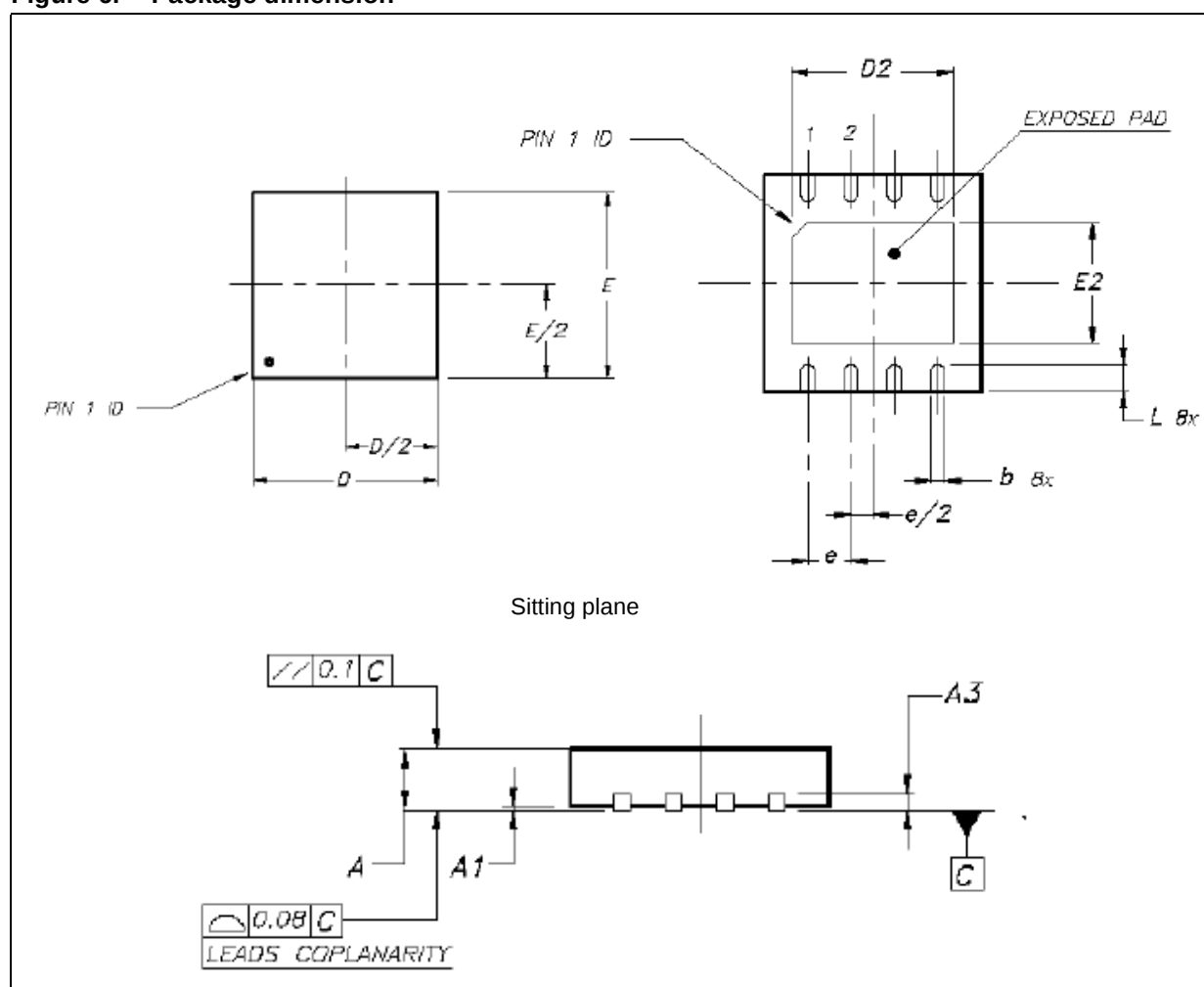
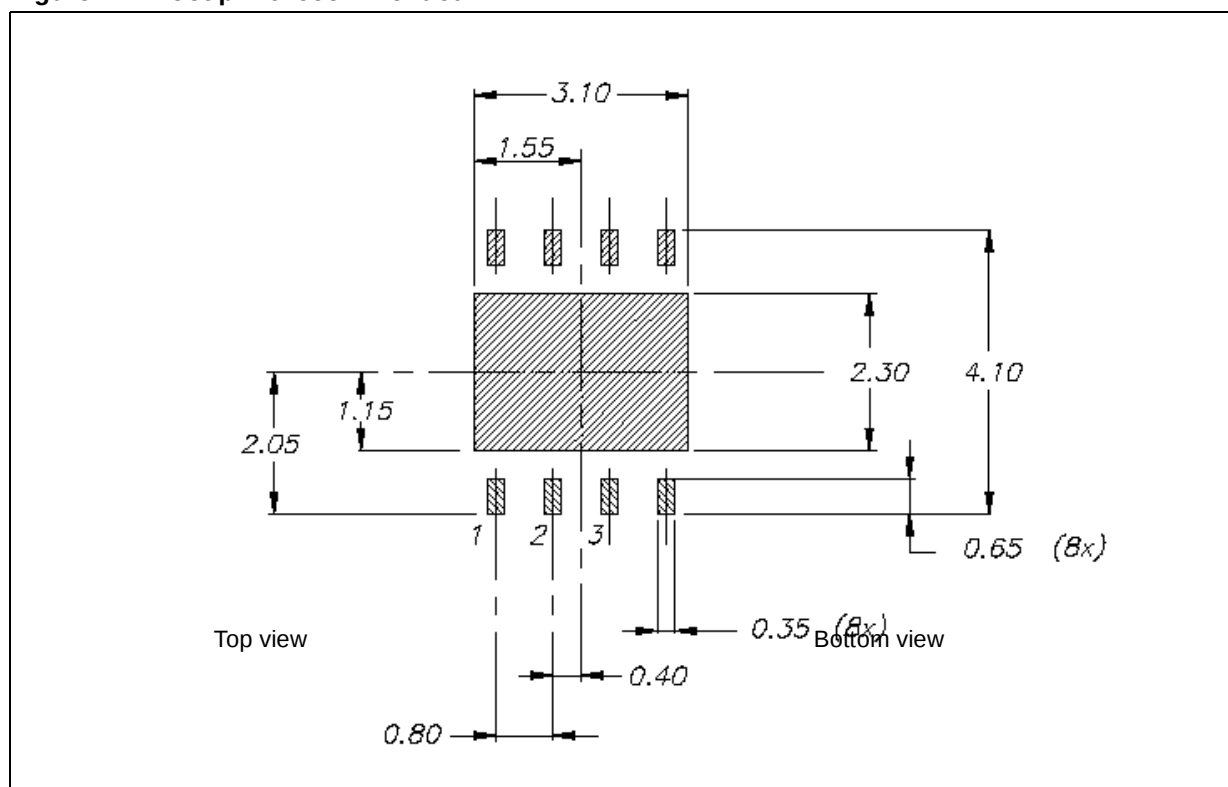


Figure 7. Foot print recommended



5 Revision history

Table 7. Revision history

Date	Revision	Changes
06-Apr-2006	1	Initial release.

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