

UHF Transparent Data Link transceiver

The TDL2 is a 9600 baud half-duplex OEM radio modem in BiM2 footprint, operating on European 433MHz ISM band. TDL2 acts as a transparent serial cable to attached host. TDL2 is an intermediate level OEM radio modem which is in between a raw FM radio module like BiM2 and a sophisticated OEM radio modem like SPM2. It takes care of preamble, synchronisation, bit balancing and error checking along with automatic noise squelching.



Figure 1: TDL2 radio modem

The TDL2 provides a half duplex link. Provided no two devices attempt to transmit simultaneously no further restrictions on data transmission need be made, as all transmit timing, valid data identification and datastream buffering is conducted by the unit. There is no Transmit Enable pin like BiM2. Synchronisation and framing words in the packet prevent the receiver outputting garbage in the absence of wanted RF signal or presence of interference. For multiple radio systems (polled networks) a TDL2 can be set to 1 of 8 unique addresses (by default all units are shipped set to address 0).

Features

- 433MHz version conforms to EN 300 220-3 and EN 301 489-3
- Crystal controlled PLL stabilised VCO
- SAW front-end filter
- Single conversion superhet
- Serial baud rate at 9600bps (half-duplex)
- Addressable point-to-point
- Data Present indication
- Fully screened. Low profile

Applications

- Handheld terminals
- EPOS equipment, barcode scanners
- Data loggers
- Industrial telemetry and telecommand
- In-building environmental monitoring and control
- GPS systems
- Vehicle data up/download

Technical Summary

- Operating frequency: 433.925MHz
- Modulation: 16kbps bi-phase FSK
- Supply: 5V at 25mA transmit, 20mA receive/idle
- Transmit power: +3dBm (2mW)
- Receiver sensitivity: -105dBm (for 1% data error)
- 32 byte data buffer
- Transmit power-up time: <4ms

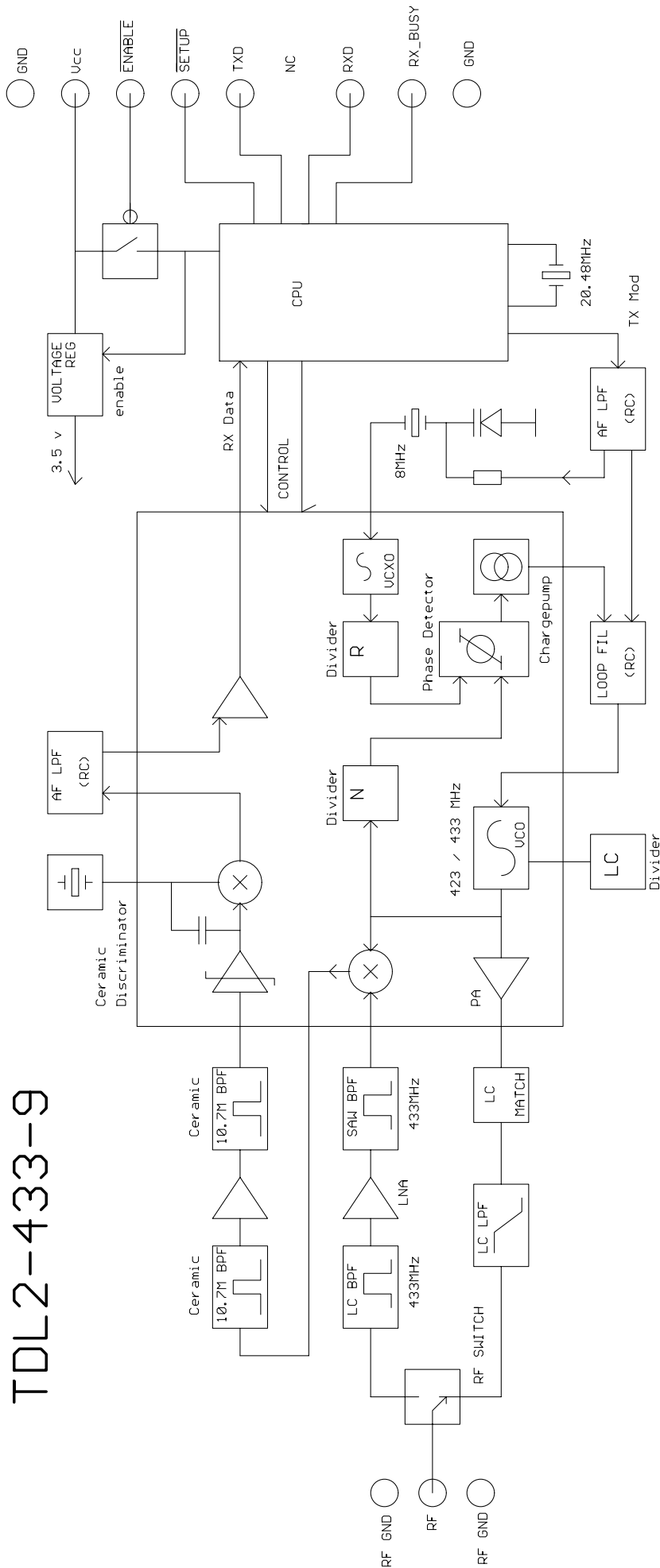


Figure 2: TDL2 block diagram

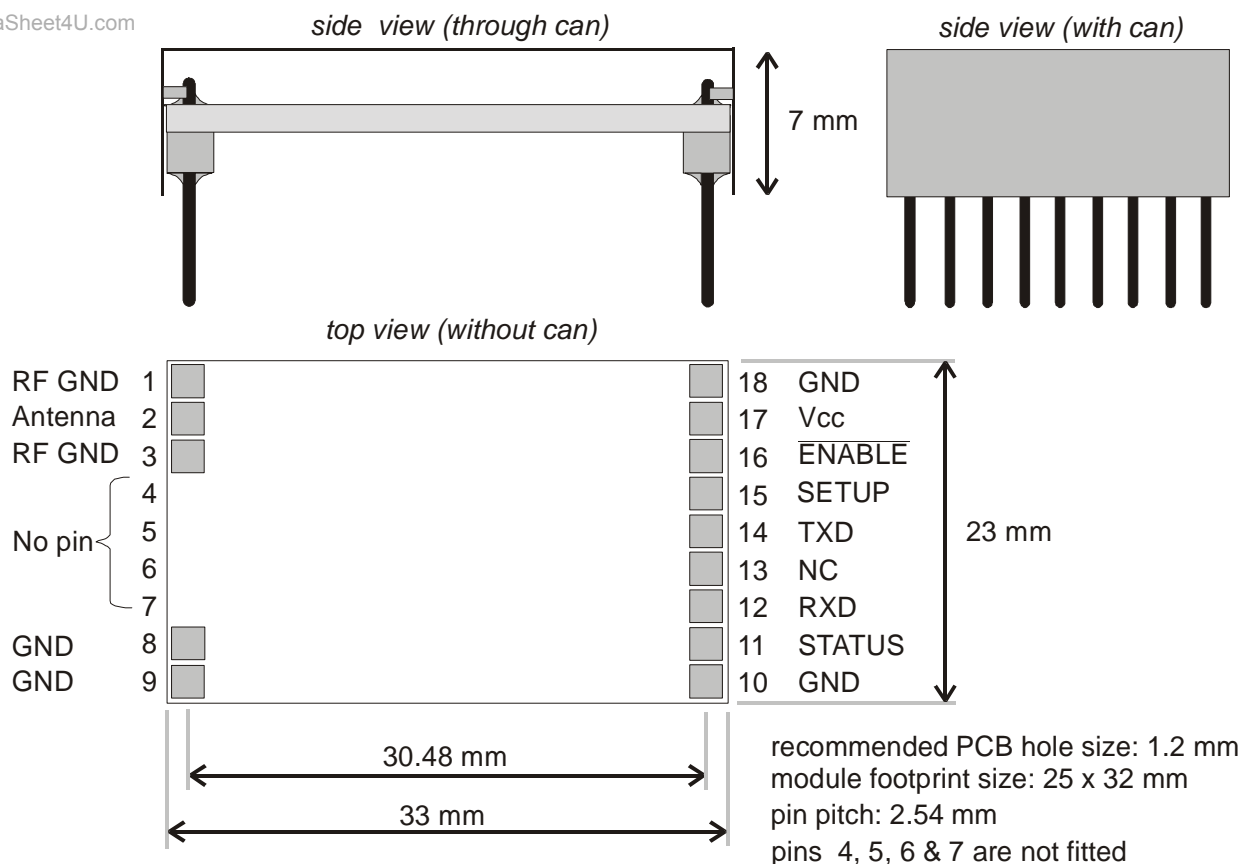


Figure 3: TDL2 footprint (top view)

Pin description - TLC2

Pin	Name	Function
18	GND	Ground
17	Vcc	5V (regulated power supply)
16	ENABLE	Enable or DTR (5V CMOS logic level input)
15	SETUP	Test/Setup mode selection
14	TXD	Transmit Data (Inverted RS232 at 5V CMOS logic level)
13	NC	No Pin
12	RXD	Receive Data (Inverted RS232 at 5V CMOS logic level)
11	STATUS	Busy or CTS (5V CMOS logic level output)
10	GND	Ground

RF GND *pin 1 & 3*

RF Ground pin, internally connected to the module screen and pin 8, 9, 10 and 18 (0V). This pin should be connected to the RF return path (e.g. co-axial cable braid, main PCB ground plane, etc).

RF *pin 2*

50Ω RF input/output from the antenna, it is DC isolated internally. (see antenna section for details).

GND *pin 8, 9, 10 and 18*

Supply ground connection to ground plane and can.

VCC *pin 17*

5V voltage regulator should be used to have a clean 5V supply to the module. A 3.5V regulator is used inside for radio circuitry.

ENABLE *pin 16*

Active low Enable pin. It has a 10kΩ pull-ups to Vcc. It should be pulled Low to enable the module. This can also be connected to DTR pin (only if it is asserted by the host) of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter.

SETUP *pin 15*
Active low input to enter configuration or diagnostic test mode.

TXD *pin 14*
This is inverted RS232 data input at 5V CMOS logic level. It can be directly interfaced to data output of a UART in a microcontroller or to a TXD pin of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter. TXD does not have an internal pull-up. If TDL2 is used in Receive only mode, TXD should be tied to Vcc.

NC *pin 13*
There is no pin in this position.

RXD *pin 12*
This is inverted RS232 data output at 5V CMOS logic level. It can be directly interfaced to data input of a UART in a microcontroller or to a RXD pin of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter.

STATUS *pin 11*
This pin goes high when valid data is present in the receive buffer. It can be used to trigger an interrupt in the host to download received data packet instead of waiting for it. It can be also be used as a primitive CTS signal. It is inverted RS232 data output at 5V CMOS logic level. It can be directly interfaced to an input of a microcontroller as a Data Detect (DD) or to CTS, DSR, DCD pins of an RS232 serial port via a MAX232 or equivalent RS232-CMOS level converter. This is can only be used to prevent host from uploading any data before downloading already received data, because transmission is prioritised over reception and any data to be transmitted will erase received data which is in the common buffer.

Serial interface commands

To connect to a true RS232 device, inverting RS232-CMOS level shifters must be used. Maxim MAX232 or equivalent are ideal, but simple NPN transistor switches with pull-ups often suffice. With typical microcontrollers and UARTs, direct connection is possible.

The Radio / data stream interface

A 32 byte software FIFO is implemented in both the transmit and receive sub-routine. At the transmitting end this is used to allow for the transmitter start up time (about 3mS), while on receiving end it buffers arriving packets to the constant output data rate. All timing and data formatting tasks are handled by the internal firmware. The user need not worry about keying the transmitter before sending data as the link is entirely transparent.

For transmission across the radio link data is formatted into packets, each comprising 3 bytes of data and a sync code. If less than 3 bytes are in the transmit end FIFO then a packet is still sent, but idle codes replaces the unused bytes. When the transmit end FIFO is completely emptied, then the transmitter is keyed off.

Operation: Radio interface.

Raw data is not fed to the radios. A coding operation in the transmit sub-routine, and decoding in the receiver, isolate the AC coupled, potentially noisy baseband radio environment from the datastream.

The radio link is fed a continuous tone by the modem. As in bi-phase codes, information is coded by varying the duration consecutive half-cycles of this tone. In our case half cycles of 62.5us and 31.25us are used. In idle (or 'preamble') state, a sequence of the longer cycles is sent (resembling an 8KHz tone).

A packet comprises the Synchronising (or address) part, followed by the Data part, made up of twelve Groups (of four half cycles duration). Each Group encodes 2 data bits, so one byte is encoded by 4 Groups.

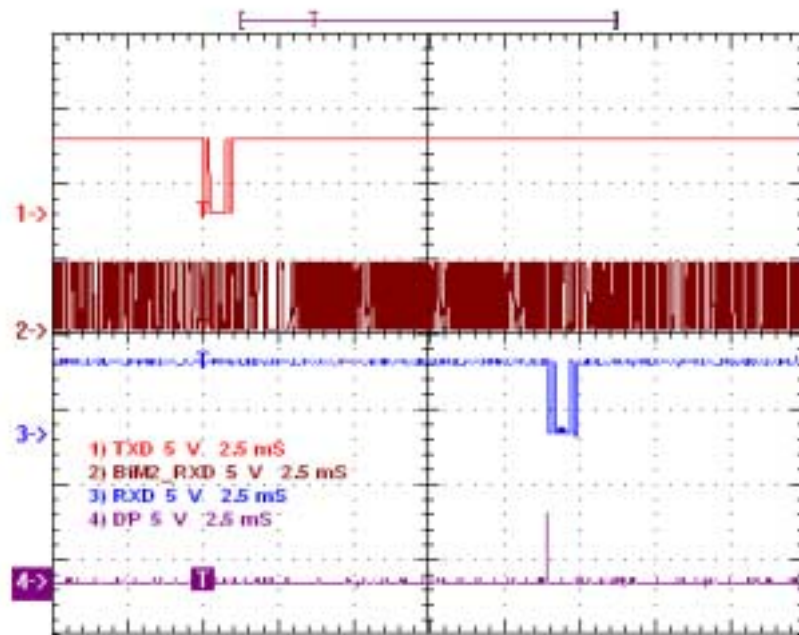


Figure 5: TDL2 transmitting and receiving

The oscilloscope screen capture shows a single ASCII character being transmitted by TDL2. A BiM2-433-160 transceiver is used to capture the transmitted data

The character appears on the serial data output (RXD) pin of the other TDL2 after about 11.3ms. Busy (STATUS) pin is momentarily set high to indicate the presence of a valid data in the receive buffer of the TDL2.

It can be clearly seen that unlike raw radio modules, TDL2 does not output any noise when there is not any transmission. Data fed into the TXD input of a TDL2 appears at the RXD output of another TDL2 within radio range in the original form it was fed.

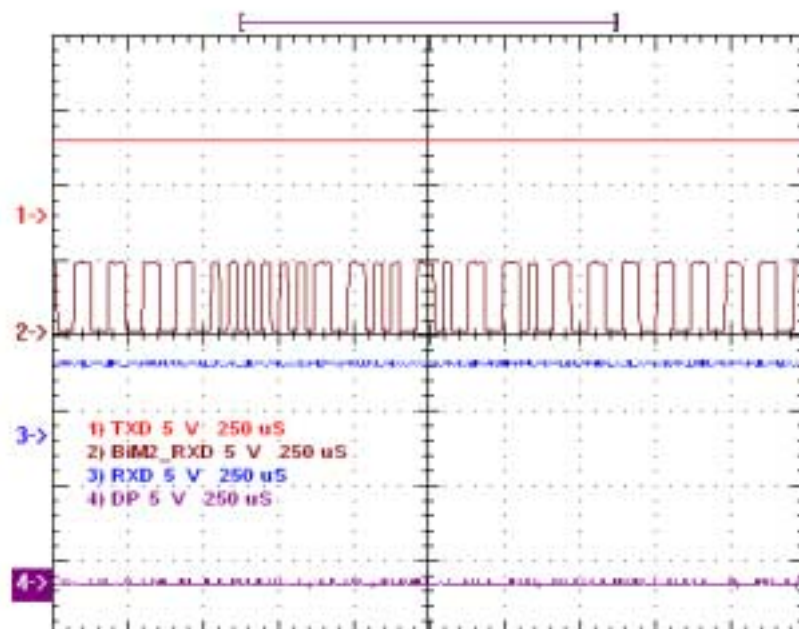


Figure 6: Bi-phase encoded TDL2 data packet (expanded view)

Programming the TDL2

In order to use all the functions embedded in the TDL2, the user must be aware of the setup/programming facility, which allow different addresses to be set up, and if necessary accesses diagnostic test modes.

The TDL2 is programmed through the same RS232 port that is used for sending/receiving data. An RS232 terminal emulator (such as Aterm or HyperTerminal) is an ideal tool.

To enter program mode, the SETUP pin must be pulled low. In this mode the radio link is disabled, but characters sent (at 9600 baud, as normal) to the unit are echoed back on the RXD pin.

The unit will only respond to certain command strings:

ADDR0 to ADDR7 These commands set up one of 8 unique addresses. A TDL2 will only communicate with a unit set to the same address.

Address number is stored in volatile memory. On power-up the TDL2 reverts to the default in EEPROM (as supplied this is always address 0)

SETPROGRAM: Writes the current set address into EEPROM as the new default. After a successful program cycle, a ~ (tilda) is sent to the terminal.

(these commands are normally only used for factory diagnostics)

NOTONE: Transmit unmodulated carrier
LFTONE: Transmit carrier modulated with 8KHz squarewave
HFTONE: Transmit carrier modulated with 16KHz squarewave
Transmitter off

Releasing the SETUP pin to high state returns the TDL2 to normal operation.

Interfacing a microcontroller to TDL2

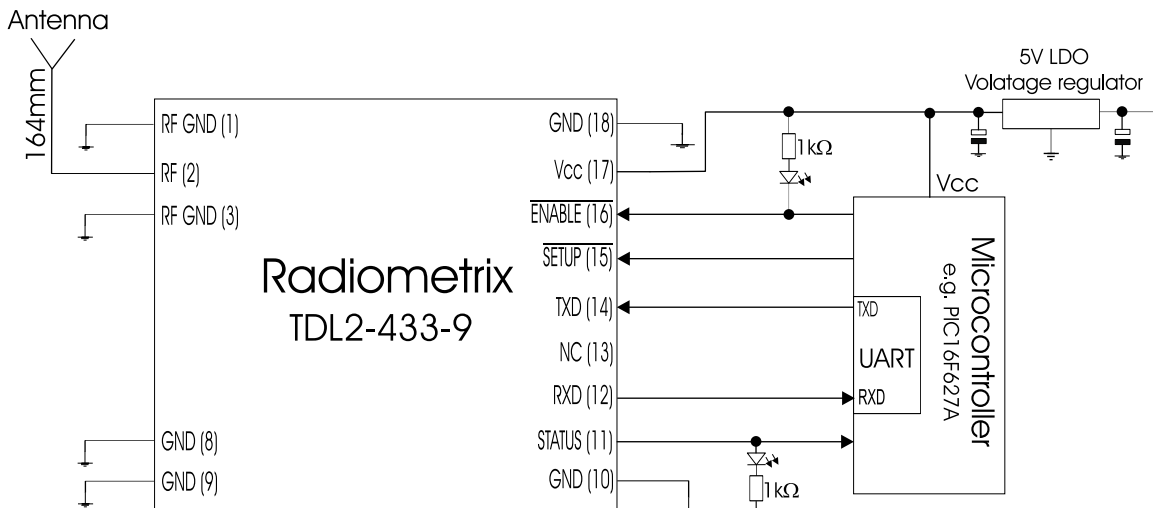


Figure 7: TDL2 interfaced directly to a microcontroller

TDL2 can be directly interfaced to any microcontrollers. If the microcontroller has a built-in UART, it can concentrate on its main task and leave the packet formatting, bit balancing and error checking of serial data to TDL2.

Serial data should be in the following format:

1 start bit, 8 data bits, no parity, 1 or 2 stop bits
 9600bps
 0V=low, 5V=high

STATUS pin can be connected to one of the port pins which can generate an interrupt on low-to-high transition (e.g. RB0/INT pin in the PIC). This can be used to enter a receive sub-routine to download data received from remote TDL2. Therefore, the host does not need to wait in a loop for a packet.

Range test and site survey can be carried out by connecting an LED on the STATUS pin. Every time, TDL2 is within range to receive valid data, the LED will flicker.

Interfacing RS232 port to TDL2

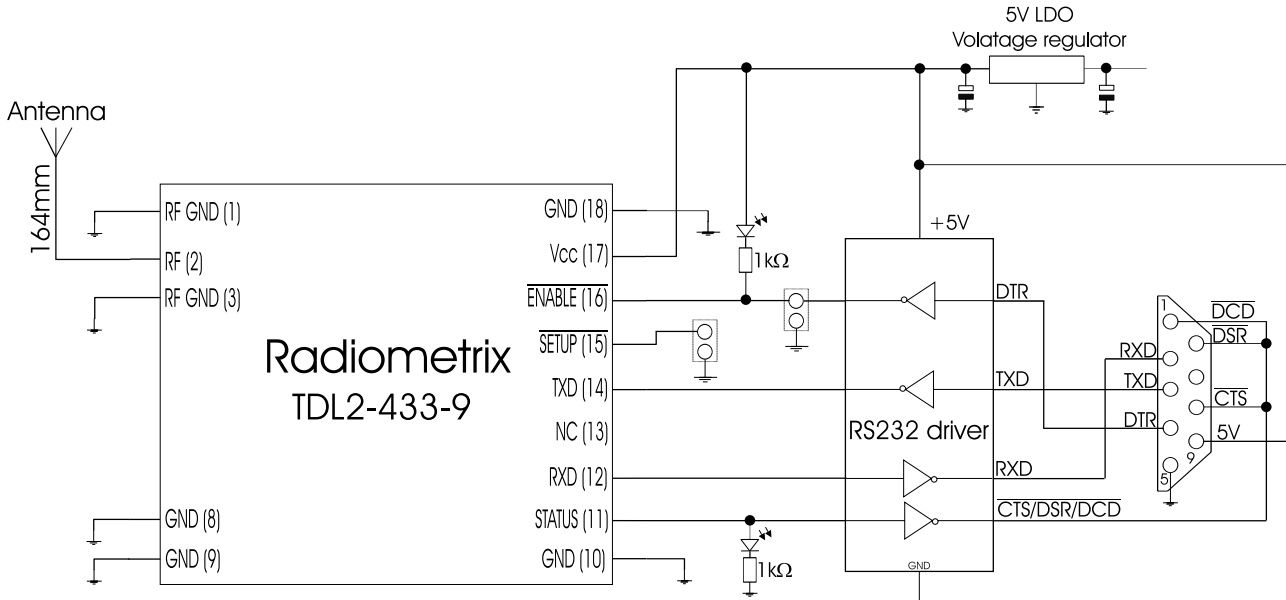


Figure 8: TDL2 interfaced to an RS232 port via an RS232 line driver/receiver

STATUS pin in this can be connected to CTS, DSR and DCD pin to simulate a flow control signal.

TDL2 is capable of continuously streaming data at 9600bps. Therefore, STATUS pin is not asserted to stop the Host from sending data as in normal RTS/CTS flow control method, but merely to warn the host that there is already data in the receive buffer which need to be downloaded before sending any more data.

Some DTE hosts assert DTR signal when they are active and this can be used via RS232 line receiver to enable TDL2. Otherwise the ENABLE must be physically pulled-low to activate the TDL2.

NOTE:

An interface board (with MAX232 type buffer, 9 way D connector, 5V voltage regulator and SMA RF connector) is available. This board is 61mm x 33mm in size.

Condensed specifications

www.DataSheet4U.com

Frequency	433.925MHz
<i>Frequency stability</i>	±10kHz
<i>Channel width</i>	300kHz
<i>Number of channels</i>	1

Operating temperature	-10 C to +60 C (Storage -30 C to +70 C)
Spurious radiations	Compliant with ETSI EN 300 220-3 and EN 301 489-3

Interface

<i>User</i>	9pin 0.1" pitch molex
<i>RF</i>	3pin 0.1" pitch molex

Size	33 x 23 x 7mm
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Transmitter	
Output power	3dBm (2mW) ±1dB
TX on switching time	<4ms
Modulation type	16kbps bi-phase FSK
FM peak deviation	+/-15KHz
Adjacent channel TX power	<-37dBm
TX spurious	<-50dBm
<i>Supply</i>	
Voltage	5V
Current	25mA transmit
Receiver	
Sensitivity	-105dBm for 1% data error
image / spurious / adjacent channel	-55dB
Blocking	-85dB
LO re-radiation	<-60dBm
<i>Supply</i>	
Voltage	5V
Current	20mA receive/idle
Data latency	14ms (first byte into TX, to first byte out of RX)

Antenna requirements

Three types of integral antenna are recommended and approved for use with the module:

- A) **Whip** This is a wire, rod ,PCB track or combination connected directly to RF pin of the module. Optimum total length is 16cm (1/4 wave @ 433MHz). Keep the open circuit (hot) end well away from metal components to prevent serious de-tuning. Whips are ground plane sensitive and will benefit from internal 1/4 wave earthed radial(s) if the product is small and plastic cased
- B) **Helical** Wire coil, connected directly to RF pin, open circuit at other end. This antenna is very efficient given it's small size (20mm x 4mm dia.). The helical is a high Q antenna, trim the wire length or expand the coil for optimum results. The helical de-tunes badly with proximity to other conductive objects.
- C) **Loop** A loop of PCB track tuned by a fixed or variable capacitor to ground at the 'hot' end and fed from RF pin at a point 20% from the ground end. Loops have high immunity to proximity de-tuning.

	A	B	C
	<i>whip</i>	<i>helical</i>	<i>loop</i>
Ultimate performance	***	**	*
Easy of design set-up	***	**	*
Size	*	***	**
Immunity proximity effects	*	**	***

The antenna choice and position directly controls the system range. Keep it clear of other metal in the system, particularly the 'hot' end. The best position by far, is sticking out the top of the product. This is often not desirable for practical/ergonomic reasons thus a compromise may need to be reached. If an internal antenna must be used, try to keep it away from other metal components, particularly large ones like transformers, batteries and PCB tracks/earth plane. The space around the antenna is as important as the antenna itself.

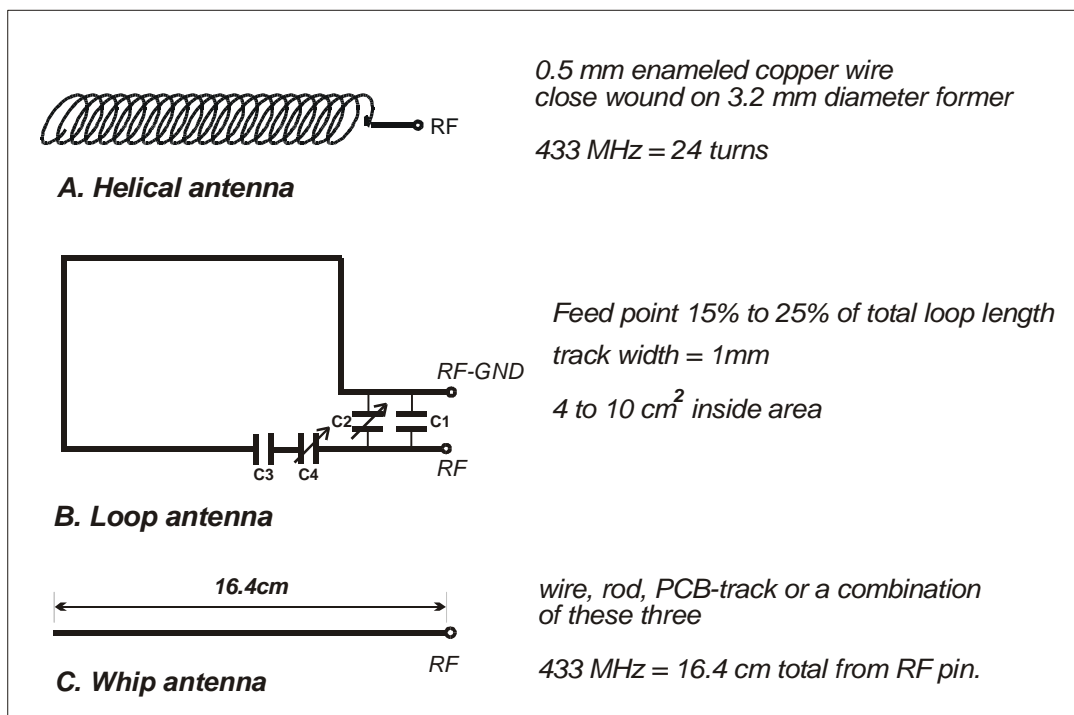


Figure 9: Antenna types

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The Intrastat commodity code for all our modules is: 8542 6000.

R&TTE Directive

After 7 April 2001 the manufacturer can only place finished product on the market under the provisions of the R&TTE Directive. Equipment within the scope of the R&TTE Directive may demonstrate compliance to the essential requirements specified in Article 3 of the Directive, as appropriate to the particular equipment.

Further details are available on Radiocommunications Agency (RA) web site:

<http://www.radio.gov.uk/topics/conformity/conform-index.htm>

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