

N-Channel Enhancement Mode MOSFET

TDM3482

DESCRIPTION

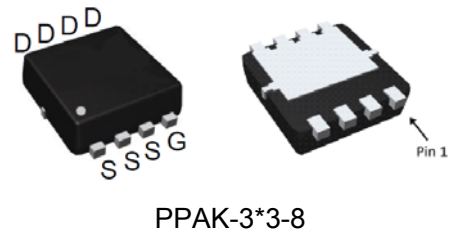
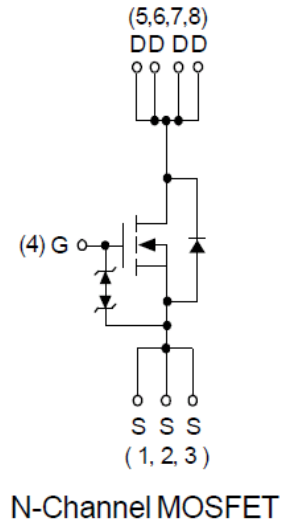
The TDM3482 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

- $R_{DS(ON)} < 16m\Omega$ @ $V_{GS}=4.5V$
 $R_{DS(ON)} < 9.5m\Omega$ @ $V_{GS}=10V$
- High Power and current handling capability
- ESD protection
- Lead free product is available
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management

ABSOLUTE MAXIMUM RATINGS($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Diode Continuous Forward Current	I_S	10	A
Drain Current @ Continuous	I_D ($T_C=25^\circ\text{C}$)	43	A
	I_D ($T_C=100^\circ\text{C}$)	28	A
Drain Current @ Current-Pulsed (Note 1)	I_{DM} ($T_C=25^\circ\text{C}$)	60	A
Maximum Power Dissipation	P_D ($T_C=25^\circ\text{C}$)	27.8	W
	P_D ($T_C=100^\circ\text{C}$)	11.1	W
Drain Current @ Continuous	I_D ($T_A=25^\circ\text{C}$)	12	A
	I_D ($T_A=70^\circ\text{C}$)	9.6	A
Maximum Power Dissipation	P_D ($T_A=25^\circ\text{C}$)	2.08	W
	P_D ($T_A=70^\circ\text{C}$)	1.3	W
Maximum Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 To 150	$^\circ\text{C}$

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THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient (Note 4)	R _{θJA} (t ≤ 10s)	40	°C/W
	R _{θJA} (Steady State)	60	°C/W
Thermal Resistance-Junction to Case	R _{θJC} (Steady State)	4.5	°C/W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

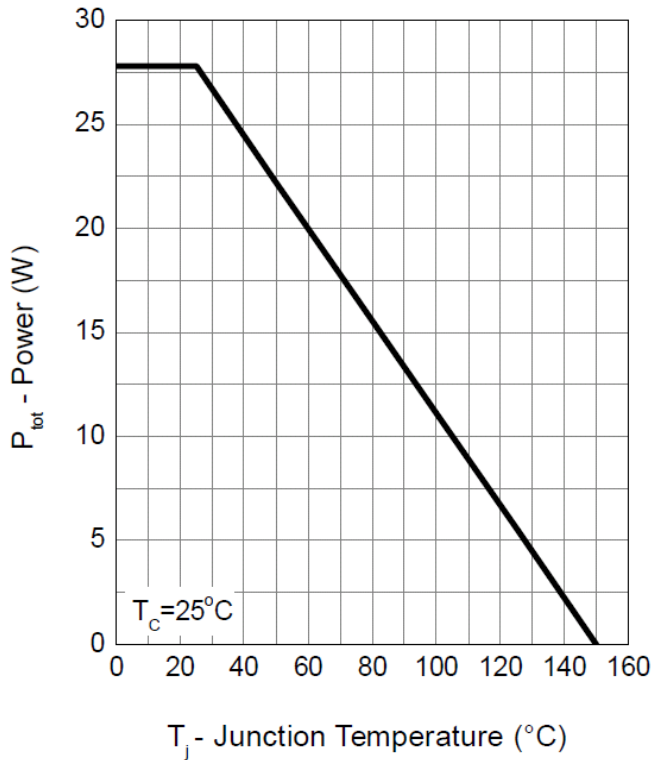
Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =32V,V _{GS} =0V	-	-	1	μ A
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±10	μ A
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.4	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =8A	-	11.5	16	mΩ
		V _{GS} =10V, I _D =15A	-	7.9	9.5	mΩ
		T _J =125℃	-	11.8	-	mΩ
DYNAMIC CHARACTERISTICS (Note3)						
Gate Resistance	R _G	V _{DS} =20V,V _{GS} =0V, F=1.0MHz	-	1.7	-	Ω
Input Capacitance	C _{iss}	V _{DS} =20V,V _{GS} =0V, F=1.0MHz	-	700	-	PF
Output Capacitance	C _{oss}		-	191	-	PF
Reverse Transfer Capacitance	C _{rss}		-	30	-	PF
SWITCHING CHARACTERISTICS (Note 3)						
Turn-on Delay Time	t _{d(on)}	V _{DS} =20V, R _L =20Ω, V _{GEN} =10V,R _G =6Ω I _D =1A	-	10	-	nS
Turn-on Rise Time	t _r		-	6.6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	18	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =20V,I _D =15A,V _{GS} =4.5V	-	5.1	-	nC
Gate-Source Charge	Q _{gs}		-	2.9	-	nC
Gate-Drain Charge	Q _{gd}		-	1.1	-	nC
Body Diode Reverse Recovery Time	T _{rr}	I _F =5A, dI/dt=100A/μs	-	18.8	-	nS
Body Diode Reverse Recovery Charge	Q _{rr}		-	4.5	-	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 2)	V _{SD}	V _{GS} =0V,I _S =20A	-	0.8	1.1	V

NOTES:

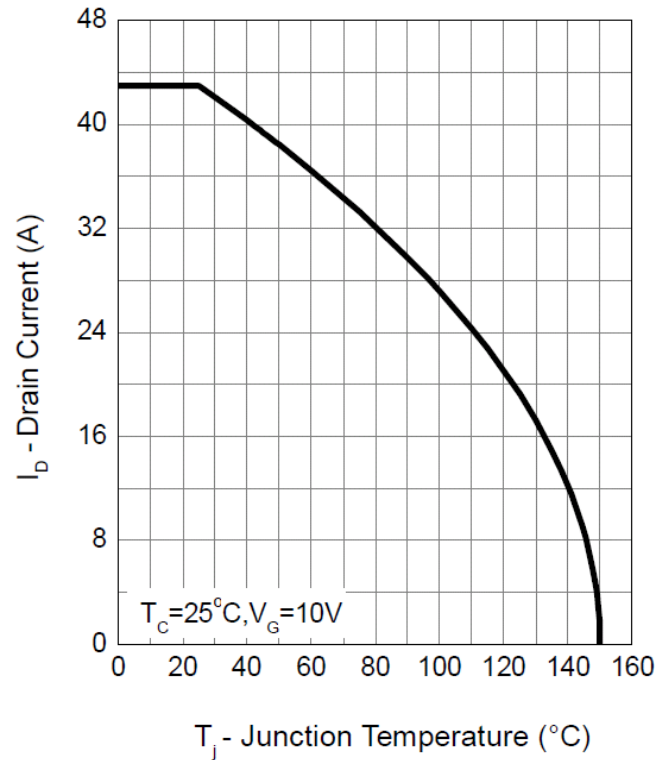
1. Pulse width limited by max. junction temperature.
2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
3. Guaranteed by design, not subject to production testing
4. R_{θJA} steady state t=100s. R_{θJA} is measured with the device mounted on 1in2, FR-4 board with 2oz. Copper.

Typical Operating Characteristics

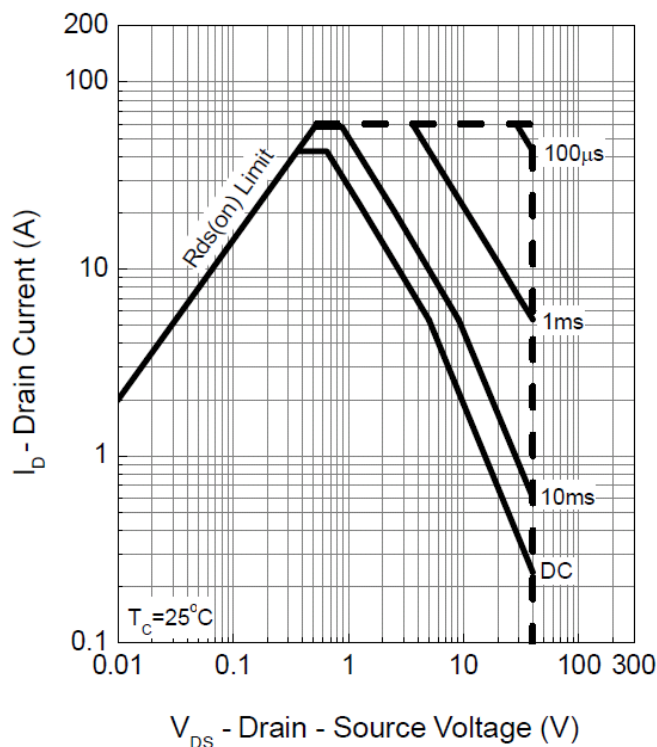
Power Dissipation



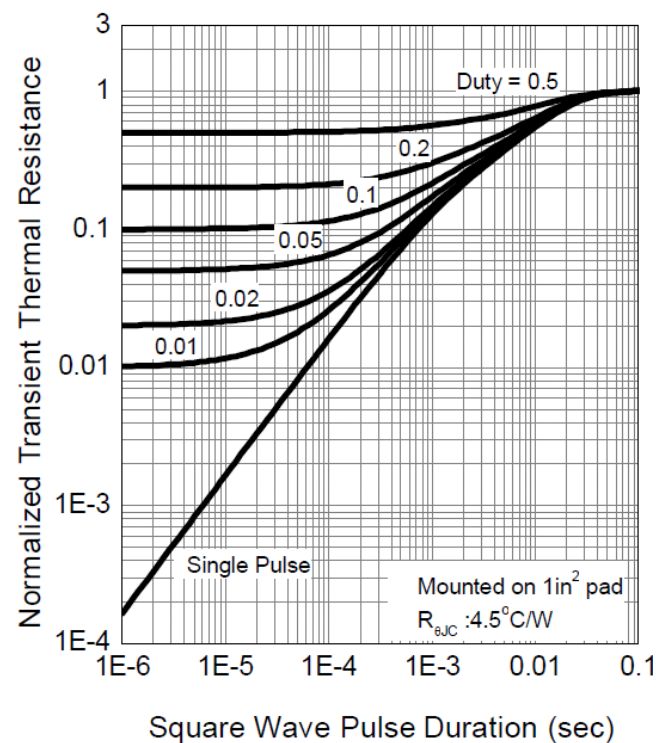
Drain Current



Safe Operation Area

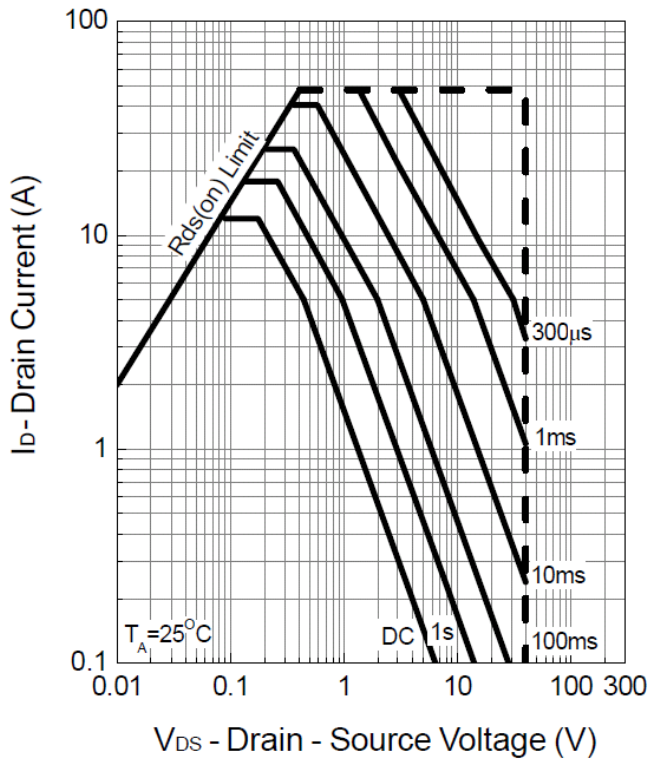


Thermal Transient Impedance

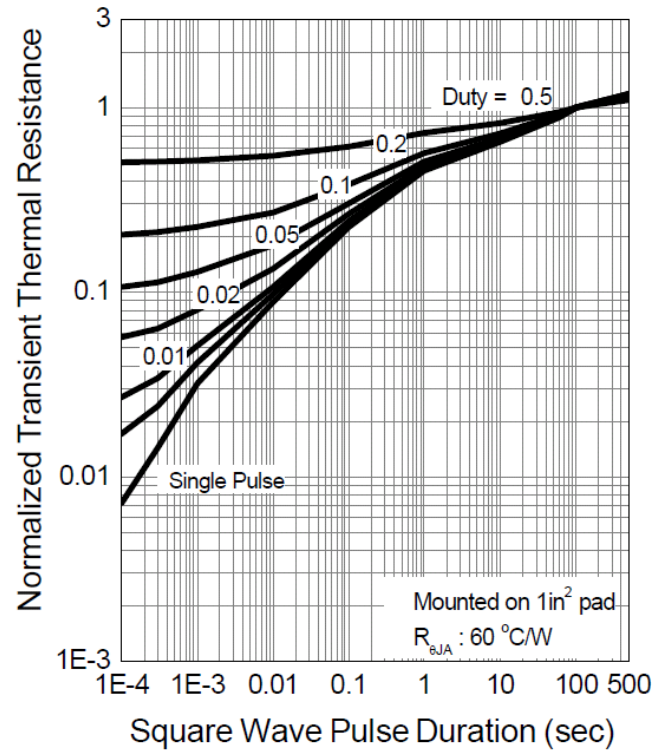


Typical Operating Characteristics(Cont.)

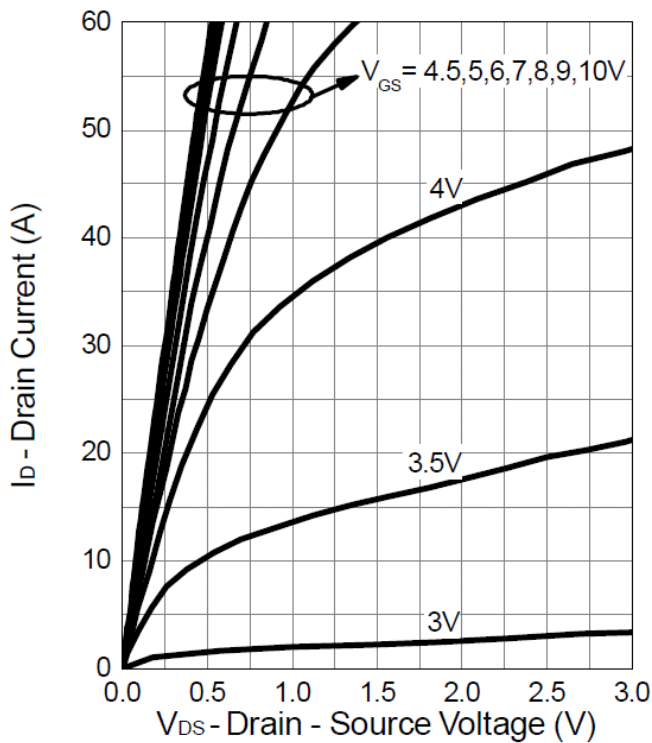
Safe Operation Area



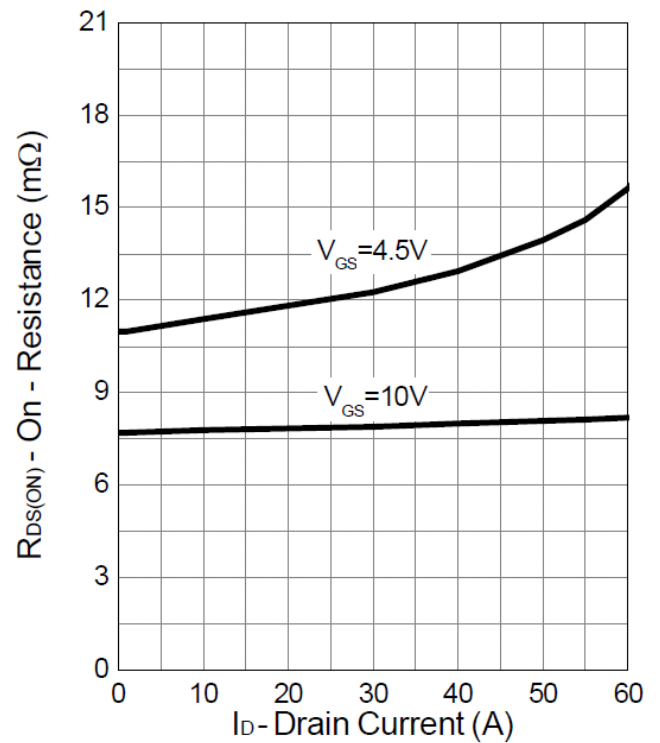
Thermal Transient Impedance



Output Characteristics

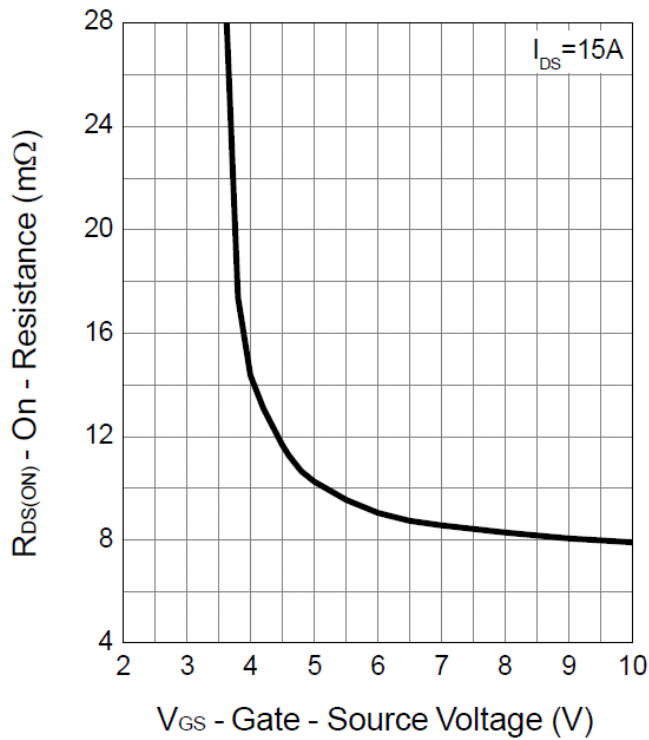


Drain-Source On Resistance

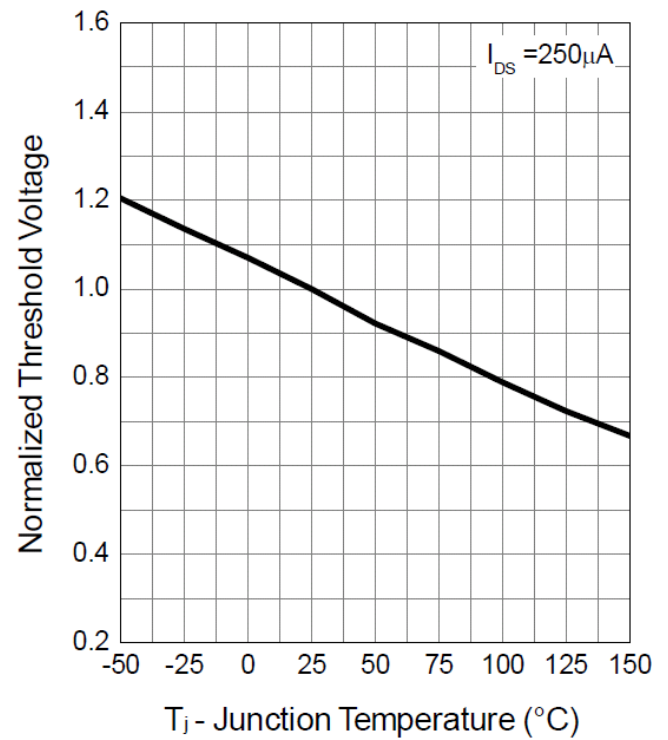


Typical Operating Characteristics(Cont.)

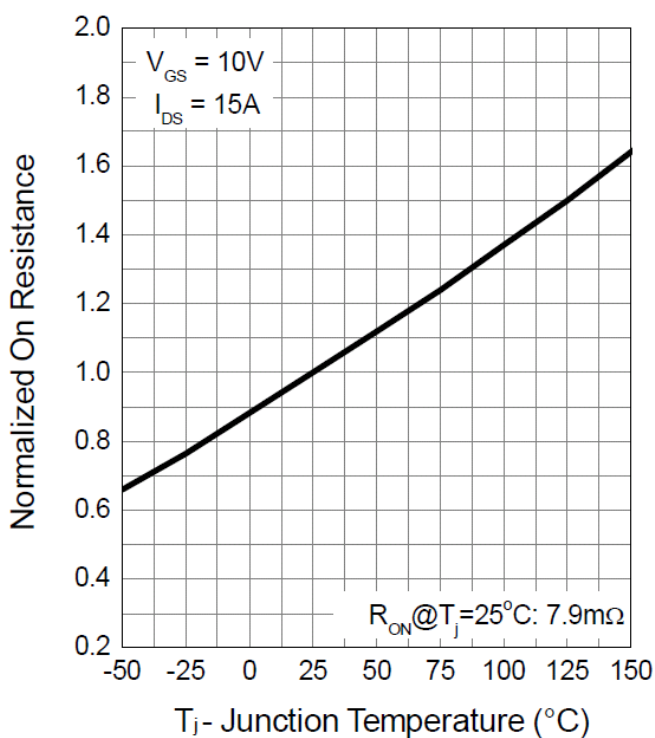
Gate-Source On Resistance



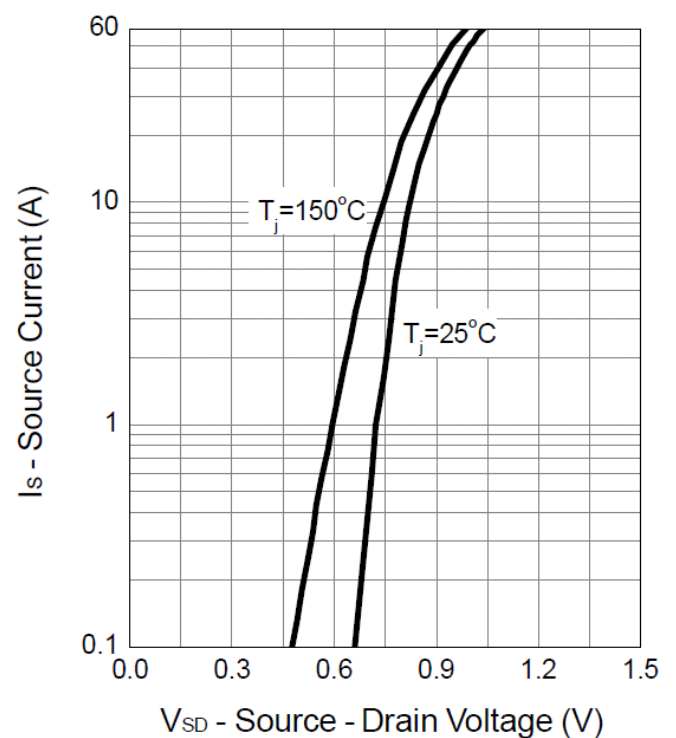
Gate Threshold Voltage



Drain-Source On Resistance

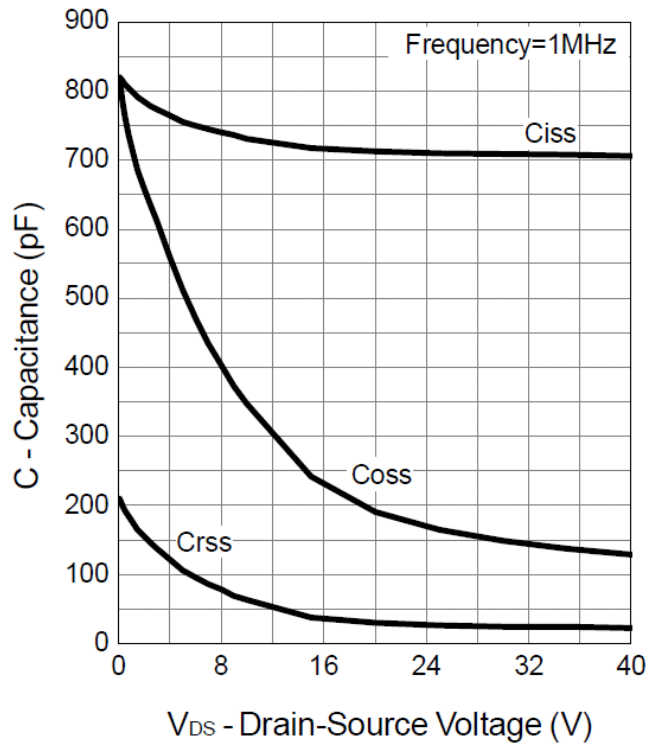


Source-Drain Diode Forward

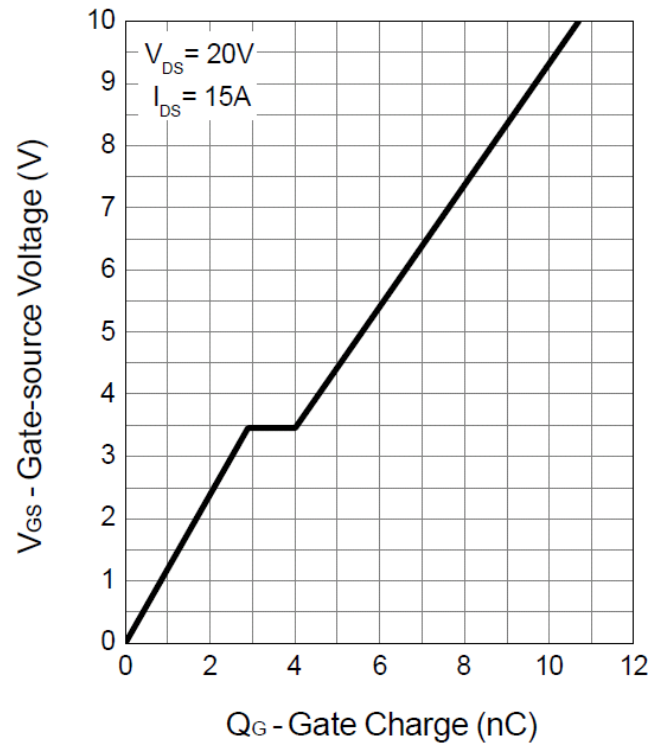


Typical Operating Characteristics(Cont.)

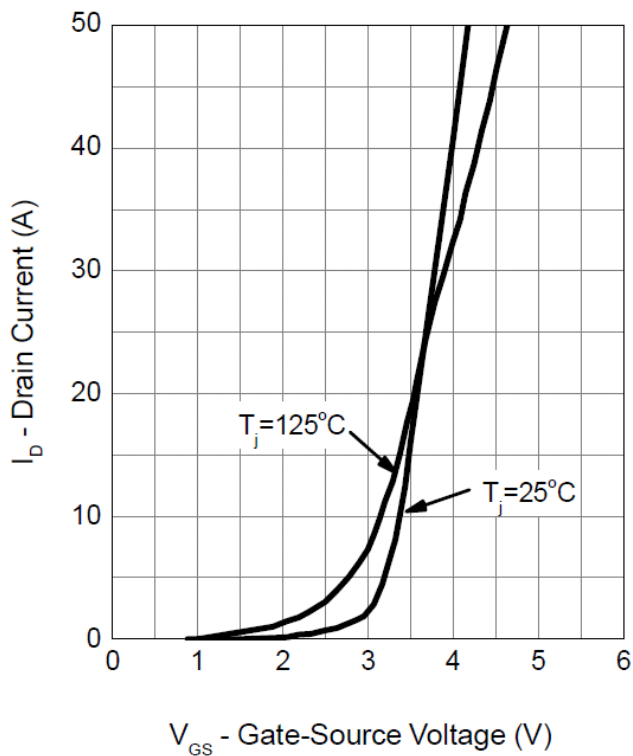
Capacitance



Gate Charge



Transfer Characteristics

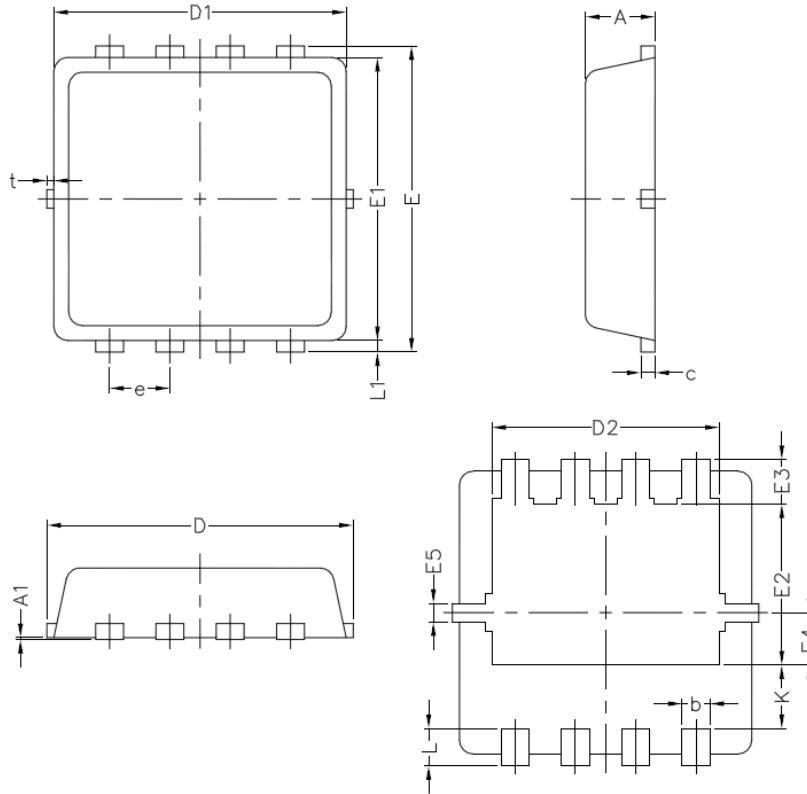


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Package Information

PPAK-3*3-8 Package



Symbol	PPAK-3*3-8(mm)		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.3	3.45
D1	3.00	3.15	3.30
D2	2.25	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.68
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.49	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	/	/	0.13

Design Notes