XC1800 Series of In-System Programmable Configuration PROMs

September 17, 1999 (Version 1.3)

Preliminary Product Specification

Features

- In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- IEEE Std 1149.1 boundary-scan (JTAG) support
- Simple interface to the FPGA; could be configured to use only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Dual configuration modes
  - Serial Slow/Fast configuration (up to 15 mHz).
  - Parallel
- Low-power advanced CMOS FLASH process
- 5 V tolerant I/O pins accept 5 V, 3.3 V and 2.5 V signals.
- 3.3 V or 2.5 V output capability
- Available in PC20, SO20, PC44 and VQ44 packages.
- Design support using the Xilinx Alliance and Foundation series software packages.
- JTAG command initiation of standard FPGA configuration.

Description

Xilinx introduces the XC1800 series of in-system programmable configuration PROMs. Initial devices in this 3.3V family are a 4 megabit, a 2 megabit, a 1 megabit, a 512 Kbit, a 256 Kbit, and a 128 Kbit PROM that provide an easy-to-use, cost-effective method for re-programming and storing large Xilinx FPGA or CPLD configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising CCLK, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

When the FPGA is in Express or SelectMAP Mode, an external oscillator will generate the configuration clock that drives the PROM and the FPGA. After the rising CCLK edge, data are available on the PROM's DATA (D0-D7) pins. The data will be clocked into the FPGA on the following rising edge of the CCLK. Neither Express nor SelectMAP utilize a Length Count, so a free-running oscillator may be used. See Figure 5

Multiple devices can be concatenated by using the $\overline{\text{CEO}}$ output to drive the $\overline{\text{CE}}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family or with the XC1700L one-time programmable Serial PROM family.

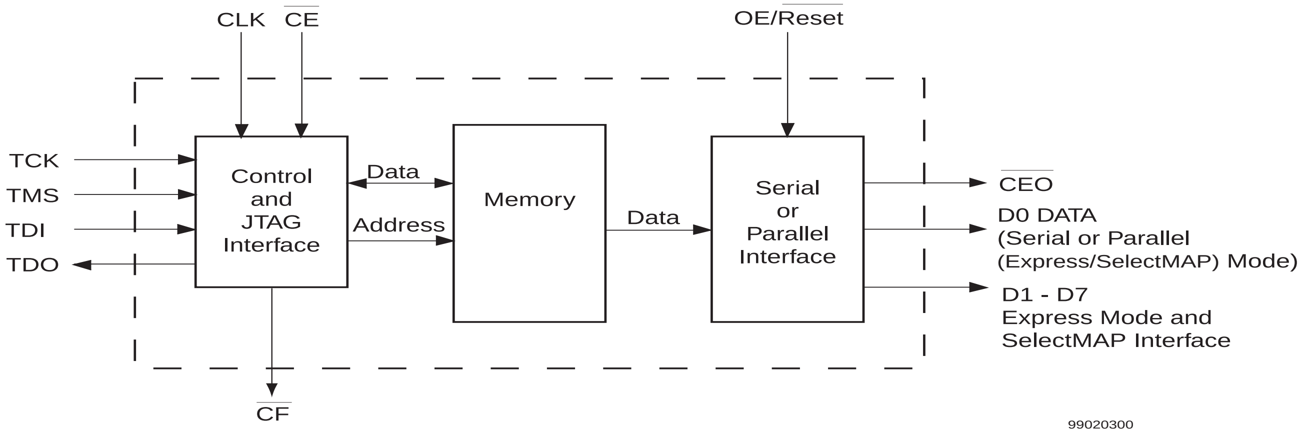


Figure 1: XC1800 Series Block Diagram

Pinout and Pin Description

Table 1: Pin Names and Descriptions

Pin Name	Boundary Scan Order	Function	Pin Description	44-pin VQFP	44-pin PLCC	20-pin SOIC & PLCC
D0	4	DATA OUT	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.	40	2	1
	3	OUTPUT ENABLE				
D1	6	DATA OUT	D0- D7 are the output pins to provide parallel data for configuring a Xilinx FPGA in express mode.	29	35	16
	5	OUTPUT ENABLE				
D2	2	DATA OUT		42	4	2
	1	OUTPUT ENABLE				
D3	8	DATA OUT		27	33	15
	7	OUTPUT ENABLE				
D4	24	DATA OUT		9	15	7*
	23	OUTPUT ENABLE				
D5	10	DATA OUT		25	31	14
	9	OUTPUT ENABLE				
D6	17	DATA OUT		14	20	9
	16	OUTPUT ENABLE				
D7	14	DATA OUT		19	25	12
	13	OUTPUT ENABLE				
CLK	0	DATA IN	Each rising edge on the CLK input increments the internal address counter if both $\overline{\text{CE}}$ is low and OE/$\overline{\text{RESET}}$ is high.	43	5	3
OE/$\overline{\text{RESET}}$	20	DATA IN	When Low, this input holds the address counter reset and the DATA output at high impedance.	13	19	8
	19	DATA OUT				
	18	OUTPUT ENABLE				
$\overline{\text{CE}}$	15	DATA IN	When $\overline{\text{CE}}$ is High, this pin puts the device into standby mode. The DATA output pin is at High impedance, and the device is in low power standby mode.	15	21	10
$\overline{\text{CF}}$	22	DATA OUT	Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA.	10	16	7*
	21	DATA IN				

Pin Name	Boundary Scan Order	Function	Pin Description	44-pin VQFP	44-pin PLCC	20-pin SOIC & PLCC
$\overline{\text{CEO}}$	13	DATA OUT	Chip Enable ($\overline{\text{CEO}}$) output is connected to the $\overline{\text{CE}}$ input of the next PROM in the chain. This output is Low when the $\overline{\text{CE}}$ and OE/$\overline{\text{RESET}}$ inputs are active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. When the PROM has been read, $\overline{\text{CEO}}$ will follow $\overline{\text{CE}}$ as long as OE/$\overline{\text{RESET}}$ is High. When OE/$\overline{\text{RESET}}$ goes Low, $\overline{\text{CEO}}$ stays High until the PROM is brought out of reset by bringing OE/$\overline{\text{RESET}}$ High. $\overline{\text{CEO}}$ can be programmed to be either active High or active Low.	21	27	13
	14	OUTPUT ENABLE				
GND			GND is the ground connection.	6, 18, 28 & 41	3, 12, 24 & 34	11
TMS		MODE SELECT	The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50K ohm resistive pull-up on it to provide a logic 1 to the device if the pin is not driven.	5	11	5
TCK		CLOCK	This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	7	13	6
TDI		DATA IN	This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50K ohm resistive pull-up on it to provide a logic 1 to the system if the pin is not driven.	3	9	4
TDO		DATA OUT	This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50k ohm resistive pull-up on it to provide a logic 1 to the system if the pin is not driven.	31	37	17
V_{CC}			Positive voltage supply of 3.3V for internal logic and input buffers.	17, 35 & 38	23, 41 & 44	18 & 20
V_{CCO}			Positive voltage supply connected to the output voltage drivers.	8, 16, 26 & 36	14, 22, 32 & 42	19

*Programmable for Serial Mode only on 18512 and 1801.

Xilinx FPGAs and Compatible PROMs

Device	Configuration Bits	PROM
XC4003E	53,984	XC18128
XC4005E	95,008	XC18128
XC4006E	119,840	XC18128
XC4008E	147,552	XC18256
XC4010E	178,144	XC18256
XC4013E	247,968	XC18256
XC4020E	329,312	XC18512
XC4025E	422,176	XC18512
XC4002XL	61,100	XC18128
XC4005XL	151,960	XC18256
XC4010XL	283,424	XC18512
XC4013XL/XLA	393,632	XC18512
XC4020XL/XLA	521,880	XC18512
XC4028XL/XLA	668,184	XC1801
XC4036XL/XLA	832,528	XC1801
XC4044XL/XLA	1,014,928	XC1801
XC4052XL/XLA	1,215,368	XC1802
XC4062XL/XLA	1,433,864	XC1802
XC4085XL/XLA	1,924,992	XC1802
XC40110XV	2,686,136	XC1804
XC40150XV	3,373,448	XC1804
XC40200XV	4,551,056	XC1804 + XC18512
XC40250XV	5,433,888	XC1804 + XC1802
XCV50	559,232	XC1801
XCV100	781,248	XC1801
XCV150	1,041,128	XC1801
XCV200	1,335,872	XC1802
XCV300	1,751,840	XC1802
XCV400	2,546,080	XC1804
XCV600	3,608,000	XC1804
XCV800	4,715,648	XC1804 + XC18512
XCV1000	6,127,776	XC1804 + XC1802

Capacity

Devices	Configuration Bits
1804	4,194,304
1802	2,097,152
1801	1,048,576
18512	524,288
18256	262,144
18128	131,072

In-System Programming

One or more in-system programmable PROMs can be daisy chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using Xilinx JTAG Programmer software and a download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All outputs are 3-stated or held at clamp levels during in-system programming.

External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx HW-130 device programmer. This provides the added flexibility of using pre-programmed devices in design, boundary-scan manufacturing tools, with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a minimum endurance level of 10,000 in-system program/erase cycles and a minimum data retention of 10 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable PROM devices incorporate advanced data security features to fully protect the programming data against unauthorized reading. Table 2 shows the security setting available.

The read security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. When set it allows device erase. Erasing the entire device is the only way to reset the read security bit.

Table 2: Data Security Options

Default	Set
Read Allowed Program/Erase Allowed	Read Inhibited via JTAG Erase Allowed

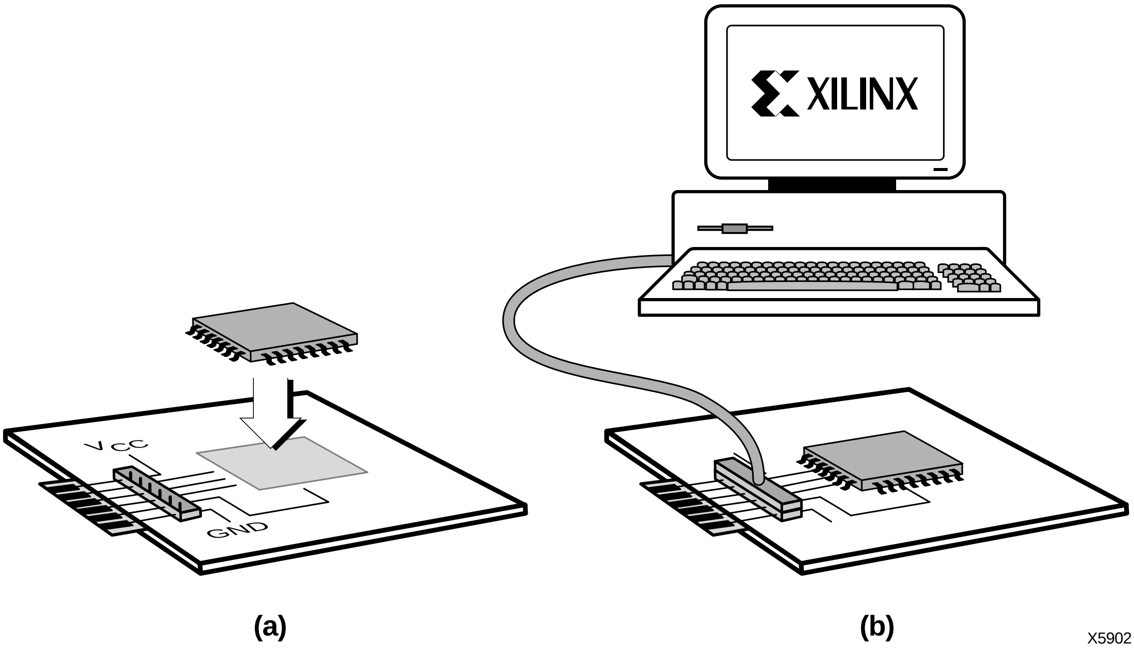


Figure 2: In-System Programming Operation (a) solder device to PCB and (b) Program using Download Cable

IEEE 1149.1 Boundary-Scan (JTAG)

The XC1800 family is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the XC1800 device.

Table 3 lists the required and optional boundary-scan instructions supported in the XC1800. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Table 3: Boundary Scan Instructions

Boundary-Scan Command	Binary Code (7:0)	Description
Required Instructions		
BYPASS	11111111	Enables BYPASS
SAMPLE/ PRELOAD	00000001	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00000000	Enables boundary-scan EXTEXT operation
Optional Instructions		
CLAMP	11111010	Enables boundary-scan CLAMP operation
HIGHZ	11111100	3-states all outputs simultaneously
IDCODE	11111110	Enables shifting out 32-bit IDCODE
USERCODE	11111101	Enables shifting out 32-bit USERCODE
XC1800 Specific Instructions		
CONFIG	11101110	Initiates FPGA configuration by pulsing CF pin low

Instruction Register

The Instruction Register (IR) for the XC1800 is 8-bits wide and is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI. The detailed composition of the instruction capture pattern is illustrated in Figure 3.

The ISP Status field, IR(4), contains logic 1 if the device is currently in ISP mode; otherwise, it will contain 0. The Security field, IR(3), will contain logic 1 if the device has been programmed with the security option turned on; otherwise, it will contain 0.

	IR(7:5)	IR(4)	IR(3)	IR(2)	IR(1:0)	
TDI->	0 0 0	ISP Status	Security	0	0 1	->TDO

Note: IR(1:0) = 01 is specified by IEEE Std. 1149.1

Figure 3: Instruction Register values loaded into IR as part of an instruction scan sequence

Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/ PRELOAD, and CLAMP instructions. Each output pin on the XC1800 has two register stages that contribute to the boundary-scan register, while each input pin only has one register stage.

For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the 3-state enable state of the pin.

For each input pin, the register stage controls and observes the input state of the pin.

Identification Registers

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32-bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction.

The IDCODE register has the following binary format:

`vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1`

where

v= the die version number

f=the family code (50h for XC1800 family)

a=the ISP PROM product ID (06h for the XC1804)

c=the company code (49h for Xilinx)

Note: The LSB of the IDCODE register is always read as logic 1 as defined by IEEE Std. 1149.1

Table 4: IDCODES Assigned to XC1800 devices

ISP-PROM	IDCODE
XC1801	05004093h
XC1804	05006093h

Table 4 lists the IDCODE register values for the XC1800 devices.

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the devices's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted our for examination. This code is loaded into the USERCODE register during programming of the XC1800 device. If the device is blank or was not loaded during programming, the USERCODE register will contain FFFFFFFFh.

XC1800 TAP Characteristics

The XC1800 family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the XC1800 TAP are described as follows.

TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

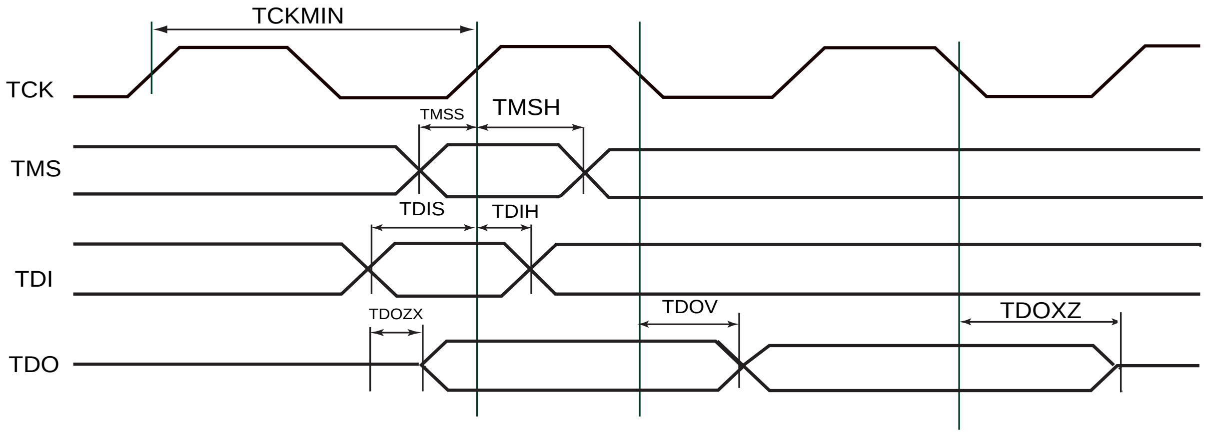


Figure 4: Test Access Port Timing

TAP AC Parameters

Table 5 shows the timing parameters for the TAP waveforms shown in Figure 4

Table 5: Test Access Port Timing Parameters (ns)

Symbol	Parameter	Min	Max
TCKMIN	TCK Minimum Clock Period	100	
TMSS	TMS Setup Time	10	
TMSH	TMS Hold Time	10	
TDIS	TDI Setup Time	15	
TDIH	TDI Hold Time	25	
TDOZX	TDO Float to Valid Delay		35
TDOXZ	TDI Valid to Float Delay		35
TDOV	TDO Valid Delay		35

Controlling Configuration PROMs

Connecting the FPGA device with the configuration PROM.

- The DATA output(s) of the of the PROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The CEO output of a PROM drives the CE input of the next PROM in a daisy chain (if any).
- The OE/RESET input of all PROMs is best driven by the INIT output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The PROM CE input can be driven from either the LDC or DONE pins. Using LDC avoids potential contention on the DIN pin. If the CE input of the first (or only) PROM can be driven by the DONE output of the first FPGA device, provided that DONE is not permanently grounded. Otherwise, LDC can be used to drive CE, but must then be unconditionally High during user operation. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.
- Express mode is similar to slave serial mode. The DATA is clocked out of the SPROM one byte per CCLK instead of one bit per CCLK cycle. To synchronize with the FPGA the first byte of data is valid 20ns before the second rising edge of CCLK and then on every consecutive CCLK thereafter. Note: When programming in Express mode, to accommodate the 4us set-up time on the INIT pin of the Spartan FPGA, the first line of the configuration stream must not be placed higher than the 3C byte address of the PROM.

Initiating FPGA Configuration

The XC1800 devices incorporate a pin named CF that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG will pulse the CF low for 300-500ns, which will reset the FPGA and initiate configuration.

The CF pin must be connected to the PROGRAM pin on the FPGA to use this feature.

Selecting Configuration Modes

The XC1800 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC1800 device. This control register is accessible through JTAG, using the Xilinx JTAG Programmer software.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. Xilinx PROMs are designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK. If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a PROM, the OE/RESETpin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the OE/RESETpin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

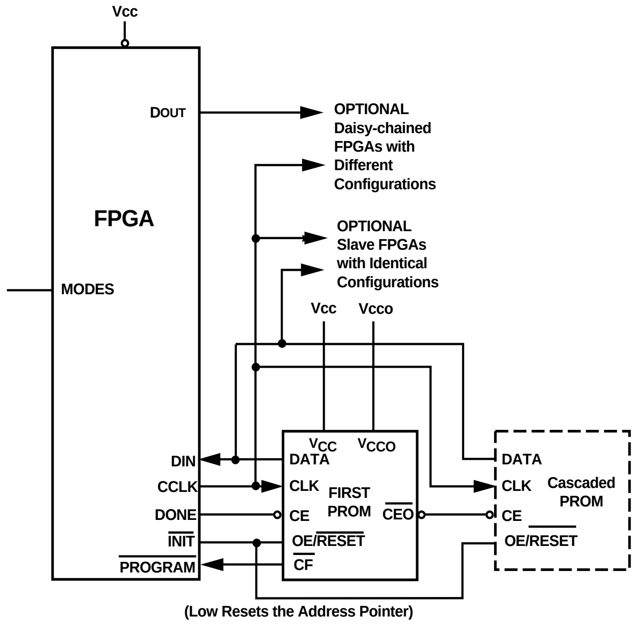
This method fails if a user applies OE/RESET during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its OE input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

Cascading Configuration PROMs

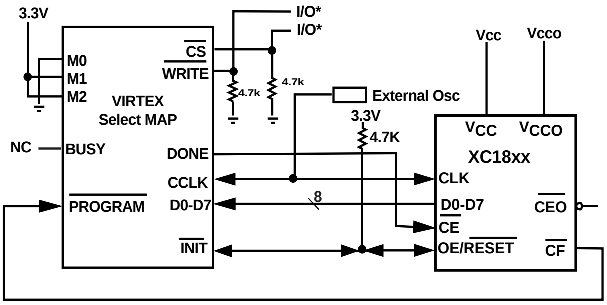
For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. Multiple XC1800 devices can be concatenated by using the CEO output to drive the CE input of the following device. The clock inputs and the data outputs of all XC1800 devices in the chain are interconnected. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{\text{CEO}}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{\text{CE}}$ input and enables its DATA output. See Figure 5.

After configuration is complete, the address counters of all cascaded PROMs are reset if the PROM OE/$\overline{\text{RESET}}$ pin goes Low.

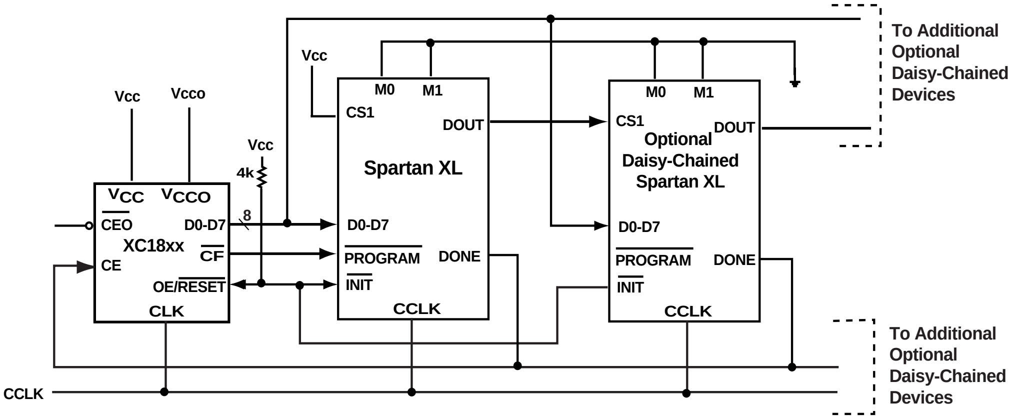
To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.



Master Serial Mode



Virtex Select MAP Mode



Spartan XL Express Mode

*CS and WRITE must be pulled down to be used as I/O. One option is shown.

Figure 5: (a) Master Serial Mode (b) Virtex Select MAP Mode (c) Spartan XL Express Mode

5V Tolerant I/Os

The I/Os on each re-programmable PROM are fully 5V tolerant even through the core power supply is 3.3 volts. This allows 5V CMOS signals to connect directly to the PROM inputs without damage. In addition, the 3.3V V_{CC} power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply (V_{CC}), and the output power supply (V_{CCO}) may have power applied in any order. This makes the PROM devices immune to power supply sequencing issues.

Reset Activation

On power up, OE/$\overline{\text{RESET}}$ is held low until the XC1800 is active (1ms) and able to supply data after receiving a CCLK pulse from the FPGA. OE/$\overline{\text{RESET}}$ is connected to an external resistor to pull OE/$\overline{\text{RESET}}$ HIGH releasing the FPGA $\overline{\text{INIT}}$ and allowing configuration to begin. OE/$\overline{\text{RESET}}$ is held low until the XC1800 voltage reaches the operating voltage range. If the power drops below 2.0 Volts, the PROM will reset.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. The output remains in a high impedance state regardless of the state of the OE input. JTAG pins TMS, TDI and TDO can be 3-state or high.

Table 6: Truth Table for PROM Control Inputs

Control Inputs		**Internal Address**	**Outputs**		
OE/$\overline{\text{RESET}}$	**$\overline{\text{CE}}$**		**DATA**	**CEO**	**I_{CC}**
Low	Low	if address ≤ TC: increment if address > TC: don't change	active 3-state	High Low	active reduced
High	Low	Held reset	3-state	High	active
Low	High	Held reset	3-state	High	standby
High	High	Held reset	3-state	High	standby

Note: TC = Terminal Count = highest address value. TC+1 = address 0.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to +5.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction Temperature	+150	°C

Notes

1: Maximum DC undershoot below GND must be limited to either 0.5V or 10mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200mA.

2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol		Parameter	Min	Max	Units
V_{CCINT}	Commercial	Internal Voltage supply (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Internal Voltage supply (T_A = -40°C to +85°C)	3.0	3.6	V
V_{CCO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCO}	V

Quality and Reliability Characteristics

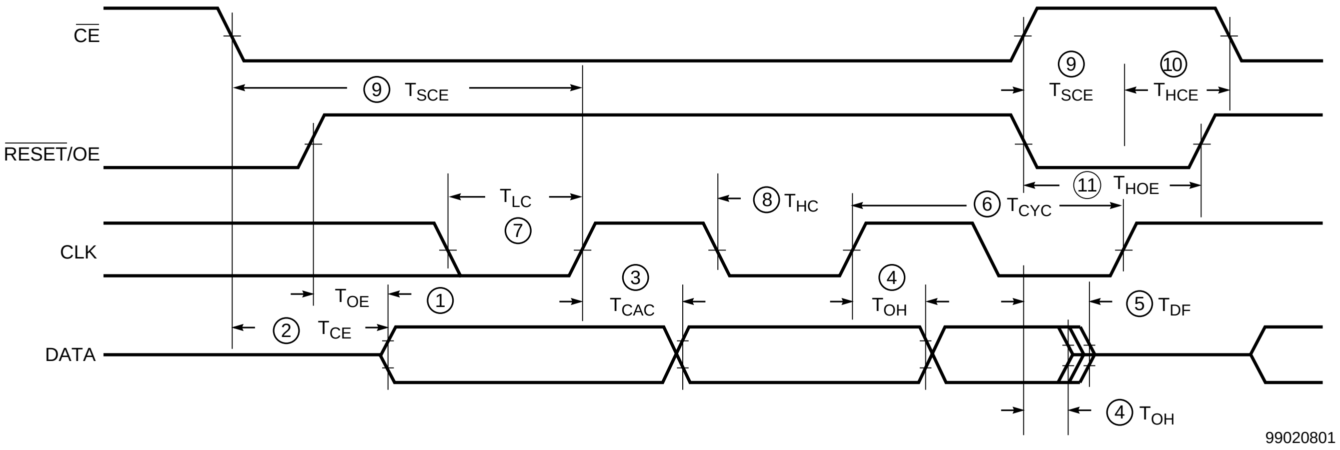
Symbol	Description	Min	Max	Units
t_{DR}	Data Retention	10	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	High-level output voltage for 3.3 V outputs	I_{OH} = -4 mA	2.4		V
	High-level output voltage for 2.5 V outputs	I_{OH} = -500 µA	90% V_{CCO}		V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA		0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA		0.4	V
I_{CCA}	Supply current, active mode	at maximum frequency		30.0	mA
I_{CCS1}	Supply current, standby mode 1			2.0	mA
I_{CCS2*}	Supply current, standby mode 2			300	µA
I_{CCS3**}	Supply current, standby mode 3			100	µA
I_{ILJ}	JTAG pins TMS, TDI, and TDO	$V_{CC\,=}$ MAX V_{IN} = GND	-100		µA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	-10.0	10.0	µA
I_{IH}	Input & Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	-10.0	10.0	µA
C_{IN} & C_{OUT}	Input and Output Capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF

***** 1801/18512/18256/18128 only, cascadable
**1801/18512/18256/18128 only, non-cascadable

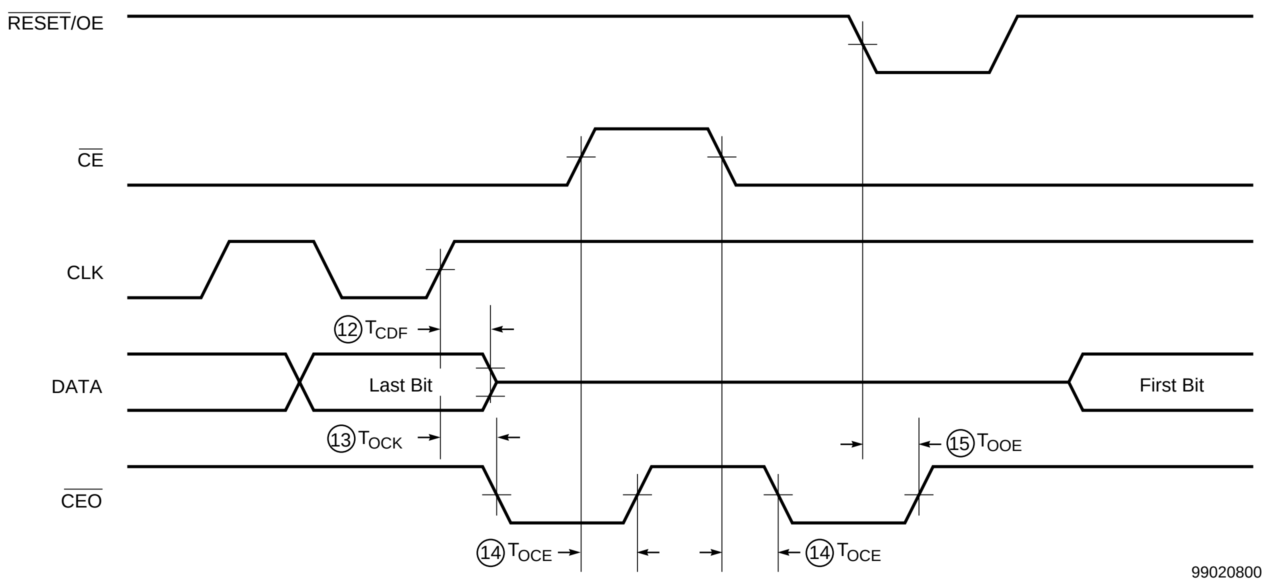
.AC Characteristics Over Operating Conditions



Symbol		Description	Min	Max	Units
1	T_{OE}	OE to Data Delay		30	ns
2	T_{CE}	CE to Data Delay		45	ns
3	T_{CAC}	CLK to Data Delay		45	ns
4	T_{OH}	Data Hold From $\overline{\text{CE}}$, OE, or CLK	0		ns
5	T_{DF}	$\overline{\text{CE}}$ or OE to Data Float Delay[2]		50	ns
6	T_{CYC}	Clock Periods	67		ns
7	T_{LC}	CLK Low Time[3]	25		ns
8	T_{HC}	CLK High Time[3]	25		ns
9	T_{SCE}	$\overline{\text{CE}}$ Setup Time to CLK (to guarantee proper counting)	25		ns
10	T_{HCE}	$\overline{\text{CE}}$ Hold Time to CLK (to guarantee proper counting)	0		ns
11	T_{HOE}	OE Hold Time (guarantees counters are reset)	25		ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

AC Characteristics Over Operating Condition When Cascading



Symbol		Description	Min	Max	Units
12	T_{CDF}	CLK to Data Float Delay[2, 3]		50	ns
13	T_{OCK}	CLK to $\overline{\text{CEO}}$ Delay[3]		30	ns
14	T_{OCE}	CE to $\overline{\text{CEO}}$ Delay[3]		35	ns
15	T_{OOE}	$\overline{\text{RESET}}$/OE to $\overline{\text{CEO}}$ Delay[3]		30	ns

Notes:
1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.
3. Characterized but not 100% tested.
4. All AC parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

Ordering Information

XC1804 VQ44 C

Device Number
XC1804
XC1802
XC1801
XC18512
XC18256
XC18128

Package Type
VQ44=44-Pin Plastic Quad Flat Package
PC44=44-Pin Plastic Chip Carrier
SO20=20-Pin Small-Outline Package
PC20=20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing
C = Commercial (T_A = 0° to +70°C)
I = Industrial (T_A = –40° to +85°C)

Valid Ordering Combinations

XC1804VQ44C	XC1802VQ44C	XC1801SO20C	XC18512SO20C	XC18256SO20C	XC18128SO20C
XC1804PC44C	XC1802PC44C	XC1801PC20C	XC18512PC20C	XC18256PC20C	XC18128PC20C
XC1804VQ44I	XC1802VQ44I	XC1801SO20I	XC18512SO20I	XC18256SO20I	XC18128SO20I
XC1804PC44I	XC1802PC44I	XC1801PC20I	XC18512PC20I	XC18256PC20I	XC18128PC20I

Marking Information

44-Pin Package

XC1804 VQ44 C

Device Number
XC1804
XC1802

Package Type
VQ44=44-Pin Plastic Quad Flat Package
PC44=44-Pin Plastic, Leaded Chip Carrier

Operating Range/Processing
C = Commercial (T_A = 0° to +70°C)
I = Industrial (T_A = –40° to +85°C)

20-Pin Package

1801 S C

Device Number
XC1801
XC18512
XC18256
XC18128

Package Type
S=20-Pin Small-Outline Package
J=20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing
C = Commercial (T_A = 0° to +70°C)
I = Industrial (T_A = –40° to +85°C)

Revision Control

Date	Version	Revision
2/9/99	1.0	First publication of this early access specification
8/23/99	1.1	Edited text, changed marking, added $\overline{\text{CF}}$ and parallel load
9/1/99	1.2	Corrected JTAG order, Security and Endurance data.
9/16/99	1.3	Corrected SelectMAP diagram, control inputs, reset polarity. Added JTAG and $\overline{\text{CF}}$ description, 256 Kbit and 128 Kbit devices.