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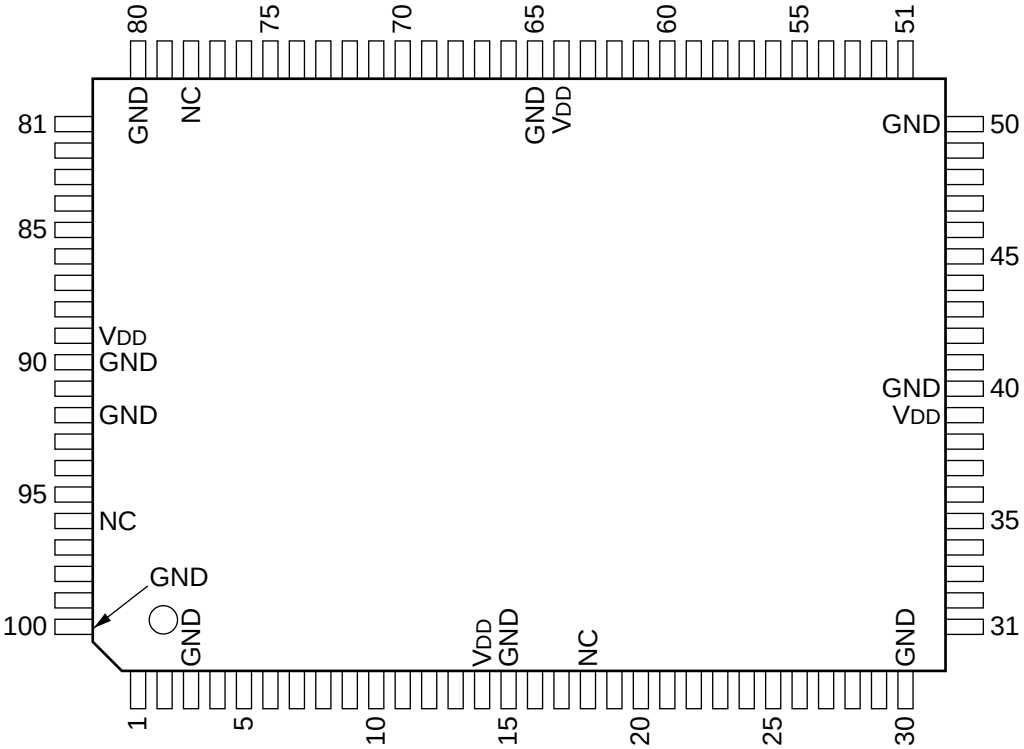
C-MOS ENHANCED MULTI INTERFACE FOR LBP

-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	iRST	21	I	iS0	41	I/O	P1bD4	61	O	BPoFT	81	I	HDiD/C
2	I	iCIS	22	I	iA2	42	I/O	P1bD3	62	O	BPoSE	82	I	HDiRXD
3	—	GND	23	I	iA1	43	I/O	P1bD2	63	I/O	BPbD7	83	I	UTiRXD
4	I/O	bD7	24	I	iA0	44	I/O	P1bD1	64	—	VDD	84	I	UTiDSR
5	I/O	bD6	25	O	HDoINT	45	I/O	P1bD0	65	—	GND	85	I	UTiCTS
6	I/O	bD5	26	O	BPoINT0	46	I/O	P2bD7	66	I/O	BPbD6	86	O	UToTXD
7	I/O	bD4	27	O	UToINT	47	I/O	P2bD6	67	I/O	BPbD5	87	O	UToDTR
8	I/O	bD3	28	O	IOoINT1	48	I/O	P2bD5	68	I/O	BPbD4	88	O	UToRTS
9	I/O	bD2	29	O	IOoINT2	49	I/O	P2bD4	69	I/O	BPbD3	89	—	VDD
10	I/O	bD1	30	—	GND	50	—	GND	70	I/O	BPbD2	90	—	GND
11	I/O	bD0	31	I	UTiECK	51	I/O	P2bD3	71	I/O	BPbD1	91	I	BPiCLK
12	I	iRD/RW	32	I	P3iD1	52	I/O	P2bD2	72	I/O	BPbD0	92	—	GND
13	I	iWR/EN	33	I	P3iD2	53	I/O	P2bD1	73	O	HDoRTS	93	O	BPoRT
14	—	VDD	34	O	BPoINT1	54	I/O	P2bD0	74	O	HDoSYNC	94	I	BPiCLS
15	—	GND	35	O	BPoINT2	55	I	BPiSEI	75	O	HDoTRXC	95	O	BPoDRQ
16	I	iCLK	36	I/O	P1bD7	56	I	BPiAF	76	O	HDoTXD	96	—	NC
17	I	iCS	37	I/O	P1bD6	57	I	BPiSTB	77	O	HDoW/Q	97	O	PBoDEND
18	—	NC	38	I/O	P1bD5	58	O	BPoPE	78	—	NC	98	I	BPiDAK
19	I	iS2	39	—	VDD	59	O	BPoACK	79	I	HDiPCLK	99	I	BPiINI
20	I	iS1	40	—	GND	60	O	BPoBY	80	—	GND	100	—	GND

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INPUT

BPiAF	;	COMPATIBILITY = n AUTO Fd
BPiCLK	;	I/O PARALLEL INTERFACE CLOCK
BPiCLS	;	COMPATIBILITY MODE LEVEL SELET
BPiDAK	;	DMAC ACKNOWLEDGE
BPiINI	;	COMPATIBILITY = n INITIAL
BPiINT	;	COMPATIBILITY = n INT
BPiSEI	;	COMPATIBILITY = n SELECT IN
BPiSTB	;	COMPATIBILITY = n STROBE
HDiD/C	;	HDLC DATA/COMMAND SELECT
HDiPCLK	;	HDLC P CLOCK
HDiRXD	;	HDLC RECEIVE DATA
iA0-iA2	;	ADDRESS
iCIS	;	CPU INTERFACE SELECT
iCLK	;	CLOCK (3.6864 MHz)
iCS	;	CHIP SELECT
iRD/RW	;	READ/READ WRITE SELECT
iRST	;	RESET
iS0-iS2	;	BLOCK SELECT
iWR/EN	;	WRITE/ENABLE
P3iD1, P3iD2	;	EXTERNAL INTERRUPT
UTiCTS	;	UART CTS
UTiDSR	;	UART DATA SET READY
UTiECK	;	EXTERNAL UART CLOCK
UTiRXD	;	UART RECEIVE DATA

OUTPUT

BPoACK	;	COMPATIBILITY = n ACK
BPoBY	;	COMPATIBILITY = BUSY
BPoDEND	;	DMAC END
BPoDRQ	;	DMAC REQUEST
BPoFT	;	COMPATIBILITY = n FAULT
BPoINT0-BPoINT2	;	INTERRUPT REQUEST 0-2
BPoPE	;	COMPATIBILITY = P ERROR
BPoRT	;	INDICATE REVERSE TRANSFER
BPoSE	;	COMPATIBILITY = SELECT
HDoINT	;	HDLC INTERRRUPT
HDoRTS	;	HDLC REQUEST TO SEND
HDoSYNC	;	HDLC SYNC
HDoTRXC	;	HDLC TRANSMIT/RECEIVE CLOCK
HDoTXD	;	HDLC TRANSMIT DATA
HDoW/Q	;	HDLC WAIT/REQUEST
IOoINT1, IOoINT2	;	INTERRUPT
UToDTR	;	UART DATA TERMINAL READY
UToINT	;	UART INTERRUPT
UToRTS	;	UART REQUEST TO SEND
UToTXD	;	UART TRANSMIT DATA

INPUT/OUTPUT

bD0-bD7	;	DATA BUS
BPbD0-BPbD7	;	COMPATIBILITY = DATA
P1bD0-P1bD7	;	PARALLEL PORT1
P2bD0-P2bD7	;	PARALLEL PORT2

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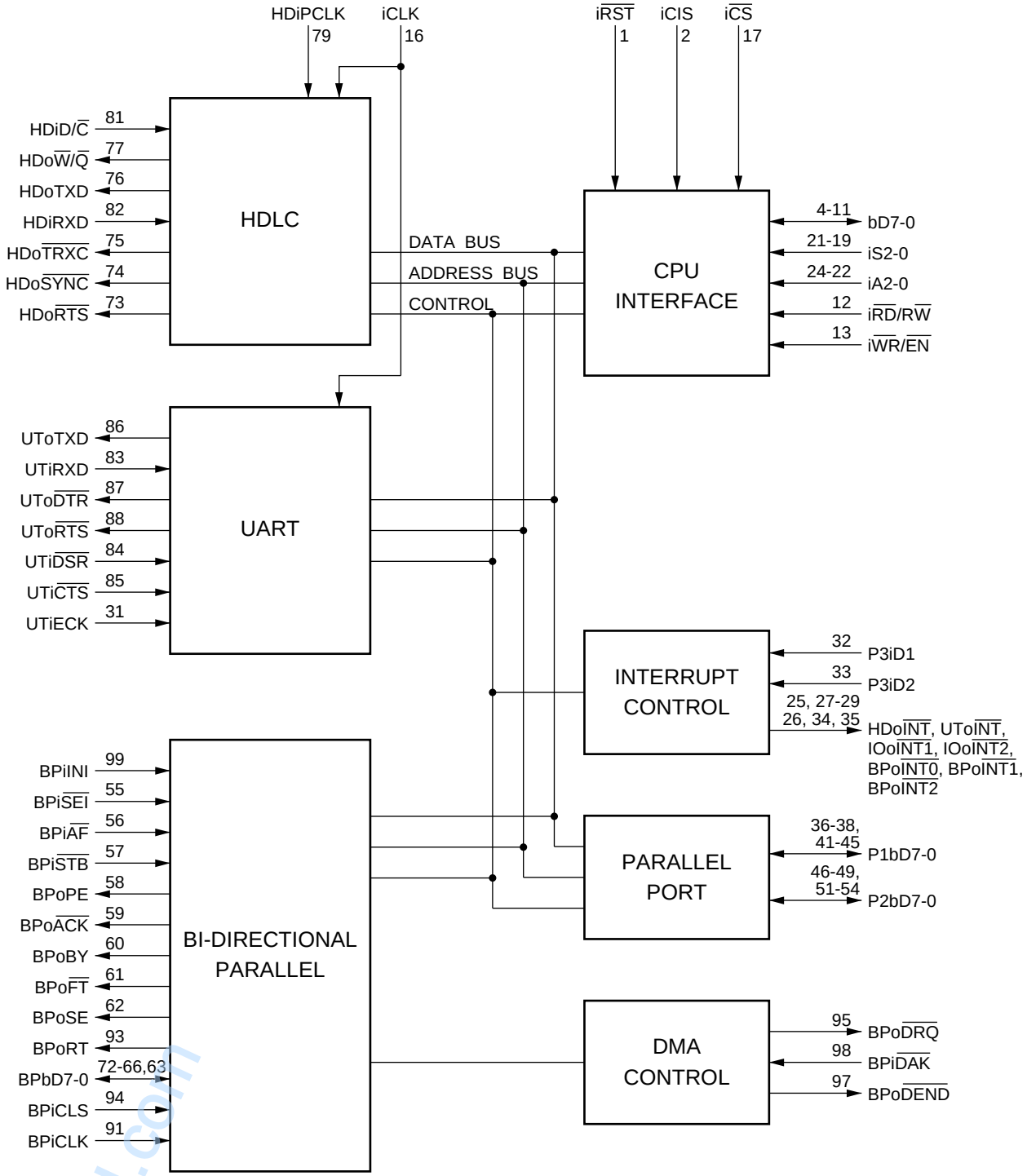

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