13-BIT SERIES-PARALLEL CONVERTER

GENERAL DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

Features

- TTL and CMOS compatible inputs
- Outputs drive load in both directions
- Power-on reset makes outputs floating
- Wide supply voltage range

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,5 to 18	V
Output current, each output	I_{OL}; $-I_{OH}$	max.	80	mA
Clock frequency	f_{CLK}	max.	50	kHz
Operating ambient temperature range	T_{amb}		0 to +80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

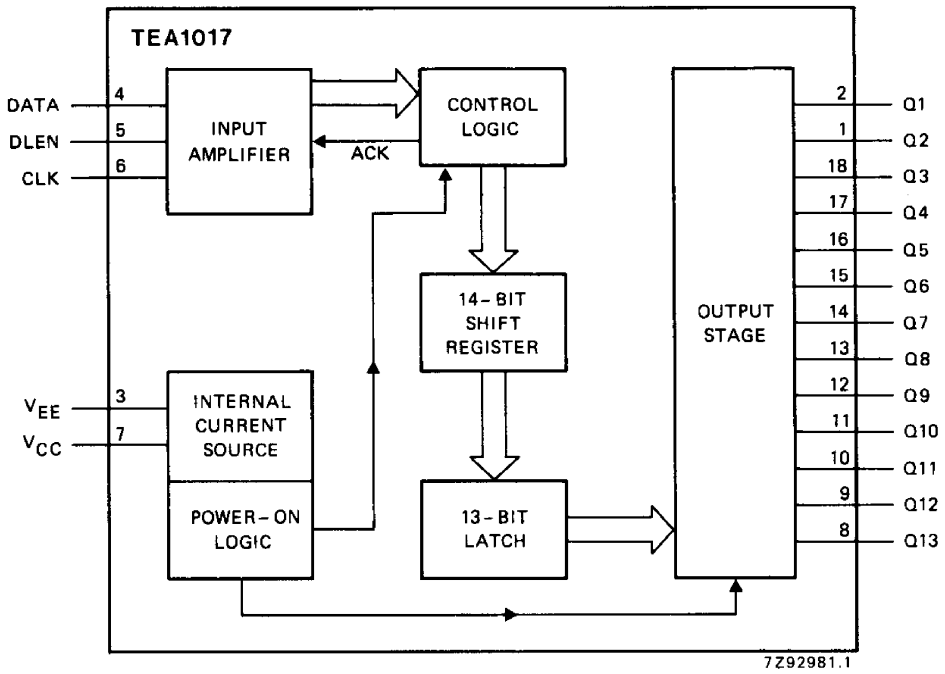

Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The control logic performs a key function in this device. It checks whether the input information has the correct format: a DLEN signal that has been HIGH during 14 clock pulses, and a DATA signal with its first bit LOW.
When the format is found to be correct, the 15th clock pulse makes the control logic generate a signal that loads the content of the first 13 bits of the shift register into 13 latches. These drive the output stages.

"Acknowledge" (pin 4)

After the 15th clock pulse an acknowledge signal drives the DATA pin to LOW. To use this information the DATA should be programmed HIGH and an open collector-device, or a series resistor should be used on the DATA-input. This signal is valid till the next clock pulse, LOW-to-HIGH transition, see Fig. 3.

Supply V_{CC} (pin 7)

The supply current of the TEA1017 is regulated internally. This permits the circuit to be used over a very wide range of supply voltages, viz. 4,5 to 18 V, with little variation of supply current.

The circuit has a power-on reset arrangement that resets the circuit and sets the outputs to a high-impedance state. It requires a rise-time of the supply larger than 3 us/V.

DATA input (pin 4)

The circuit requires input information on the DATA input consisting of 14 bits, the first bit being LOW. This information should be synchronous with the clock pulse.
Data is loaded into the shift register at HIGH-to-LOW transitions of the clock pulse.

Data line enable input DLEN (pin 5)

A HIGH level on the DLEN input enables the shift register. This HIGH level should have a duration of 14 clock pulses (see Fig. 3).
After the DLEN input has returned to LOW the subsequent (15th) clock pulse transfers the contents of the shift register to the latches and then to the outputs.

Clock input CLK (pin 6)

The shift register shifts at the HIGH to LOW transitions of the clock pulse. The clock signal may be a continuously running clock or a clock burst of 15 clock pulses.

Outputs Q1 to Q13

The outputs are capable of supplying a load current in both directions, i.e. they can drive a load to the supply (V_{CC}) or to ground (V_{EE}).

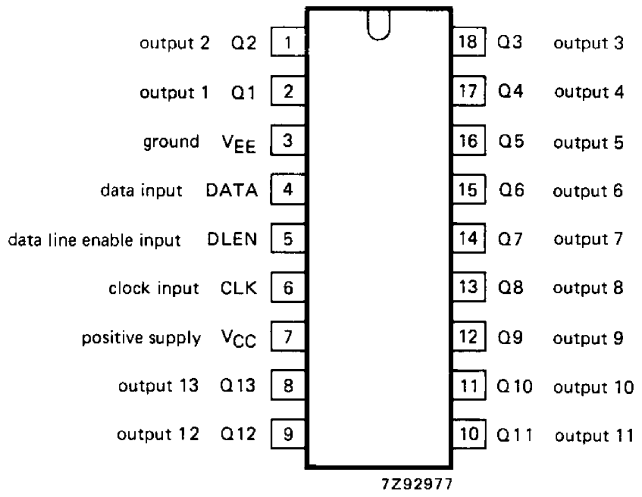

Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	18 V
Input voltage range, all inputs	V_I	−0,3 to V_{CC} +0,3	V
Output current, all outputs			
HIGH	$-I_{OH}$	max.	150 mA
LOW	I_{OL}	max.	150 mA
Total power dissipation *	P_{tot}	max.	1,4 W
Storage temperature range	T_{stg}	−40 to +150	°C
Operating ambient temperature range	T_{amb}	0 to + 80	°C

* See Fig. 4.

CHARACTERISTICS

V_{CC} = 4,5 to 18 V; V_{EE} = 0 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply current					
during normal operation, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	45	60	mA
at V_{CC} = 18 V	I_{CC}	–	50	70	mA
during power-on blanking, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	1,5	2	mA
at V_{CC} = 18 V	I_{CC}	–	5	7	mA
Supply voltage rise time to ensure power on reset		3	–	–	μs/V
Clock input CLK (pin 6)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{CLKH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{CLKL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Clock pulse duration					
HIGH	t_{WH}	8	–	–	μs
LOW	t_{WL}	10	–	–	μs
DATA input (pin 4)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{IH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{IL} = 0,4 V	$-I_{IL}$	–	–	10	μA
DATA input in sink current					
ACK = TRUE	I_{DACK}	1	–	–	mA
Data line enable input DLEN (pin 5)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{5-3} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{5-3} = 0,4 V	$-I_{IL}$	–	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs Q1 to Q13					
Output voltage during normal operation					
HIGH at $-I_{OH}$ = 80 mA	V_{OH}	$V_{CC}-1,5$	–	–	V
LOW at I_{OL} = 80 mA	V_{OL}	–	–	1	V
Output current during power-on reset					
HIGH	$-I_{OH}$	–	–	10	μA
LOW	I_{OL}	–	–	10	μA
Rise and fall times: no maximum					
Minimum times as V_{CC} = 4,5 volts (see Fig. 3)					
Set-up time ENABLE	t_{SUDL}	2,8	–	–	μs
Hold time ENABLE	t_{HDL}	5,0	–	–	μs
Set-up time DATA	t_{SDA}	0	–	–	μs
Hold time DATA	t_{HDA}	2,8	–	–	μs
Set-up time LOAD	t_{SLO}	1,4	–	–	μs
Pulse width LOW	t_{WL}	10	–	–	μs
Pulse width HIGH	t_{WH}	8	–	–	μs
Max. clock input frequency = $1/(t_{WH} + t_{WL})$	f_{max}	–	–	50	kHz
Propagation delay					
clock to outputs	t_{PCQ}	–	–	8,5	μs
acknowledge	t_{PCA}	–	–	6	μs
acknowledge release	t_{PCAR}	–	–	6	μs

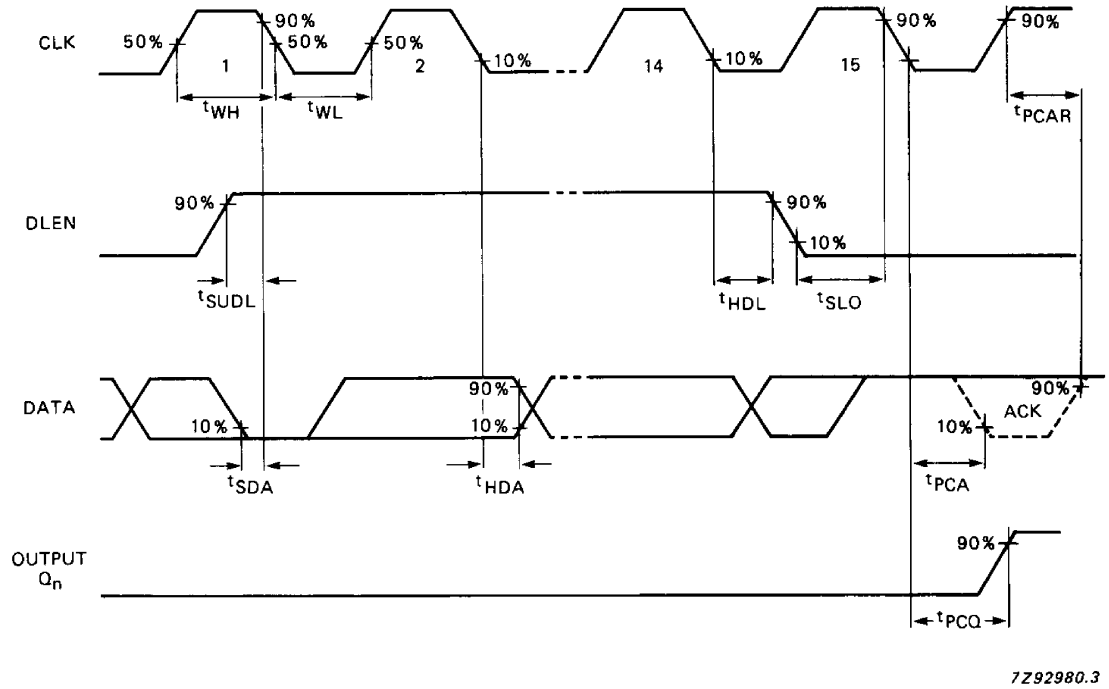

Fig. 3 Bus timing characteristics.

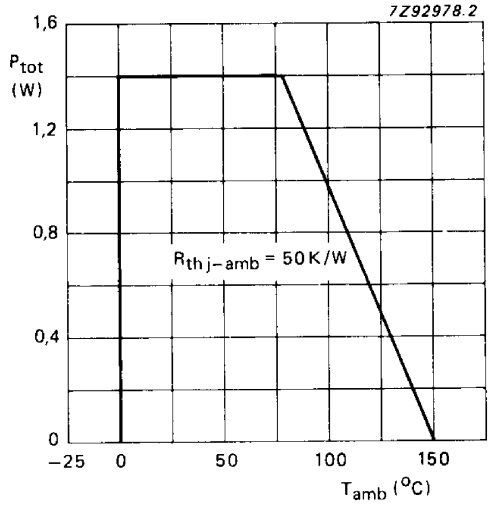

Fig. 4 Derating curve.

APPLICATION INFORMATION

1. From the buffer-capacitors C1 of the power supply the supply connections to the TEA1017 and the loads should be separated. An extra capacitor of 10 μF with good high-frequency characteristics should be mounted across the V_{CC} and V_{EE} connections as close as possible to the TEA1017.
2. If no use is made of the acknowledge information it is advised to program the data-output from the controller to LOW during the time ACK is valid. To use the acknowledge information the data-output has to be programmed HIGH. When a push-pull controller device is used a series resistor has to be connected in the data-line between the controller and TEA1017.
   The ACK may be sensed on the TEA1017-side of this resistor. See Fig. 5.

Note. ACK is removed from the data-line after the next LOW-to-HIGH transition of the clock-line with a maximum delay of 6 μs. (t_{PCA} maximum).

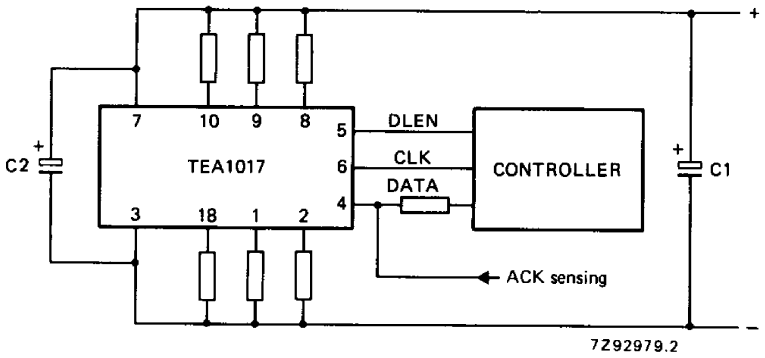

Fig. 5 TEA1017 with 3 loads to V_{CC} Q = 0 and 3 loads to V_{EE} Q = 1.