TEA1530T/AT/AP

GreenChip II SMPS control IC

Rev. 01 — 30 June 2008 Product data sheet

1. General description

The GreenChip II is the second generation of green Switched Mode Power Supply (SMPS) controller ICs. Its high level of integration allows the design of a cost effective power supply with a very low number of external components.

The TEA1530(A) (TEA1530T, TEA1530AT and TEA1530AP) can be used in fixed frequency converter designs for low voltage, high current applications. At low power (standby) levels, the system operates in cycle skipping mode which minimizes the switching losses during standby.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. A second low voltage BICMOS IC is used for accurate, high speed protection functions and control.

The TEA1530(A) enables highly efficient and reliable supplies to be designed easily.

2. Features

2.1 Distinctive features

- Universal mains supply operation, 70 VAC to 276 VAC.
- High level of integration, resulting in a very low external component count.
- Fixed frequency operation.

2.2 Green features

- Cycle skipping mode at very low loads; input power < 300 mW at no-load operation for a typical adapter application.
- On-chip start-up current source.

2.3 Protection features

- Safe restart mode for system fault conditions.
- Undervoltage protection (foldback during overload).
- IC OverTemperature Protection (OTP) (latched).
- Low and adjustable OverCurrent Protection (OCP) trip level.
- Soft (re)start.
- Mains voltage-dependent operation-enabling level.
- TEA1530AT and TEA1530AP: General purpose input for latched or safe restart protection and timing, e.g. to be used for OverVoltage Protection (OVP), output short circuit protection or system OTP.

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- TEA1530T: General purpose input for latched protection and timing, e.g. to be used for OVP, output short circuit protection or system OTP.

3. Applications

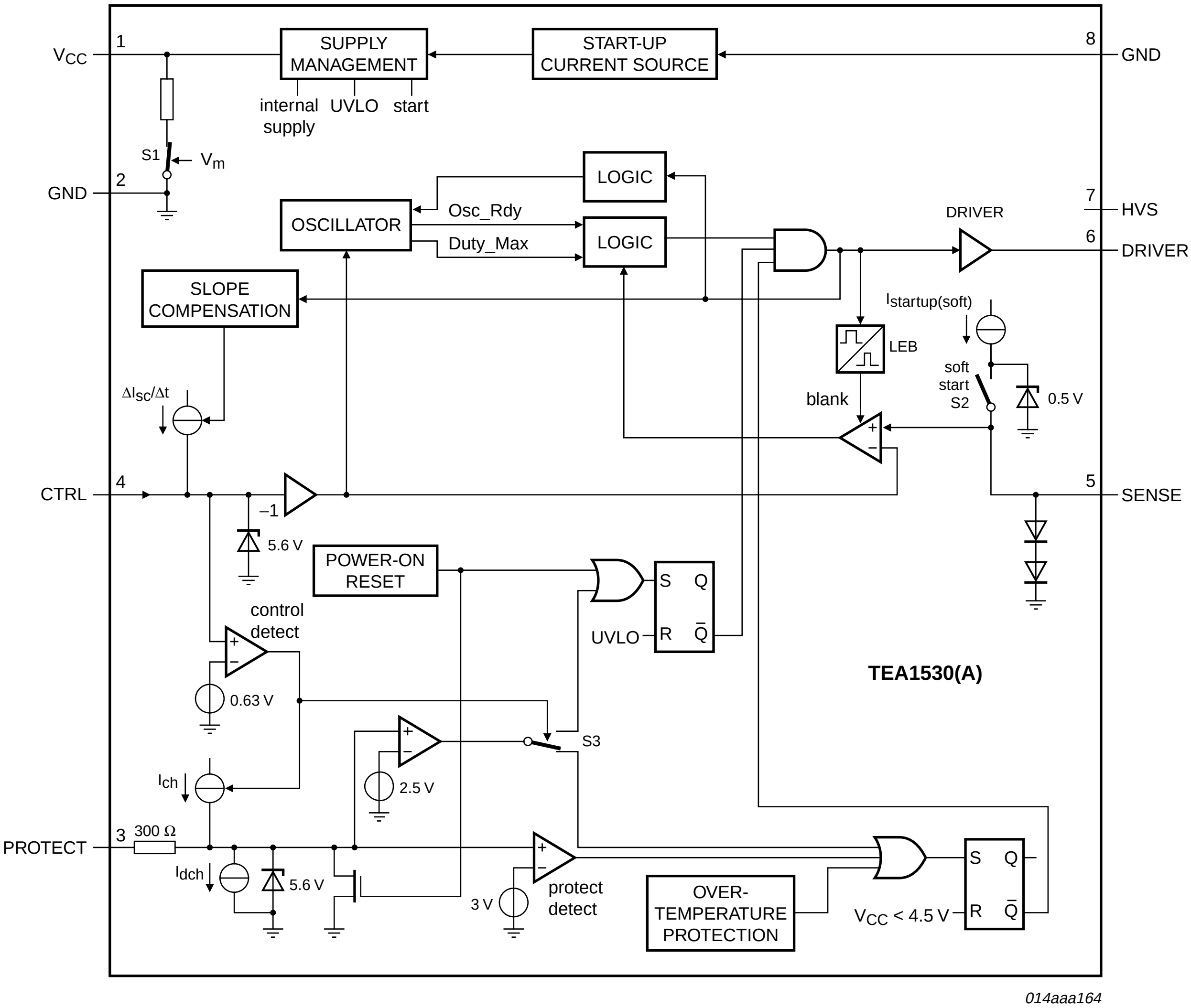
- Printer & LCD adapters / chargers / supplies. The device can, however, also be used in all applications that demand an efficient and cost-effective solution up to 65 W.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
TEA1530T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TEA1530AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TEA1530AP	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

5. Block diagram



(1) Switch S3 is not controlled in TEA1530T, it is fixed as drawn.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

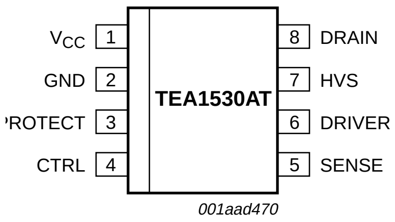


Fig 2. Pin configuration: TEA1530T, TEA1530AT (SOT96-1), TEA1530AP (SOT97-1)

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
PROTECT	3	protection and timing input
CTRL	4	control input
SENSE	5	programmable current sense input
DRIVER	6	MOSFET gate driver output
HVS	7	High voltage spacer
DRAIN	8	High voltage rectified mains input for start-up current

7. Functional description

The TEA1530(A) is the controller of a compact flyback converter, with the IC situated at the primary side. An auxiliary winding of the transformer powers the IC after start-up; see Figure 3.

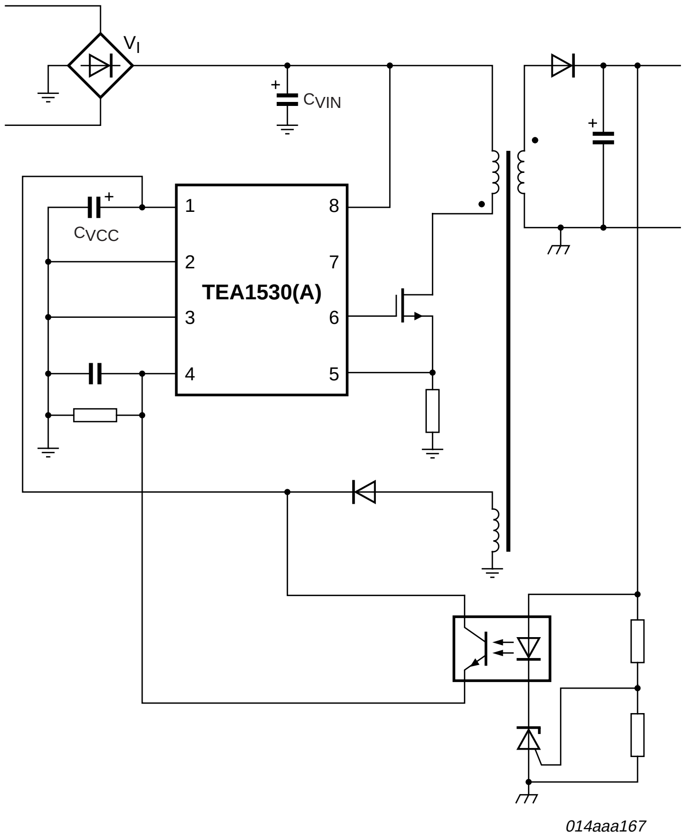


Fig 3. Typical configuration

The TEA1530(A) can operate in multi modes; see Figure 4.

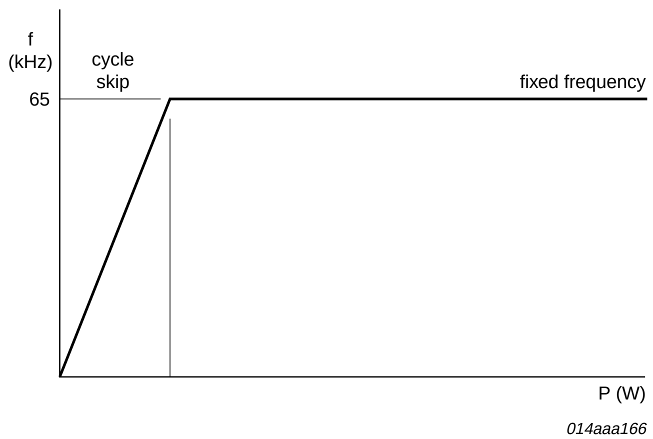


Fig 4. Cycle skip and FF-CCM operation

Because of the fixed frequency mode, the internal oscillator determines the start of the next converter stroke.

A cycle skipping mode is activated at very low power (standby) levels.

7.1 Start-up, mains enabling operation level and undervoltage lockout

Refer to Figure 8 and Figure 9. Initially, the IC is self supplying from the rectified mains voltage via pin DRAIN. The supply capacitor C_{VCC} (at pin 1) is charged by the internal start-up current source to a level of about 4 V or higher, depending on the drain voltage. Once the drain voltage exceeds the $V_{mains(oper)(en)}$ (mains-dependent operation-enabling level), the start-up current source will continue charging capacitor C_{VCC} (switch S1 will be opened), see Figure 1. The IC activates the power converter as soon as the voltage on pin V_{CC} passes the $V_{startup}$ level. At this moment the IC supply from the high voltage pin is stopped (green function). The IC supply is taken over by the auxiliary winding of the flyback converter.

The moment the voltage on pin V_{CC} drops below $V_{th(UVLO)}$ (undervoltage lockout), the IC stops switching and performs a safe restart from the rectified mains voltage. In the safe restart mode the driver output is disabled and the voltage on pin V_{CC} is recharged via the pin DRAIN.

7.2 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

7.3 Current control mode

Current control mode is used for its good line regulation behavior.

The primary current is sensed across an external resistor and compared with the internal control voltage. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the voltage on the external pin CTRL with an offset of 1.5 V. This means that a voltage range from 1 V to approximately 1.5 V on pin CTRL will result in a pin SENSE voltage range from 0.52 V to 25 mV (a high external control voltage results in a low duty cycle).

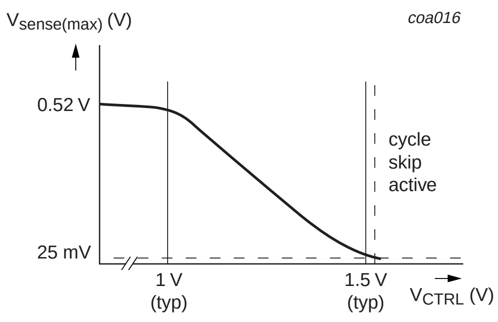


Fig 5. The $V_{sense(max)}$ voltage as a function of V_{CTRL}

7.4 Oscillator

The fixed frequency of the oscillator is set by an internal current source and capacitor.

7.5 Cycle skipping

At very low power levels, a cycle skipping mode activates. An internal control voltage ($V_{sense(max)}$) lower than 25 mV will inhibit switch-on of the external power MOSFET until this voltage increases to a higher value; see Figure 5.

7.6 Continuous Conduction Mode (CCM)

The IC operates in Fixed Frequency Continuous Conduction Mode (FF CCM). Pin DRAIN should be connected to the high voltage rectified mains V_I; see Figure 8.

7.7 OverCurrent Protection (OCP)

The primary peak current in the transformer is measured accurately cycle-by-cycle using the external sense resistor R_{sense}. The OCP circuit limits the voltage on pin SENSE to an internal level equal to 1.5 V – V_{CTRL} (see also Section 7.3). The OCP detection is suppressed during the leading edge blanking period, t_{leb} to prevent false triggering caused by the switch-on spikes.

7.8 Control pin protection

If pin CTRL becomes open-circuit or is disconnected, a fault condition is assumed and the converter will stop switching immediately. Operation recommences when the fault condition is removed.

7.9 Adjustable slope compensation

A slope compensation function has been added at pin CTRL; see Figure 6. The slope compensation function prevents subharmonic oscillation in CCM at duty cycles over 50 %. The CTRL voltage is modulated by sourcing a (non-constant) current out of pin CTRL and by adding externally a series resistor $R_{slopecomp}$. This increases the CTRL voltage proportionally with the on-time, which therefore limits the OCP level. A longer on-time results in a higher CTRL voltage, this increase in CTRL voltage will decrease the on-time. Slope compensation can be adjusted by changing the value of $R_{slopecomp}$. Slope compensation prevents modulation of the on-time (duty cycle) while operating in FF CCM. A possible drawback of subharmonic oscillation can be output voltage ripple.

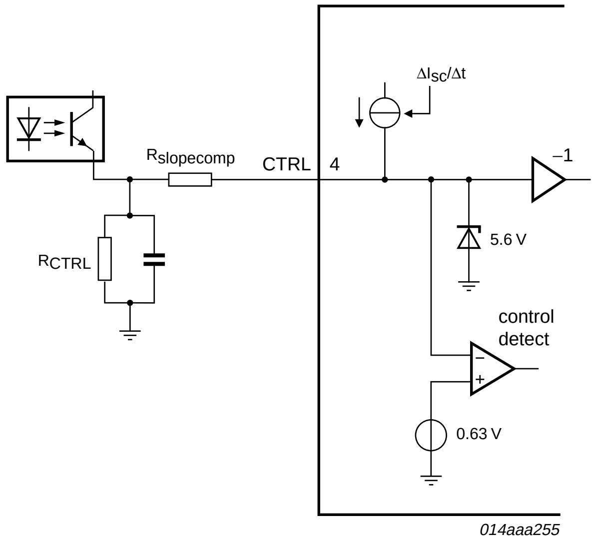


Fig 6. Slope compensation

7.10 Minimum and maximum on-time

The minimum on-time of the SMPS is determined by the LEB time (typically 400 ns). The IC limits the maximum on-time by limiting the driver duty cycle to 70 %. So the maximum on-time is correlated to the oscillator time which results in an accurate limit of the minimum input voltage of the flyback converter.

7.11 PROTECT and timing input

The PROTECT input (pin 3) is a multipurpose, high-impedance input, which can be used to switch off the IC and create a relatively long timing function. As soon as the voltage on this pin rises above 2.5 V, switching stops immediately. For the timing function, a current of typically 50 μA flows out of pin PROTECT and charges an external capacitor until the activation level of 2.5 V is reached. This current source is only activated when the converter is not in regulation, which is detected by the voltage on pin CTRL (V_{CTRL} < 0.63 V). A (small) discharge current is also implemented to ensure that the capacitor is not charged, for example, by spikes. An internal MOSFET switch is added to discharge the external capacitor and ensures a defined start situation. For the TEA1530AP and TEA1530AT the voltage on pin CTRL determines whether the IC enters latched protection mode or safe restart protection mode:

- When the voltage on pin CTRL is below 0.63 V, the IC is assumed to be out of regulation (e.g. the control loop is open). In this case activating pin PROTECT ($V_{PROTECT}$ > 2.5 V) will cause the converter to stop switching. Once V_{CC} drops below $V_{th(UVLO)}$, capacitor C_{VCC} will be recharged and the supply will restart. This cycle will be repeated until the fault condition is removed (safe restart mode).
- When the voltage on pin CTRL is above 0.63 V, the output is assumed to be in regulation. In this case activating pin PROTECT ($V_{PROTECT}$ > 2.5 V), by external means, will activate the latch protection of the IC. The voltage on pin V_{CC} will cycle between $V_{startup}$ and $V_{th(UVLO)}$, but the IC will not start switching again until the latch

protection is reset. The latch is reset as soon as V_{CC} drops below 4.5 V (typical value) (this only occurs when the mains has been disconnected). The internal overtemperature protection will also trigger this latch; see also Figure 1.

For the TEA1530T the IC always enters the latched mode protection independent of the voltage on pin CTRL.

A voltage higher than 3 V on pin PROTECT will always latch the IC. This is independent of the state of the IC.

7.12 OverTemperature Protection (OTP)

The IC provides accurate OTP. The IC stops switching when the junction temperature exceeds the thermal shutdown temperature. When V_{CC} drops to $V_{th(UVLO)}$, capacitor C_{VCC} is recharged to the $V_{startup}$ level, however, switching will not restart. Subsequently, V_{CC} will drop again to $V_{th(UVLO)}$.

Operation only recommences when V_{CC} drops below a level of about 4.5 V, typically when the mains voltage is disconnected for a short period.

7.13 Soft start-up (pin SENSE)

To prevent transformer rattle at start-up or during hiccup, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin SENSE (pin 5) and sense resistor R_{sense}. An internal current source charges the capacitor to $V_{SENSE} = I_{startup(soft)} \times R_{ss}$ (about 0.5 V maximum).

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{ss} and C_{ss}.

$$I_{DM} = \frac{V_{sense(max)} - (I_{\mathrm{startup(soft)}} \times R_{\mathrm{ss}})}{R_{\mathrm{sense}}}$$

$$\tau = R_{\mathrm{ss}} \times C_{ss}$$

The charging current $I_{startup(soft)}$ will flow as long as the voltage on pin SENSE is below approximately 0.5 V. If the voltage on pin SENSE exceeds 0.5 V, the soft start current source will start limiting current $I_{startup(soft)}$. At $V_{startup}$, the $I_{startup(soft)}$ current source is completely switched off, see Figure 7.

Since the soft start current $I_{startup(soft)}$ is supplied from pin DRAIN, the R_{ss} value will not affect V_{CC} current during start-up.

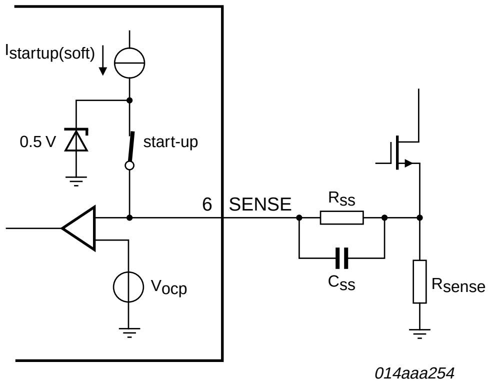


Fig 7. Soft start-up

7.14 Driver

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 150 mA and a current sink capability of typically, 500 mA at V_{CC} = 9.5 V. At V_{CC} = 15 V, the current sourcing capability is typically 250 mA and the current sink capability typically 0.7 A. This permits fast turning on and off of the power MOSFET for efficient operation.

A low driver source current has been chosen to limit the ΔV/Δt at switch-on. This reduces ElectroMagnetic Interference (EMI) and also limits the current spikes across R_{sense}.

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	continuous	–0.4	+20	V
$V_{PROTECT}$	voltage on pin PROTECT	continuous	–0.4	+5	V
V_{CTRL}	voltage on pin CTRL		–0.4	+5	V
V_{SENSE}	voltage on pin SENSE	current limited	–0.4	-	V
V_{DRAIN}	voltage on pin DRAIN		–0.4	+650	V
Currents					
I_{CTRL}	current on pin CTRL	d < 10 %	-	50	mA
I_{SENSE}	current on pin SENSE		–1	+10	mA
I_{DRIVER}	current on pin DRIVER	d < 10 %	–0.8	+2	A
I_{DRAIN}	current on pin DRAIN		-	5	mA

Table 3: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
General						
P_{tot}	total power dissipation	T_{amb} < 70 °C				
		SO8 package		-	0.5	W
		DIP8 package		-	0.75	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–20	+145	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model				
		pins 1 to 6	[1]	-	2000	V
		pin 8 (DRAIN)	[1]	-	1500	V
		machine model	[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient.	in free air, SO8 package.	150	K/W
		in free air, DIP8 package	95	K/W

10. Characteristics

Table 5: Characteristics

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin DRAIN)						
I_{DRAIN}	current on pin DRAIN	V_{DRAIN} > 100 V				
		V_{CC} = 0 V	1.0	1.2	1.4	mA
		with auxiliary supply	-	100	300	µA
V_{BR}	breakdown voltage		650	-	-	V
$V_{mains(oper)(en)}$	mains-dependent operation-enabling voltage		60	-	100	V
Supply voltage management (pin V_{CC})						
$V_{startup}$	start-up voltage		10.3	11	11.7	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		8.1	8.7	9.3	V

Table 5: Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	2.0	2.3	2.6	V
$I_{ch(high)}$	high charging current	V_{DRAIN} > 100 V; V_{CC} < 3 V	–1.2	–1	–0.8	mA
$I_{ch(low)}$	low charging current	V_{DRAIN} > 100 V; 3 V < V_{CC} < $V_{th(UVLO)}$	–1.2	–0.75	–0.45	mA
$I_{restart}$	restart current	V_{DRAIN} > 100 V; $V_{th(UVLO)}$ < V_{CC} < $V_{startup}$	–650	–550	–450	µA
$I_{CC(oper)}$	operating supply current	no load on pin DRIVER	1.1	1.3	1.5	mA
Pulse width modulator						
$t_{on(min)}$	minimum on-time		-	t_{leb}	-	ns
$t_{on(max)}$	maximum on-time		20	25	30	µs
δ_{max}	maximum duty cycle		67	70	73	%
Oscillator						
f_{osc}	oscillator frequency	V_{CTRL} < 1 V	50	63	75	kHz
Duty cycle control (pin CTRL)						
$V_{min(\delta max)}$	minimum voltage (maximum duty cycle)		-	1.0	-	V
$V_{max(\delta min)}$	maximum voltage (minimum duty cycle)		-	1.5	-	V
$\Delta I_{sc}/\Delta t$	slope compensation current		–1.2	–1	–0.8	µA/µs
$V_{CTRL(detect)}$	detection voltage on pin CTRL		0.56	0.63	0.70	V
Protection and timing input (pin PROTECT)						
V_{trip}	trip voltage	[1]	2.37	2.5	2.63	V
$V_{trip(latch)}$	latch trip voltage		2.85	3	3.15	V
$V_{VCC(latch)(reset)}$	latch reset voltage on pin V_{CC}	$V_{CC(latch)}$ < 2.3 V	-	4.5	-	V
I_{ch}	charge current	V_{CTRL} < 0.63 V	–57	–50	–43	µA
I_{dch}	discharge current		-	100	-	nA
Overcurrent and winding short circuit protection (pin SENSE)						
$V_{sense(max)}$	maximum sense voltage	$\Delta V/\Delta t$ = 0.1 V/µs	0.48	0.52	0.56	V
t_{PD}	propagation delay	$\Delta V/\Delta t$ = 0.5 V/µs	-	140	185	ns
t_{leb}	leading edge blanking time		330	400	470	ns
$I_{startup(soft)}$	soft startup current	V_I < 0.5 V	45	60	75	µA
Driver (pin DRIVER)						
I_{source}	source current	V_{CC} = 9.5 V; V_{DRIVER} = 2 V	-	–150	–88	mA
I_{sink}	sink current	V_{CC} = 9.5 V				
		V_{DRIVER} = 2 V	-	250	-	mA
		V_{DRIVER} = 9.5 V	300	500	-	mA
$V_{o(max)}$	maximum output voltage	V_{CC} > 12 V	-	11.5	12	V

Table 5: Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature protection						
$T_{pl(max)}$	maximum protection level temperature		130	140	150	°C
$T_{pl(hys)}$	protection level hysteresis temperature	[2]	-	8	-	°C

[1] TEA1530AT and TEA1530AP: safe restart; TEA1530T: latch.

[2] Valid for V_{CC} > 2 V.

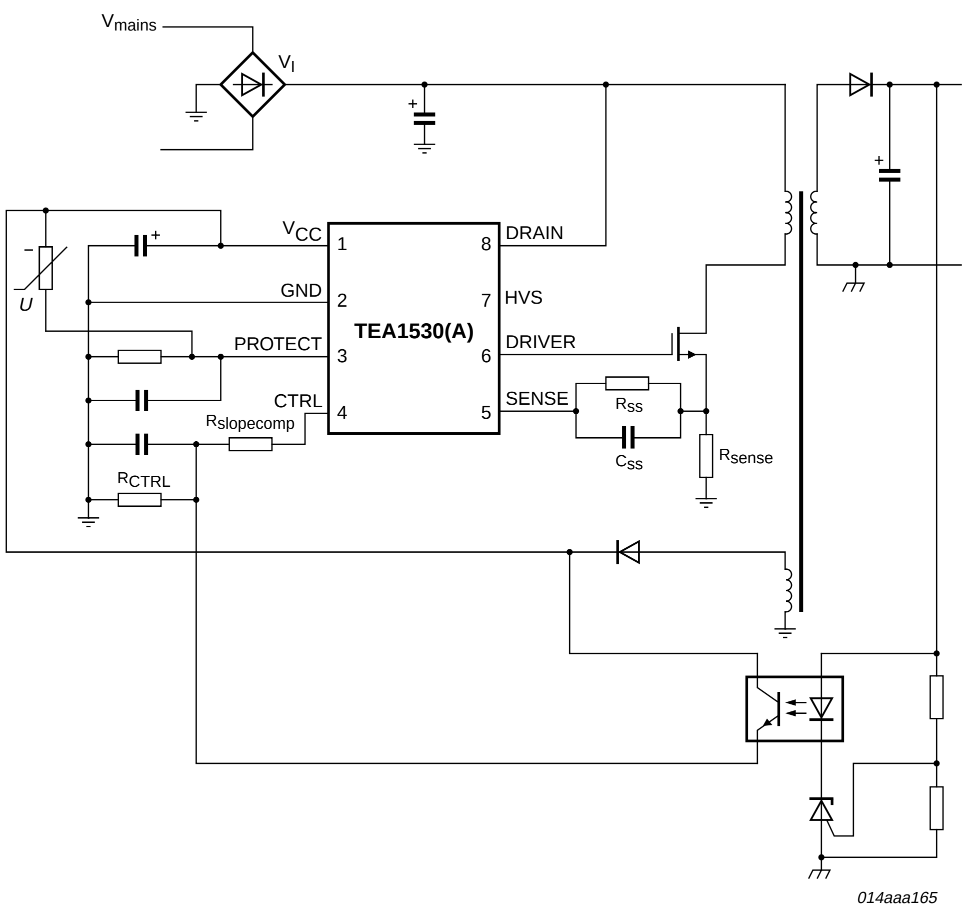
11. Application information

A converter with the TEA1530(A) consists of an input filter, a transformer with a third winding (auxiliary), and an output stage with a feedback circuit.

Capacitor C_{VCC} buffers the IC supply voltage, which is powered via the internal current source, that is connected to the rectified mains, during start-up and via the auxiliary winding during operation.

A sense resistor R_{sense} converts the primary current into a voltage at pin SENSE. The value of R_{sense} defines the maximum primary peak current.

Figure 8 shows a typical CCM flyback configuration. Pin PROTECT is used in this example for external overtemperature protection and open loop or output short circuit protection.



(1) Pin PROTECT is used in this example for external OTP and open loop or output short circuit protection. Slope compensation is determined by the value of $R_{slopecomp}$.

Fig 8. Flyback configuration using CCM

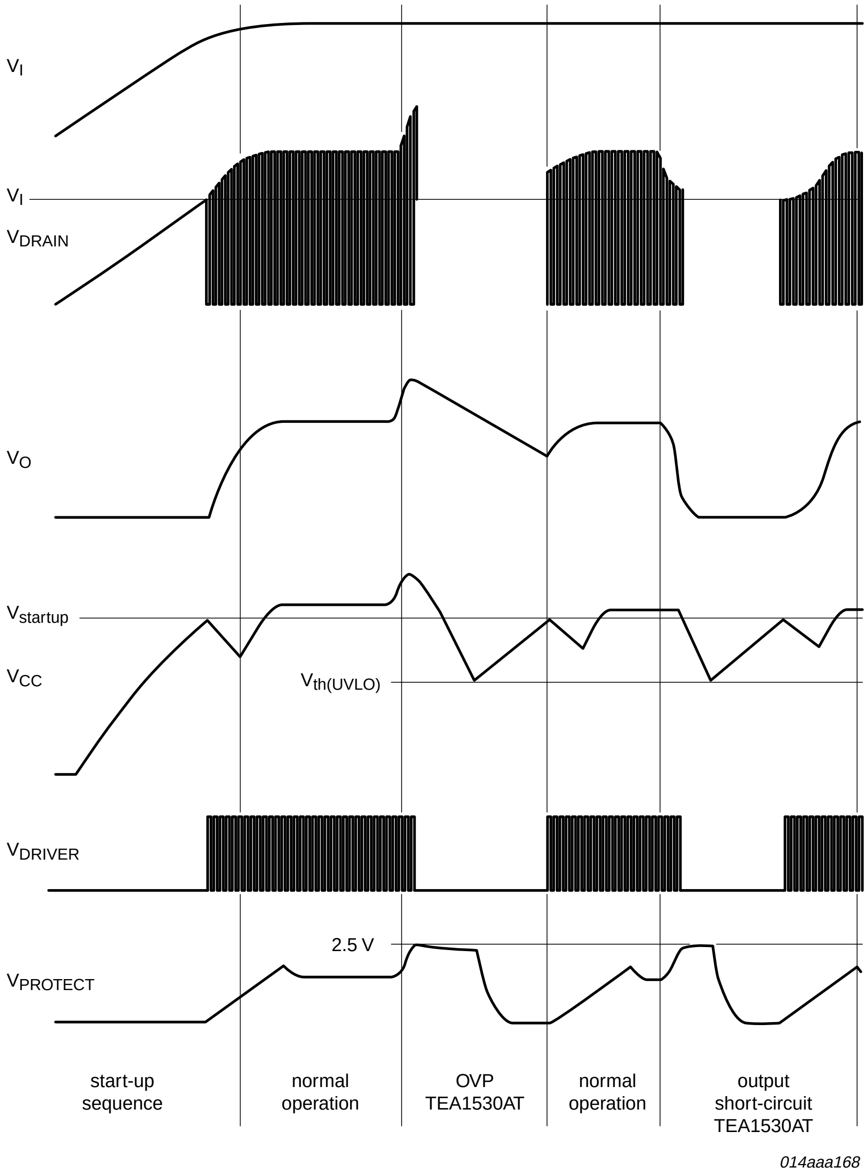
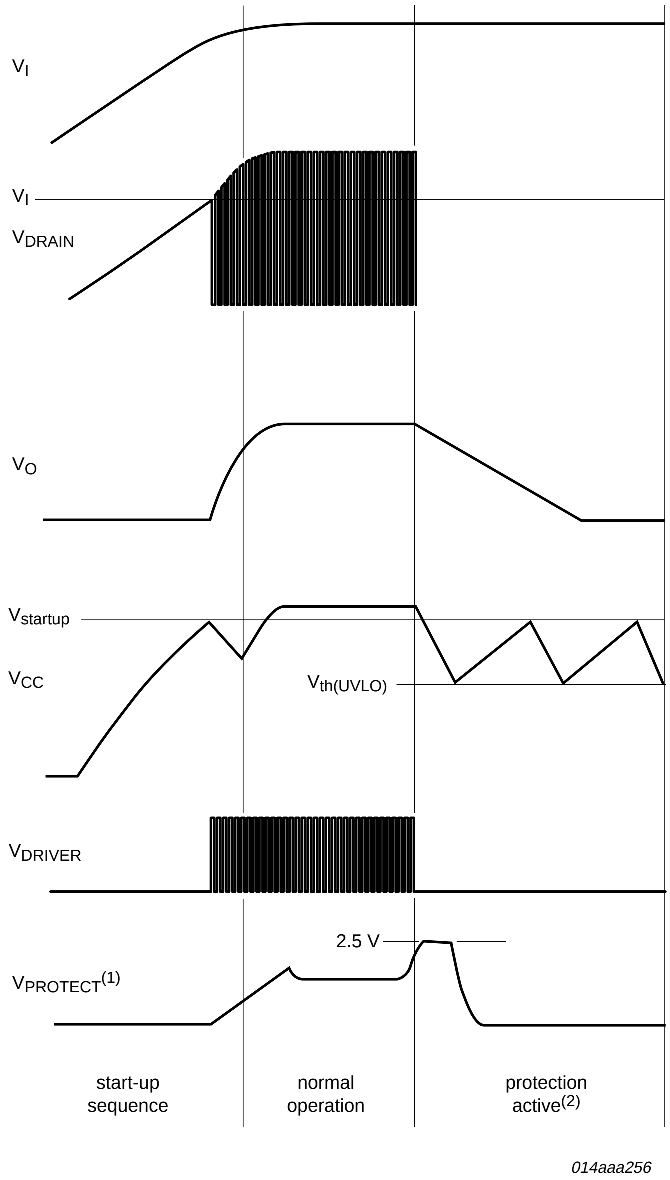


Fig 9. Typical waveforms 1



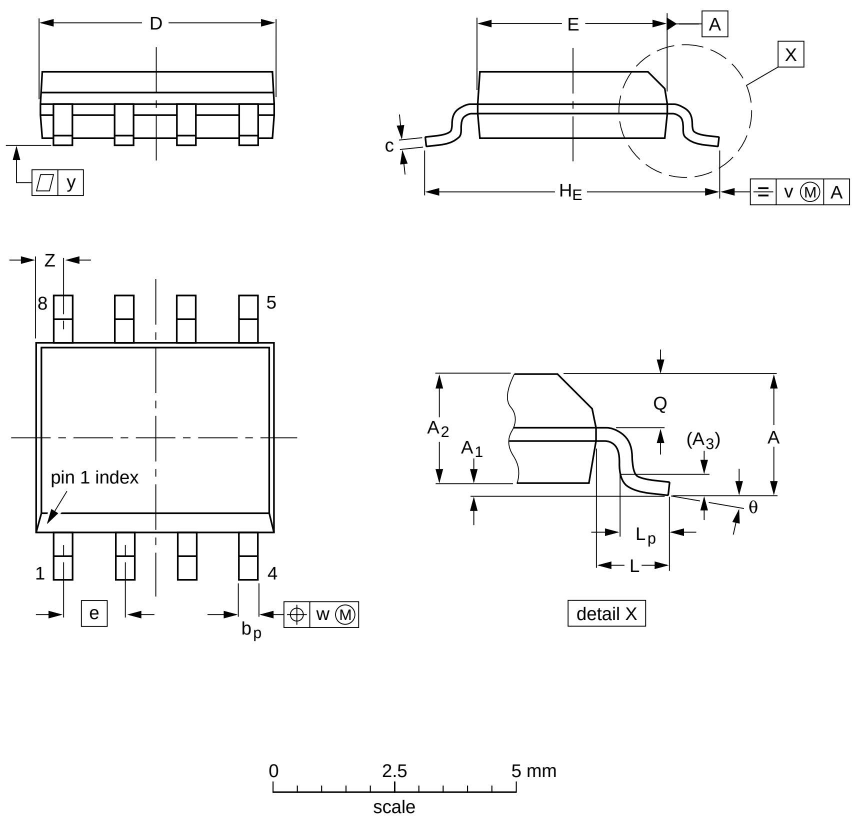
(1) When $V_{PROTECT}$ is forced above 3 V, the protection is always latched. So the IC is not started at $V_{startup}$ unless the V_{CC} voltage drops below the $V_{VCC(latch)(reset)}$ level. This is the same action used for external OTP compensation described in Section 7.12.

(2) External OTP for TEA1530(A); OVP and output short circuit for TEA1530T.

Fig 10. Typical waveforms 2

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

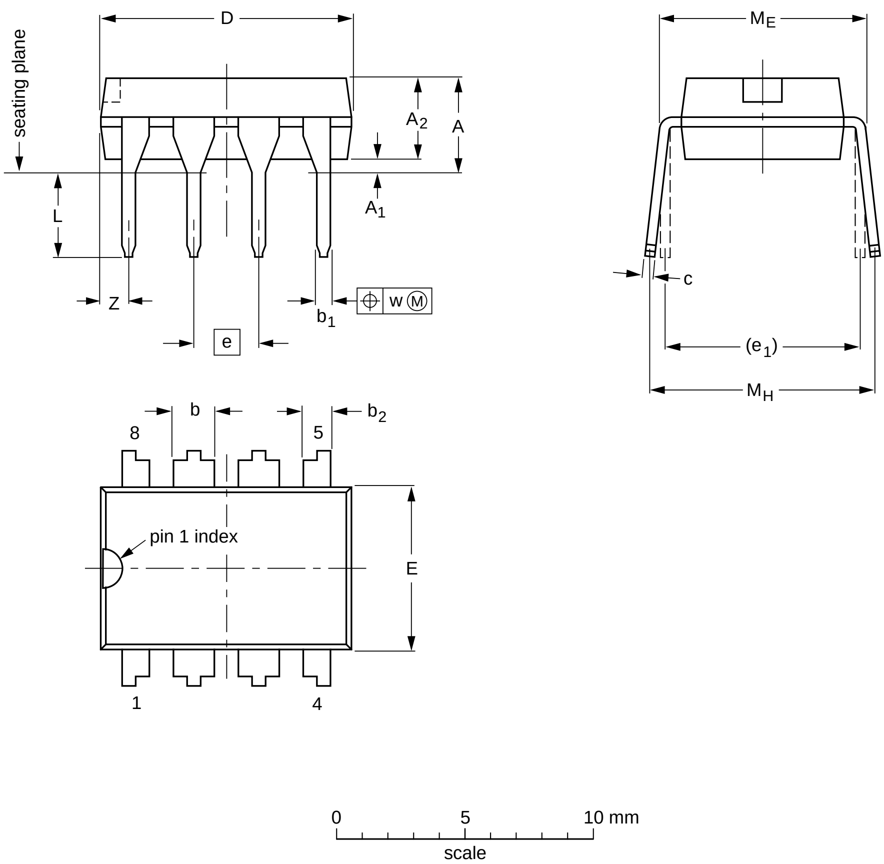
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT96-1 (SO8)

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 12. Package outline SOT97-1 (DIP8)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1530T_AT_AP_1	20080630	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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