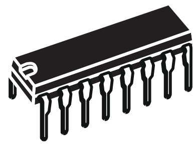
TEA2025

Stereo audio amplifier

Datasheet — production data

Features

- Dual or bridge connection modes
- Few external components
- Supply voltage 3 V to 15 V
- High channel separation
- Very low switch-on/off noise
- Max gain of 45 dB with adjustable external resistor
- Soft clipping
- Thermal protection
- $P_O = 2 \cdot 1$ W, $V_S = 6$ V, $R_L = 4\ \Omega$
- $P_O = 2 \cdot 2.3$ W, $V_S = 9$ V, $R_L = 4\ \Omega$
- $P_O = 2 \cdot 0.1$ W, $V_S = 3$ V, $R_L = 4\ \Omega$



PowerDIP16

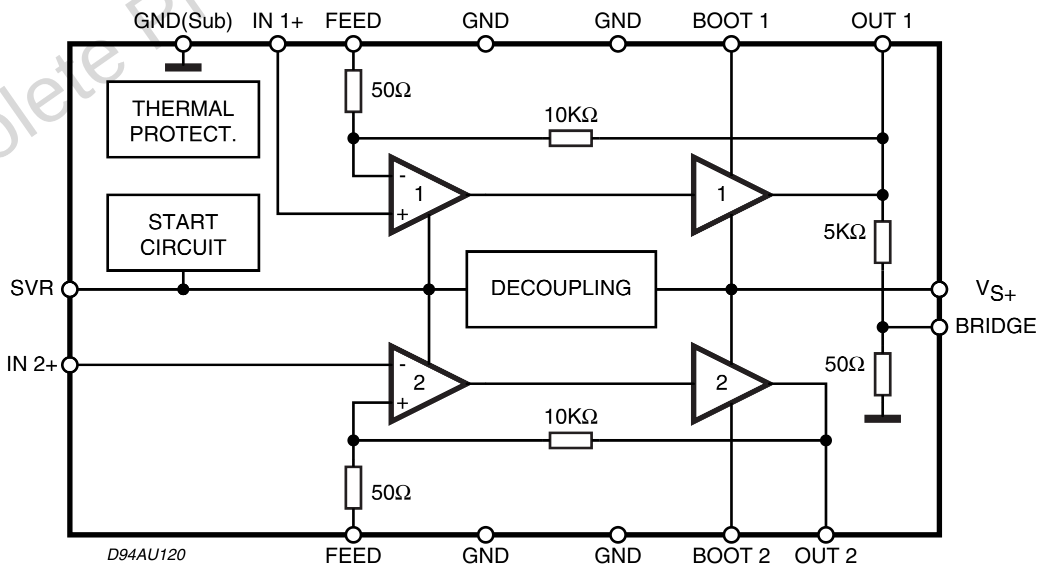
Description

The TEA2025B is a monolithic integrated circuit housed in the 12+2+2 PowerDIP16 package, intended for use as a dual or bridge power audio amplifier in portable radio cassette players.

Table 1. Device summary

Part number	Package
TEA2025B	PowerDIP16 (12+2+2)

Figure 1. Block diagram



1 Device overview and electrical specifications

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply voltage	15	V
I_O	Ouput peak current	1.5	A
T_J	Junction temperature	150	°C
T_{stg}	Storage temperature	150	°C

Figure 2. Pin connections PowerDIP16 (12+2+2)

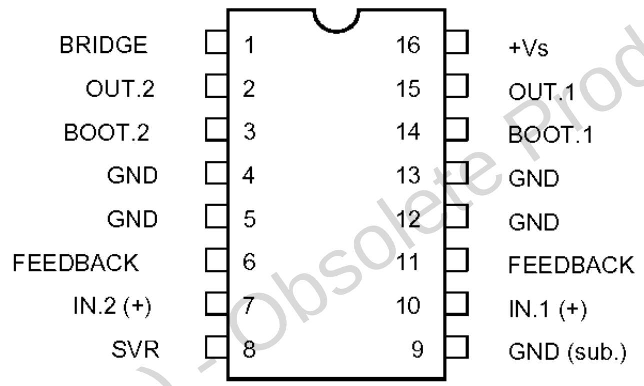


Table 3. Thermal data

Symbol	Description		PowerDIP16 (12+2+2)(1)	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	Max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	Max	60	°C/W

1. $R_{th\ j\text{-}amb}$ is measured on devices bonded on a 10 x 5 x 0.15 cm glass-epoxy substrate with a 35 mm thick copper surface of 5 cm^2.

Table 4. Electrical characteristcs (T_{amb} = 25 °C, V_S = 9 V, stereo unless otherwise specified**)**

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage			3		12	V
I_Q	Quiescent current				35	50	mA
V_O	Quiescent output voltage				4.5		V
A_V	Voltage gain	Stereo		43	45	47	dB
		Bridge		49	51	53	dB
ΔA_V	Voltage gain difference					±1	dB
R_j	Input Impedance				30		kΩ
P_O	Output power (d = 10%)	Stereo 8 (per channel)	9 V 4 Ω	1.7	2.3		W
			9 V 8 Ω		1.3		W
			6 V 4 Ω	0.7	1		W
			6 V 8 Ω		0.6		W
			6 V 16 Ω		0.25		W
			6 V 32 Ω		0.13		W
			3 V 4 Ω		0.1		W
			3 V 32 Ω		0.02		W
			12 V 8 Ω		2.4		W
		Bridge	9 V 8 Ω		4.7		W
			6 V 4 Ω		2.8		W
			6 V 8 Ω		1.5		W
			3 V 16 Ω		0.18		W
			3 V 32 Ω		0.06		W
d	Distortion	Vs = 9 V; R_L = 4 Ω	Stereo Bridge		0.3 0.5	1.5	%
SVR	Supply voltage rejection	f = 100 Hz, V_R = 0.5 V, R_g = 0		40	46		dB
$E_{N(IN)}$	Input noise voltage	R_G = 0			1.5	3	mV
		R_G = 10 4 Ω			3	6	mV
CT	Crosstalk	f = 1 kHz, R_g= 10 kΩ		40	52		dB

Term. N° (PowerDIP16)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DC volt. (V)	0.04	4.5	8.9	0	0	0.6	0.04	8.5	0	0.04	0.6	0	0	8.9	4.5	9

Figure 3. Bridge application

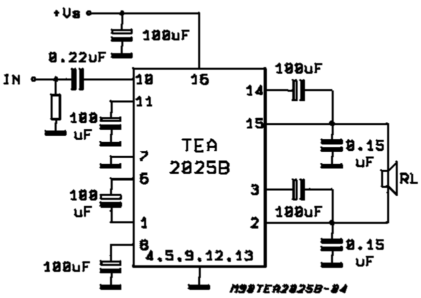


Figure 4. Stereo application

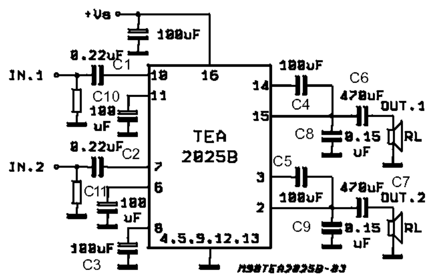


Figure 5. Supply current vs. supply voltage ($R_L = 4\ \Omega$)

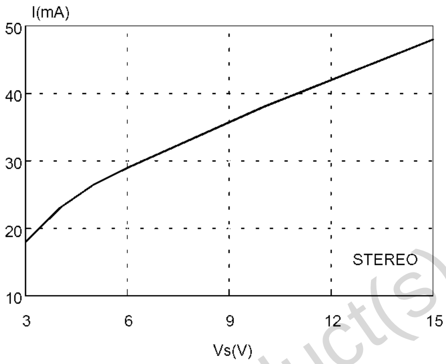


Figure 6. Output voltage vs. supply voltage

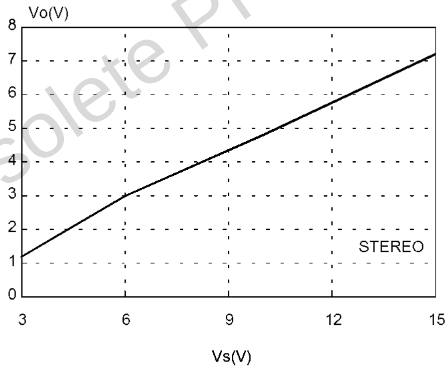


Figure 7. Output power vs. supply voltage (THD = 10%, f = 1 kHz)

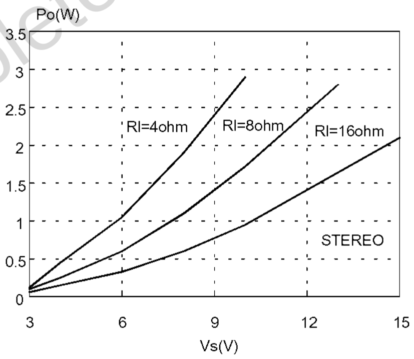
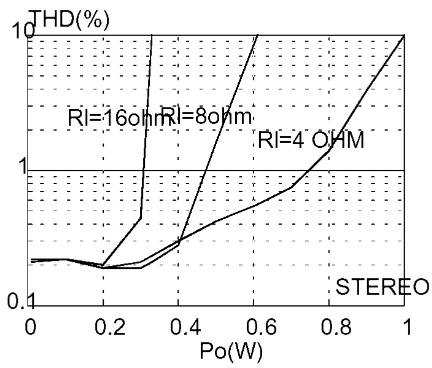


Figure 8. THD vs. output power ($f = 1\ kHz$, $V_S = 6\ V$)



2 Application information

2.1 Input capacitor

The input capacitor is PNP type allowing the source to be referenced to ground. In this way no input coupling capacitor is required. However, a series capacitor (0.22 µF) to the input side can be useful in case of noise due to variable resistor contact.

2.2 Bootstrap

The bootstrap connection allows increasing the output swing.

The recommended value for the bootstrap capacitors (100 µF) avoids a reduction of the output signal also at low frequencies and low supply voltages.

2.3 Voltage gain adjustment

2.3.1 Stereo mode

The voltage gain is determined by on-chip resistors R1 and R2 together with the external RfC1 series connected between pin 6 (11) and ground. The frequency response is approximated by:

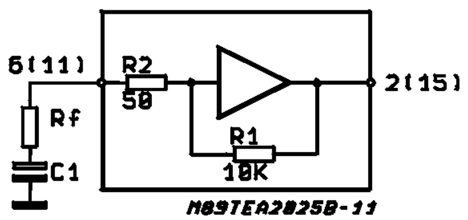
$$\frac{V_{OUT}}{V_{IN}} = \frac{R1}{Rf \div R2 + \frac{1}{JWC1}}$$

With Rf = 0, C1 = 100 µF, the gain results in 46 dB with pole at f = 32 Hz.

The purpose of Rf is to reduce the gain. It is recommended to not reduce it under 36 dB.

2.3.2 Bridge mode

Figure 9. Internal voltage divider



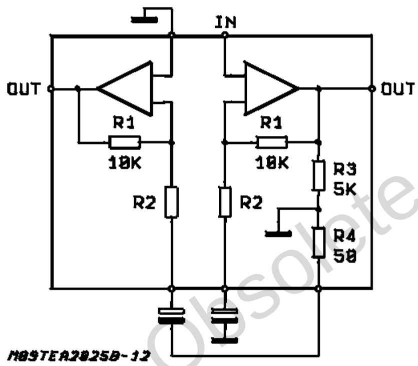
The bridge configuration is realized very easily thanks to an internal voltage divider which provides (at pin 1) the CH 1 output signal after reduction.

It is sufficient to connect pin 6 (inverting input of CH 2) with a capacitor to pin 1 and to connect pin 7 to ground. The total gain of the bridge is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R1}{Rf \div R2 + \frac{1}{JWC1}}\left(1 + \frac{R3}{R4}\frac{R1}{R2 + R4 + \frac{1}{JWC1}}\right)$$

and with the recommended values (C1 = C2 = 100 µF, Rf= 0), then Gv = 52 dB with first pole at f = 32 Hz

Figure 10. Bridge configuration (stereo)



2.4 Output capacitors

The low cutoff frequency due to the output capacitor depending on the load is given by:

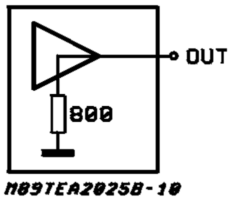
$$F_L = \frac{1}{2\Pi C_{OUT} \cdot R_L}$$

with C_{OUT} 470 µF and R_L = 4 ohm, then F_L = 80 Hz.

2.5 Pop noise

Most amplifiers similar to the TEA2025B need external resistors between the DC outputs and ground in order to minimize pop on/off noise and crossover distortion.

Figure 11. Internal resistor



The TEA2025B requires less components as these resistors (800 ohm) are in the device.

2.6 Stability

A good layout is recommended in order to avoid oscillations.

Generally the designer must pay attention to the following points:

- Short wires of components and short connections.
- No ground loops
- Bypass of supply voltage with capacitors as close as possible to the supply IC pin. The low value (polyester) capacitors must have suitable temperature and frequency characteristics.

■ No sockets
The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: P_O (and therefore P_{tot}) and I_d are simply reduced.

3 Application suggestions

The recommended values of the components are those shown in the stereo application circuit of *Figure 4*, although different values can be used (refer to the following table).

Table 5. Recommended values for stereo applications

Component	Recommended value	Purpose	Larger than	Smaller than
C1, C2	0.22 µF	Input DC decoupling in case of slider contact noise of variable resistor		
C3	100 µF	Ripple rejecton		Degradation of SVR, increase of at low frequency and low voltage
C4, C5	100 µF	Bootstrap		
C6, C7	470 µF	Output DC decoupling		Increase of low frequency cutoff
C8, C9	0.15 µF	Frequency stability		Danger of oscillations
C10, C11	100 µF	Inverting input DC decoupling		Increase of low frequency cutoff

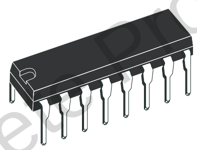
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

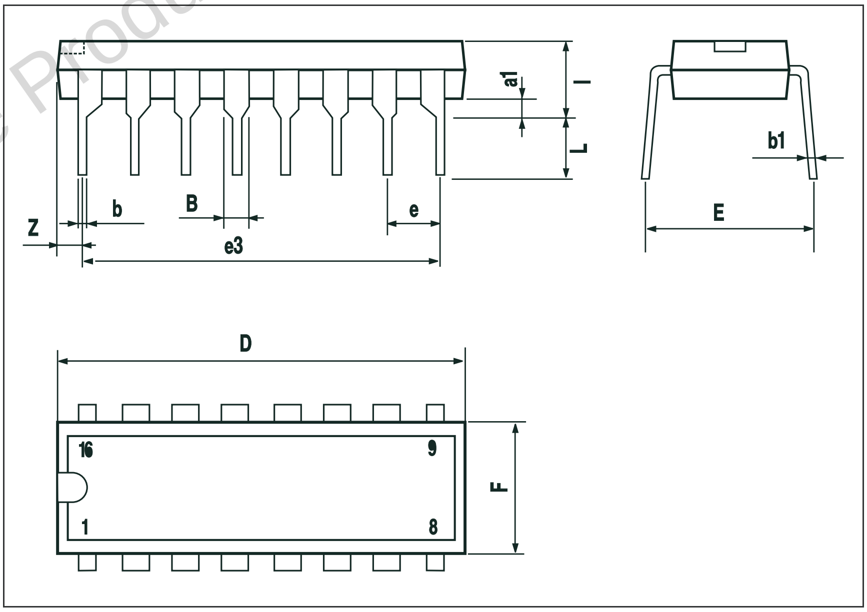
Figure 12. PowerDIP16 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



PowerDIP16



5 Revision history

Table 6. Revision history

Date	Revision	Changes
September 2003	2	Updates not recorded
30-Apr-2010	3	Updated title and added environmental compliance statement for package
01-Oct-2012	4	Removed SO20 package option from datasheet Minor textual updates Revised document presentation