SGS-THOMSON MICROELECTRONICS

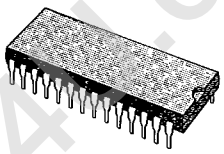
TEA5640B

PAL/SECAM COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

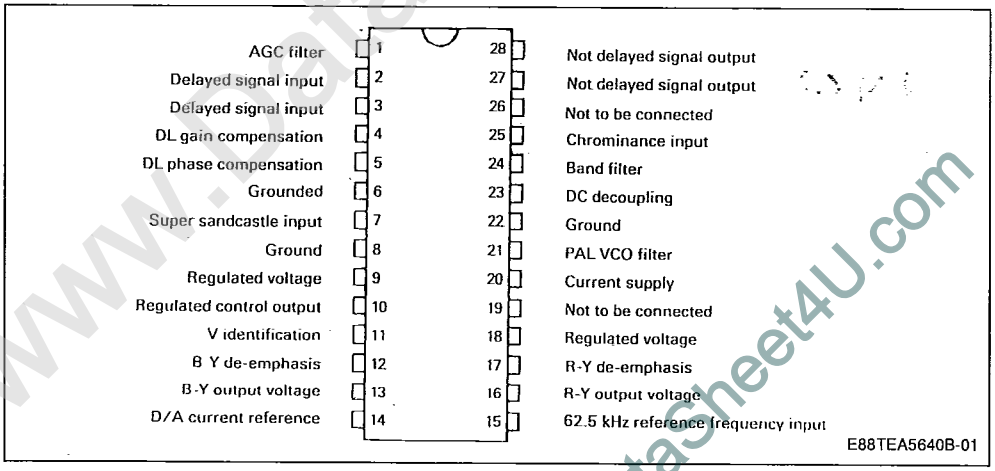
DESCRIPTION

The TEA5640B is a multistandard TV decoder for PAL-SECAM. The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are, four numerical frequency locked loops that allow the elimination of PAL crystal. The circuit uses an external reference frequency of 62.5 kHz generally provided by the frequency synthesis tuner of the TV set.



TEA5640B
DIP28
(Plastic Package)

PIN CONNECTIONS

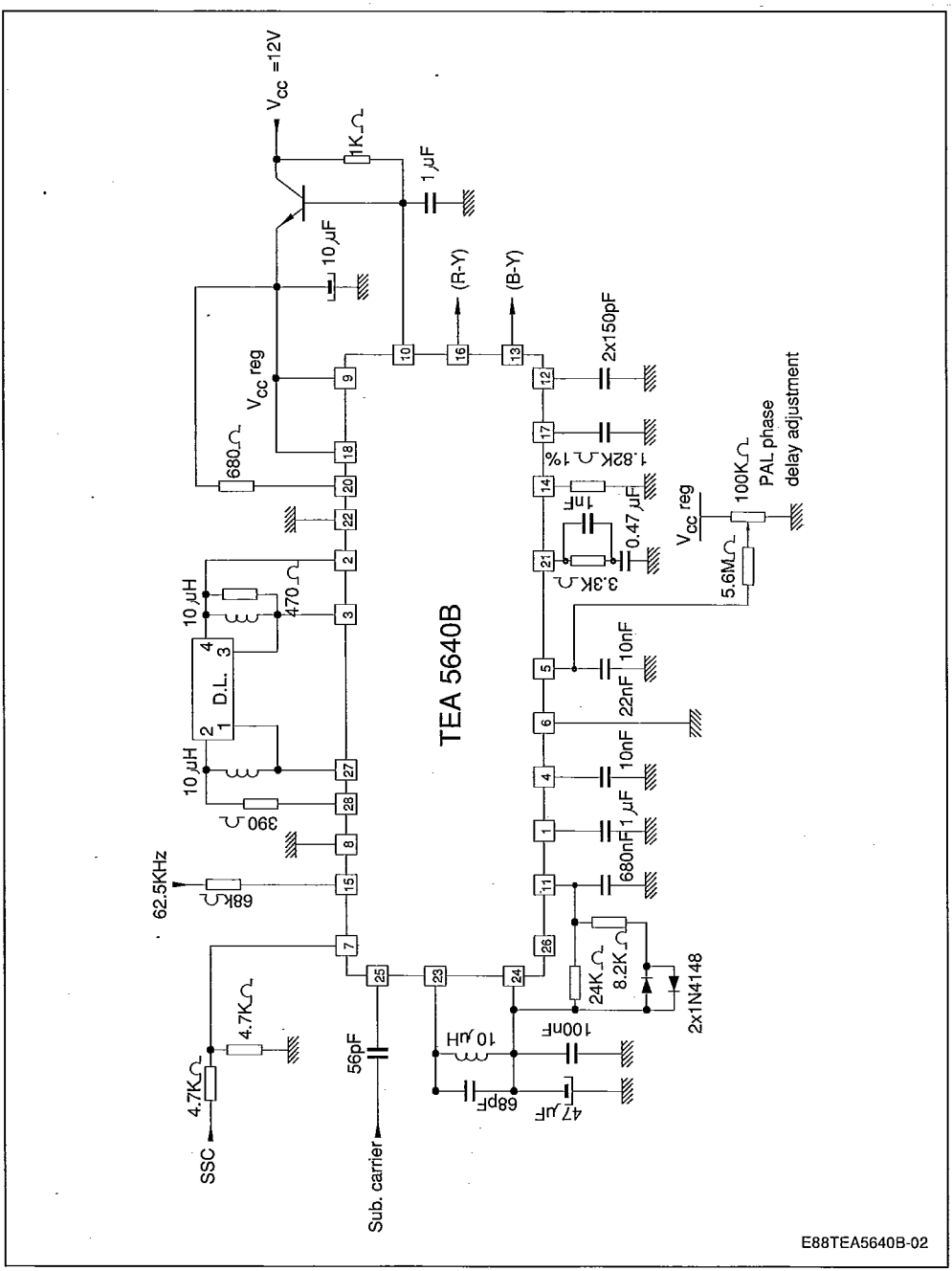


E88TEA5640B-01

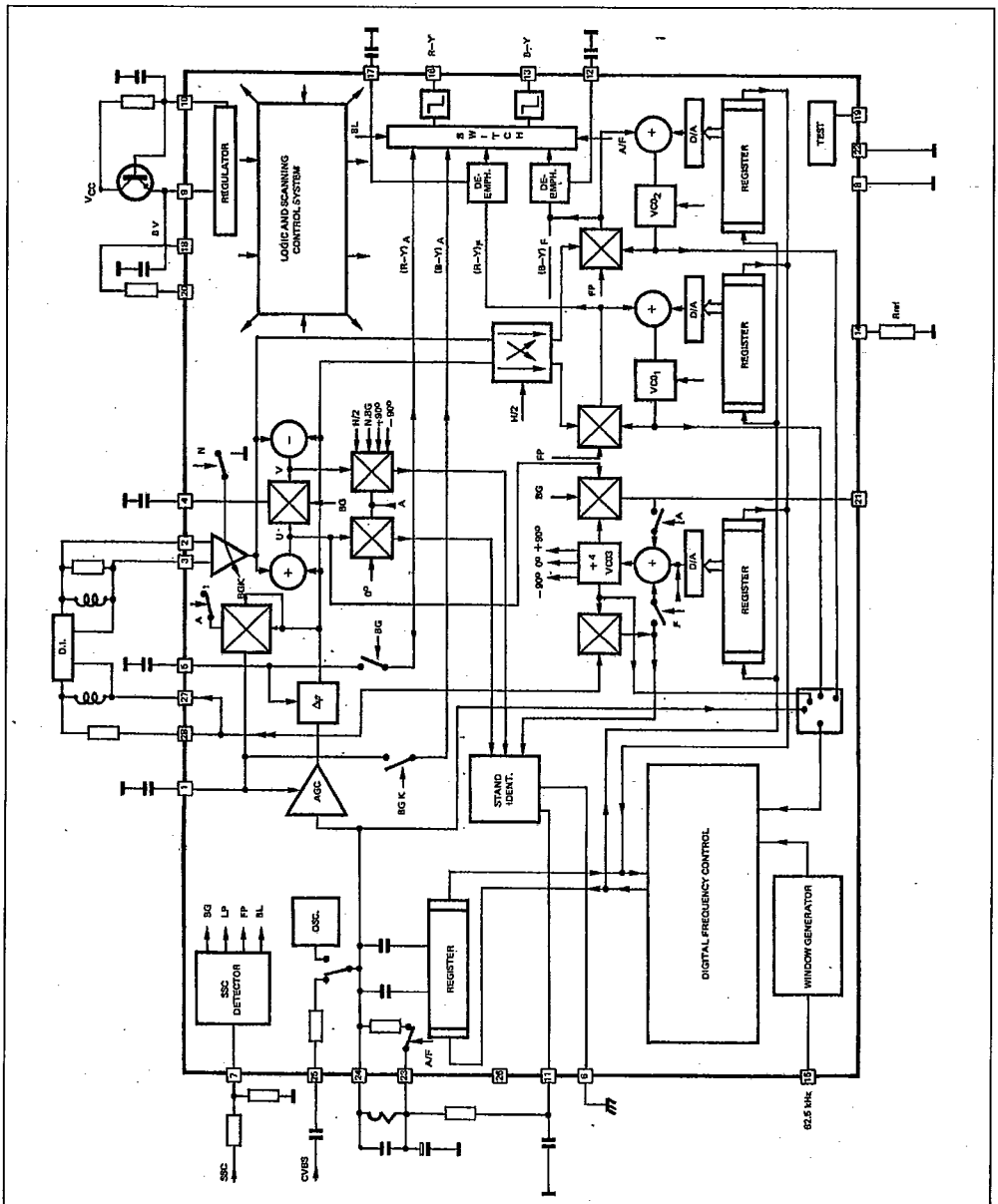
FEATURES

- FULL AUTOMATIC MULTISTANDARD SWITCHING :
- THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM THAT PROVIDES ALL THE SWITCHINGS REQUIRED FOR THE AUTOMATIC STANDARD RECOGNITION. THIS SYSTEM IS SYNCHRONIZED BY THE FRAME PULSE.
- NO CRYSTAL REQUIREMENT :
  THE PAL FREQUENCIES ARE SYNTHESIZED ORIGINALLY BY THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz AND DATA STORED IN THE ROM.
- AUTOMATIC GAIN ADJUSTMENT OF THE BELL
  FILTER : BY SWITCHING AN INTERNAL CAPACITOR NETWORK INCLUDED IN A DIGITAL LOOP.
- AUTOMATIC GAIN ADJUSTMENT OF THE DELAY LINE COMPENSATIONS :
  THIS ADJUSTMENT IS MADE ON THE BURST AND IS REFRESDED EVERY LINE RETRACE
- AUTOMATIC ADJUSTMENT FOR PAL OSCILLATOR :
  THIS OSCILLATOR HAS A DIGITAL AND AN ANALOGIC LOOP. THE PAL FREQUENCIES ARE MEMORIZED IN A ROM CONNECTED TO THE DIGITAL LOOP. THE DIGITAL LOOP GIVES THE RIGHT FREQUENCY AND THE ANALOGIC ONE HOLDS THE PHASE.
- AUTOMATIC ADJUSTMENT OF FoR AND FoB IN SECAM : THESE FREQUENCIES ARE PROGRAMMED IN THE ROM AND ARE SENT TO TWO OTHER DIGITAL LOOPS WHEN SECAM STANDARD IS SELECTED.
- AUTOMATIC DIFFERENCE PHASE ERROR COMPENSATION IN PAL MODE.
  THE PAL VCO IS LOCKED ON THE BURST AND DURING THE LINE, ON THE BLUE PICTURE CONTENT (0° axis color vector).

TYPICAL APPLICATION



BLOCK DIAGRAM



S : Secam ; BP : Bandfilter adjustment ; P : Pal ; BG : Burstgate
LP : Line Pulse ; FP : Frame Pulse
A : Amplit. Modul. ; F : Freq. Modul ; K : Identification ; BL : Blanking

E88TEA5640B-03

STANDARD SWITCHING AND INHIBITION

SECAM recognition :

- When SECAM on, pin 12 and pin 17 DC voltages are lower than 5 V.
- For PAL standard, pin 12 and pin 17 DC voltages are regulated V_{CC} (typical 8 V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0 to 70	°C
T_{stg}	Storage Temperature		– 40 to 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C ; V_{CC} = 12 V ; With Normalized Color Bar Pattern Input Signal (75 %) Subcarrier Level : 320 mVPP
Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Supplies					
Vreg	Regulated Voltage I10 = 4 mA	Pins 9 - 18	7.5	8	8.5	V
ICC	Supply Current	Pin 9 + Pin 18		90	120	mA
I9	Supply Current	Pin 9			90	mA
I18	Supply Current	Pin 18			27	mA
VI2L	DC Voltage at I20 = 15 mA	Pin 20		0.8		V
I10	Input Current	Pin 10	2		20	mA
	Transfer Characteristic (I10 = 4.0 mA)			250		mA/V
	Current Reference	Pin 14				
V14	DC Voltage (I14 = 0.77 mA		1.2	1.4	1.6	V
	Internal Bias	Pin 24				
V 24	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2 mA)			90	110	Ω
	Reference Clock Input					
	F = 62.5 kHz ± 6Hz	Pin 15				
I15L	Low Level Input Current (V15 = 2.1 V)		– 20	– 10	– 5	µA
I15H	High Level Input Current (V15 = 3.2 V)			5	10	µA
V15L	Low Level Input Voltage	R Source = 68 kΩ			1	V
V15H	High Level Input Voltage	R Source = 68 kΩ	4			V
	Voltage Threshold			2.8		V
	Super Sandcastle Detector	Pin 7				
VB	Blanking Threshold		0.5	0.75	0.9	V
VL	Line Threshold		1.6	1.8	1.9	V
V6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I7	Input Current (V7 = 1.75 V)		– 20		0	µA
	Max Input Voltage Pin 7				6.0	V

ELECTRICAL CHARACTERISTICS (continued)

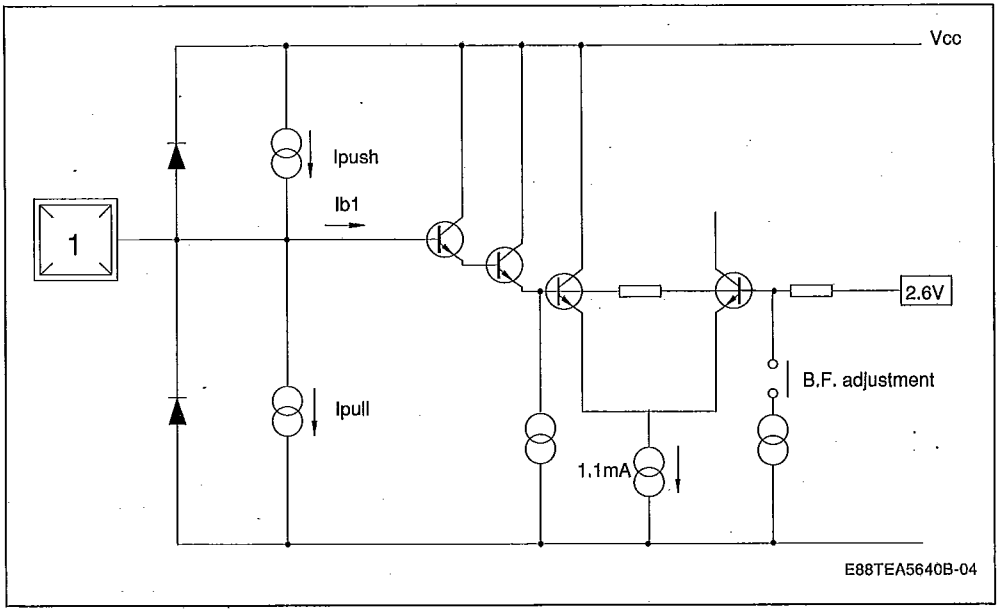
Symbol	Parameter		Min.	Typ.	Max.	Unit
	Chrominance Input	Pin 25				
V25	DC Voltage			5.5		V
	Maximum AC Input Voltage				0.64	Vpp
	Impedance		0.8	1		kΩ
	Automatic Gain Control					
	SECAM MODE					
	• 0 dB Reference Voltage for Measurement on Pins 27 - 28 (chroma input voltage V25 = 320 mVpp)		50	150	250	mVpp
	• AC Voltage Variation on Pins 27 - 28 (V25 = + 6 dB)		− 3		+ 3	dB
	• AC Voltage Variation on Pins 27 -28 (V25 = − 24 dB)		− 5		+ 2	dB
	PAL MODE WITH IDENTIFICATION					
	• 0 dB Reference Voltage for Measurement on Pins 13 -16 (chroma input voltage V25 = 320 mVpp)					
	• AC Voltage Variation on Pins 13 - 16 (V25 = + 6 dB)		− 3		+ 3	dB
	• AC Voltage Variation on Pins 13 - 16 (V25 = − 24 dB)		− 5		+ 2	dB
	Demodulator Part					
	GENERALITIES					
V13	B-Y Output DC Voltage	Pin 13	3	3.5	4	V
V16	R-Y Output DC Voltage	Pin 16	3.2	3.7	4.2	V
	Maximum Sink Current	Pin 13	0.4			mA
	Maximum Sink Current	Pin 16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance (± 50 µA)			250		Ω
	R-Y Output AC Impedance (± 50 µA)			250		Ω
	Blanking Level Offset				± 2	%
	Secam Mode					
VBYS	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYS	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mVpp
	Pal Mode					
VBYP	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYP	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.0		1.3	
	Residual Subcarrier			30		mVpp

ELECTRICAL CHARACTERISTICS (continued)

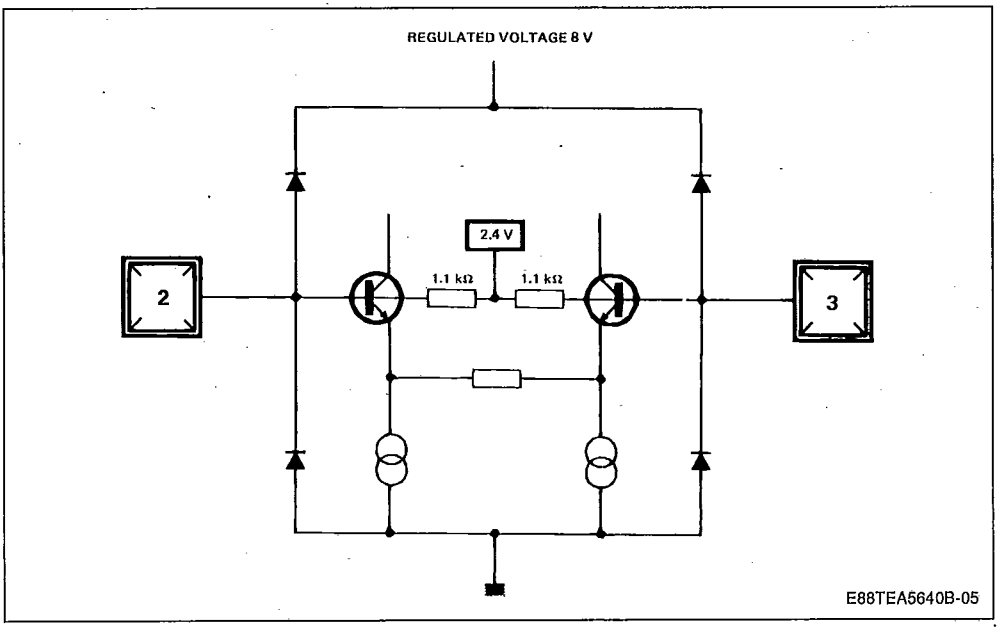
Symbol	Parameter	Min.	Typ.	Max.	Unit
	De-Emphasis Pins 12 - 17				
	SECAM MODE				
	DC Voltage (blanking level)		3.5	4.0	V
	Impedance		11		kΩ
	PAL MODE				
	DC Voltage		VREG		V
	Impedance		70		kΩ
	Reference Oscillator PLL				
	Catching Range in PAL Mode	± 350			Hz
	Holding Range	± 500			Hz
	Band Filter Pin 23				
	Impedance SECAM Mode	3.7	4.7	5.7	kΩ
	PAL Mode	0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)		20		pF
	Maximum Switchable Internal Capacitance (all standards)		50		pF
ΔF	Internal Oscillator Frequency Range for L = 10 µH C = 68 pF	590			kHz
	Frequency Offset, After Automatic Adjustement			± 10	kHz
	Undelayed Signal Outputs Pins 27 - 28				
V27 V28	DC Voltage		1.6		V
I27 I28	Sink Current	1			mA
	Impedance		30		Ω
	Identification				
	Burst Attenuation Range / Nominal Level				
	SECAM Mode (line identification)	30			dB
	Pal Mode	30			dB
	Delayed Signal Input Pins 2 - 3				
	DC Voltage in PAL Mode		2.4		V
	Input Impedance	0.88	1.1	1.32	kΩ
	Delay Line Attenuation Compensation				
	Range of Automatic Attenuation Compensation	− 3	− 9	− 15	dB
	Delay Line Phase Shift Compensation				
	Range of Phase Shift Compensation with a 100KΩ Potentiometer (see application diagram p. 3)	± 30			Degree
	Alternation Line Detection PAL or SECAM Pin 11				
VTHH	High Differential Threshold (VTHH = V11H − V24)	200		350	mV
VTHL	Low Differential Threshold (VTHL = V11L − V24)	− 350		− 200	mV
	Leakage Current Threshold (V11 = V24 + 1V)			0.5	µA

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

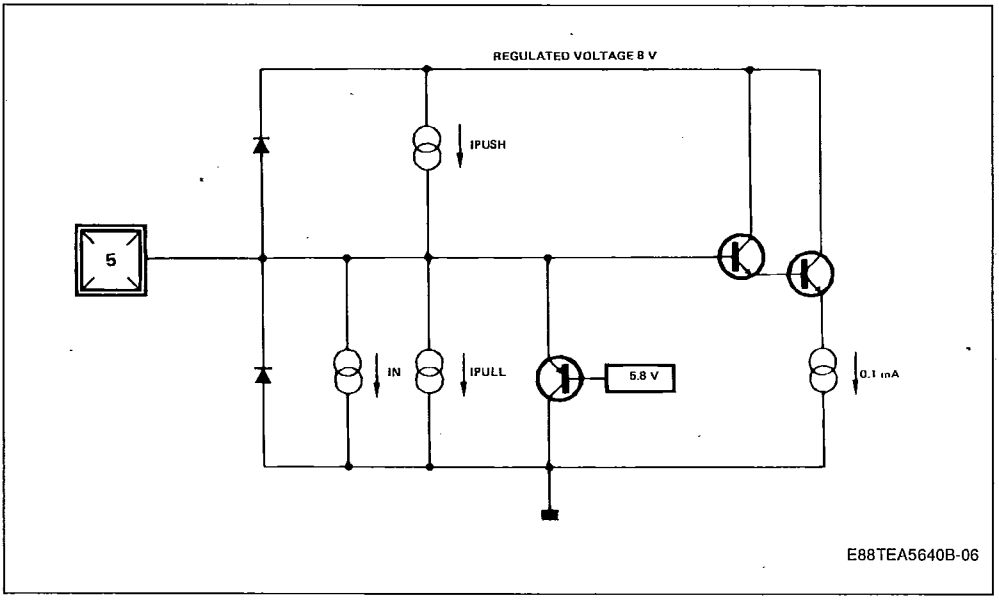
PIN 1



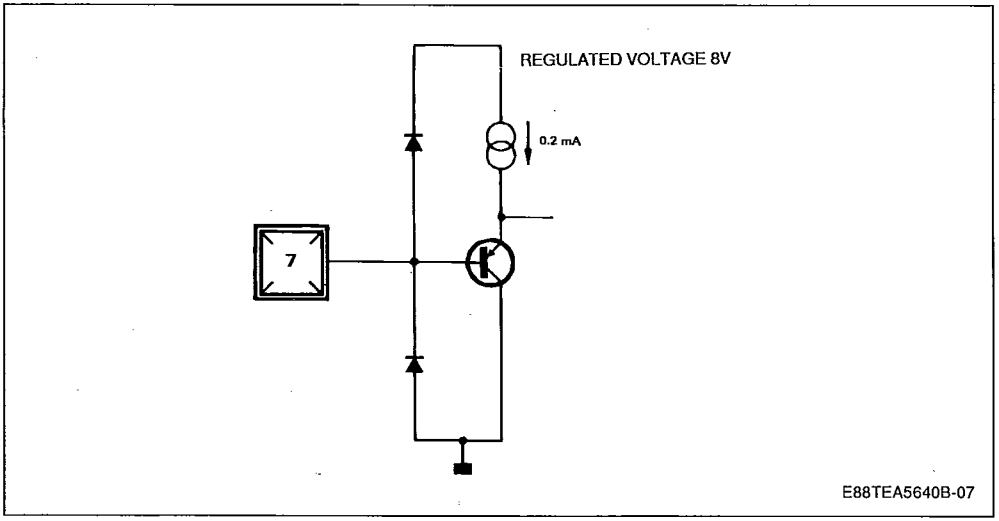
PINS 2 – 3



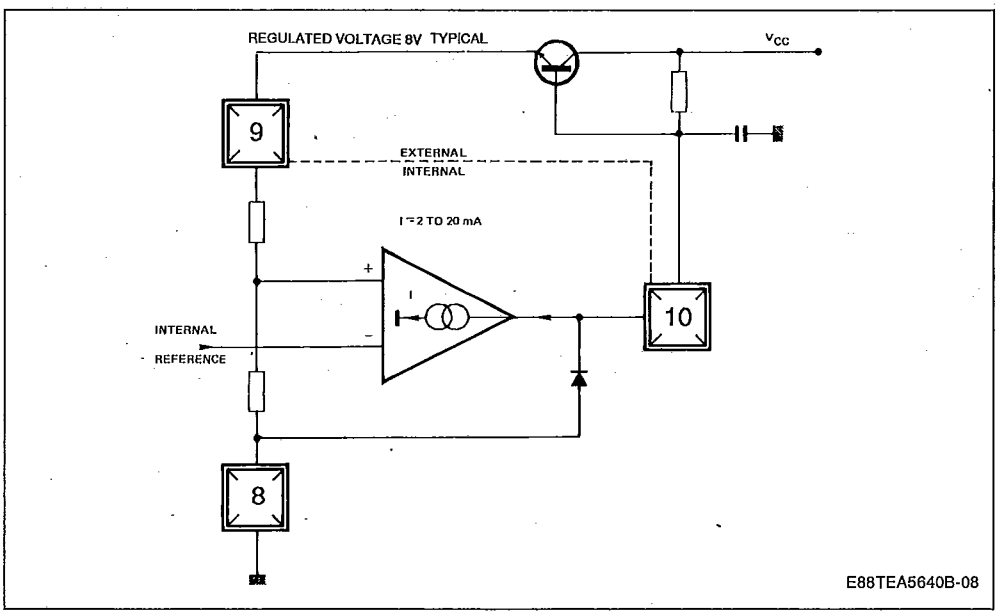
PIN 5


REGULATED VOLTAGE 8 V
IPUSH
5
IN
IPULL
5.8 V
0.1 mA
E88TEA5640B-06

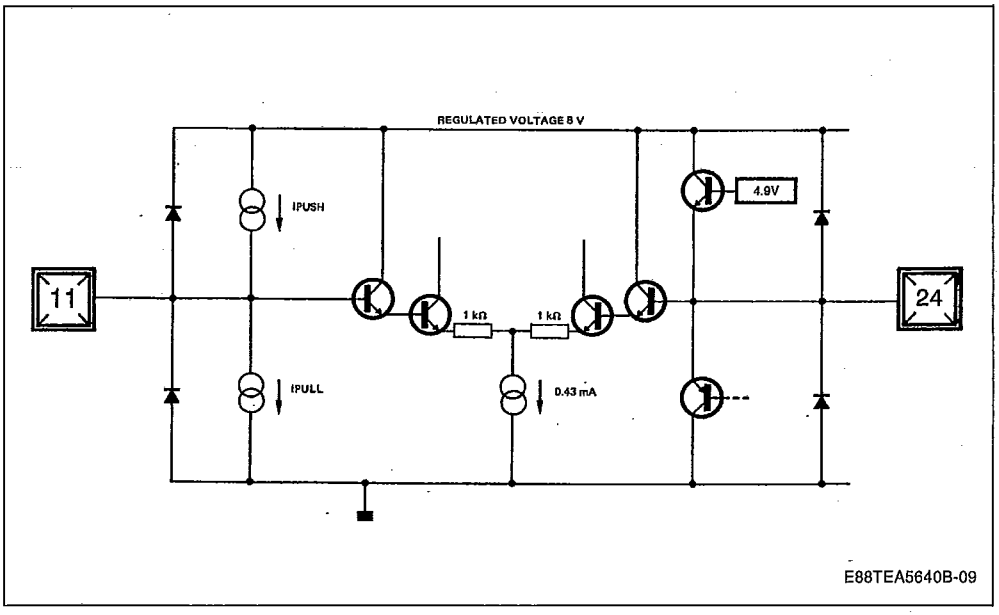
PIN 7


REGULATED VOLTAGE 8V
0.2 mA
7
E88TEA5640B-07

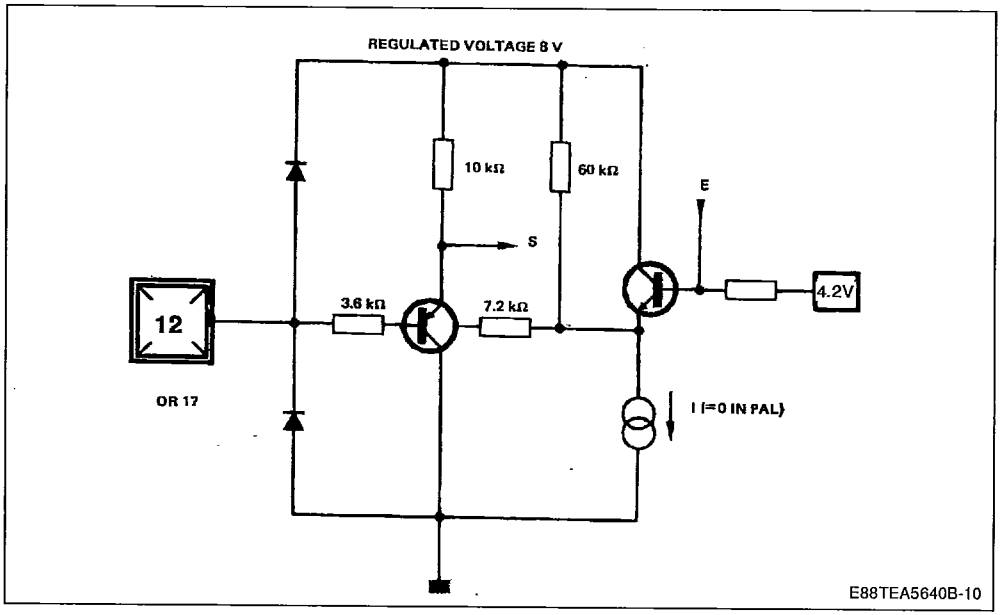
PINS 8 – 9 – 10



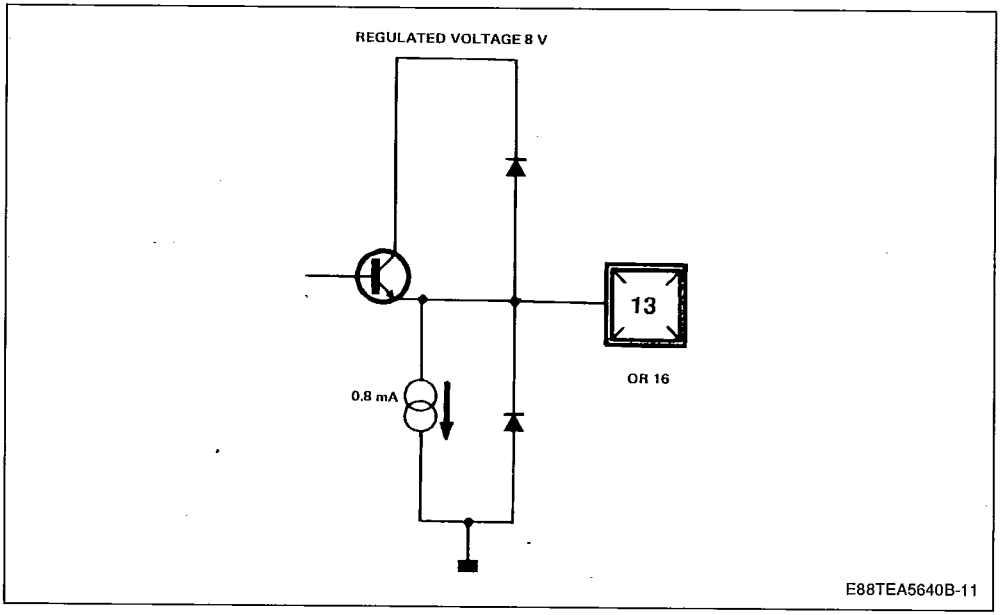
PINS 11 – 24



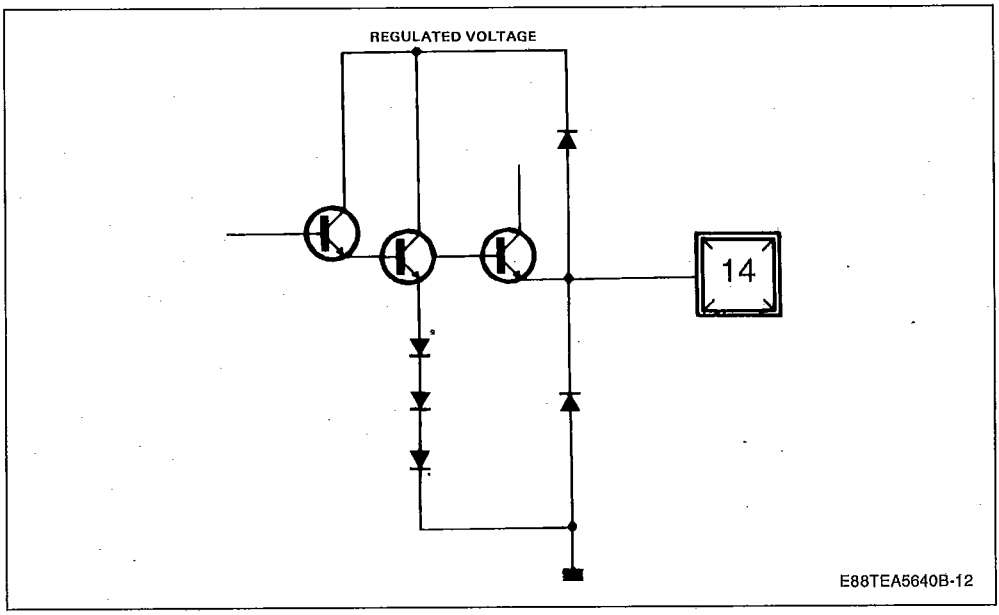
PINS 12 – 17



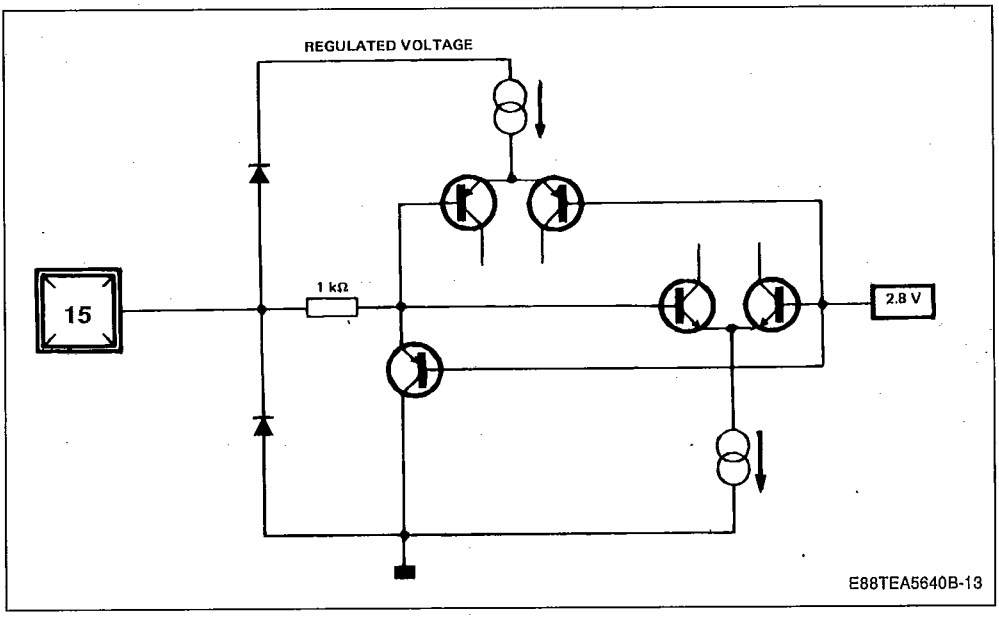
PINS 13 – 16



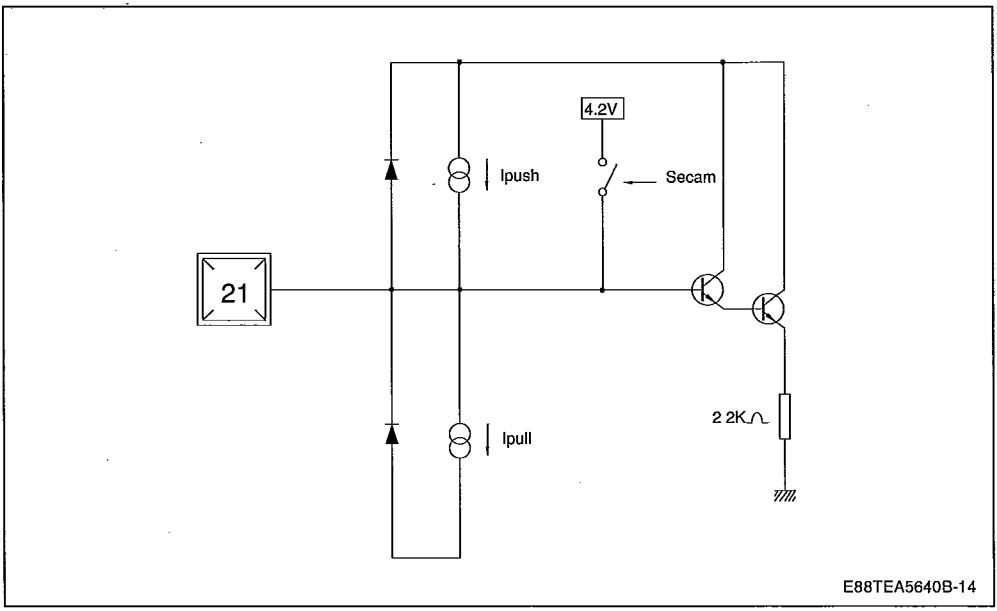
PIN 14

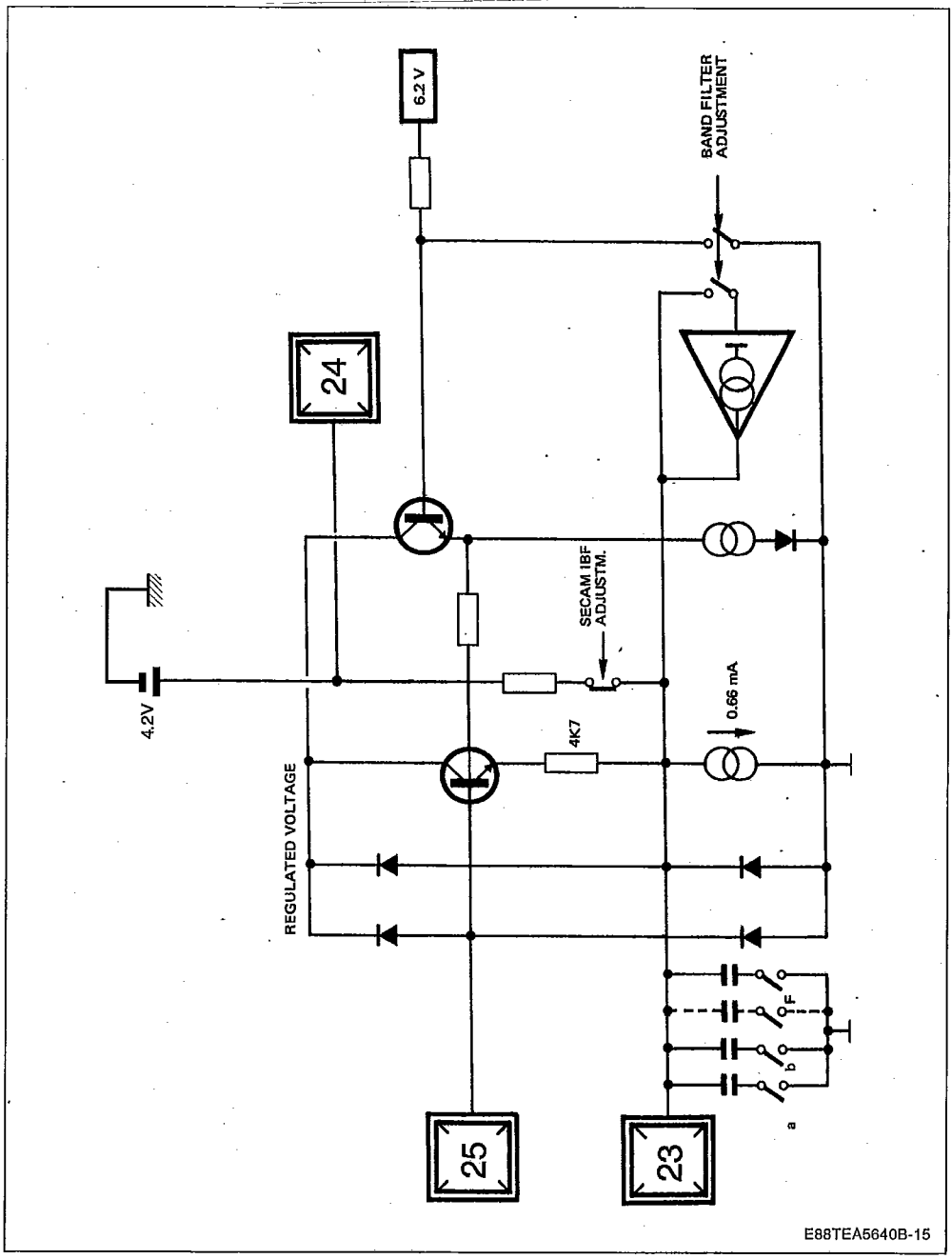

REGULATED VOLTAGE
14
E88TEA5640B-12

PIN 15

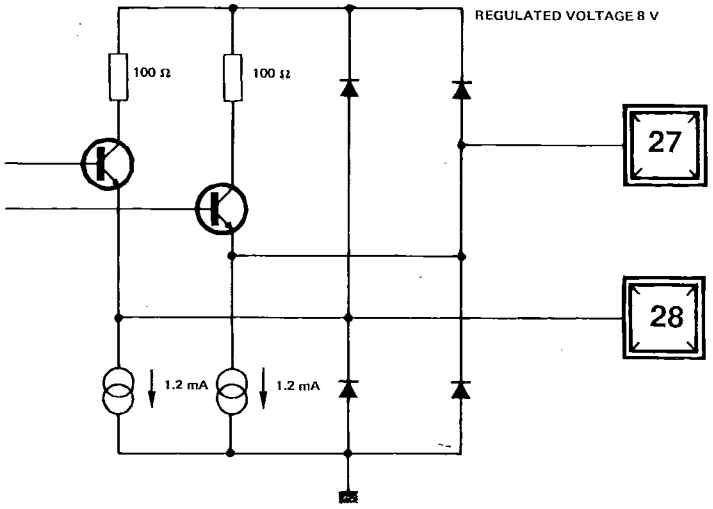

REGULATED VOLTAGE
15
1 kΩ
2.8 V
E88TEA5640B-13

PIN 21 S G S-THOMSON 30E D




6.2 V
BAND FILTER ADJUSTMENT
24
SECAM IBF ADJUSTM.
4.2V
4K7
0.66 mA
REGULATED VOLTAGE
F
b
a
25
23
E88TEA5640B-15

PINS 27 - 28



E88TEA5640B-16

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP