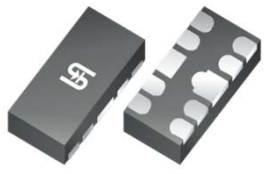
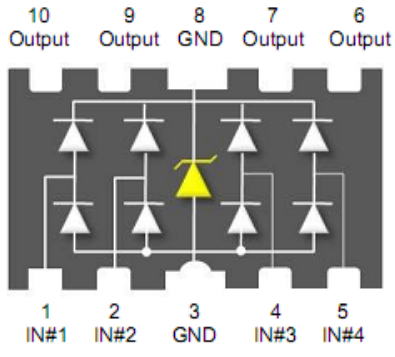
Ultra Low Capacitance ESD Protection Array

FEATURES

- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Meet IEC61000-4-5 (Lightning) rating. 1A (8/20μs)
- Protects two directional I/O lines
- Working voltage: 5V
- Low Capacitance : 0.5 pF typical (I/O to I/O)
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)



2510P10 (DSON10)



Note: Output line (No internal connection)

MECHANICAL DATA

- Case: 2510P10 (DSON10) standard package, molded plastic
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- High temperature soldering guaranteed : 260°C/10s
- Molding compound flammability rating : UL 94V-0
- Weight: 15 ± 0.5 mg
- Marking code : P524

APPLICATIONS

- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interface (DVI)
- PCI Express
- Serial ATA
- USB 3.0 Super Speed Interface

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)		
PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	150	W
Peak Pulse Current (tp=8/20μs)	I_{PP}	1	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 15 ± 8	KV
Junction and Storage Temperature Range	T_J , T_{STG}	-55 to +150	°C

PARAMETER		SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltage	I_R = 1 mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R = 5 V	I_R	-	1	μA
Clamping Voltage	I_{PP} = 1 A	V_C	-	15	V
Junction Capacitance	V_R = 0 V , f = 1.0 MHz	C_J	1		pF

RATINGS AND CHARACTERISTICS CURVES

(T_A=25°C unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

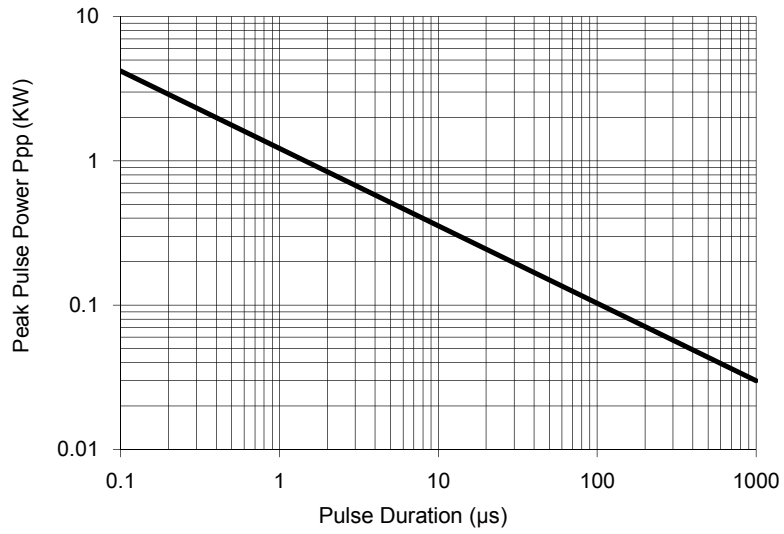


Fig. 2 Pulse Waveform

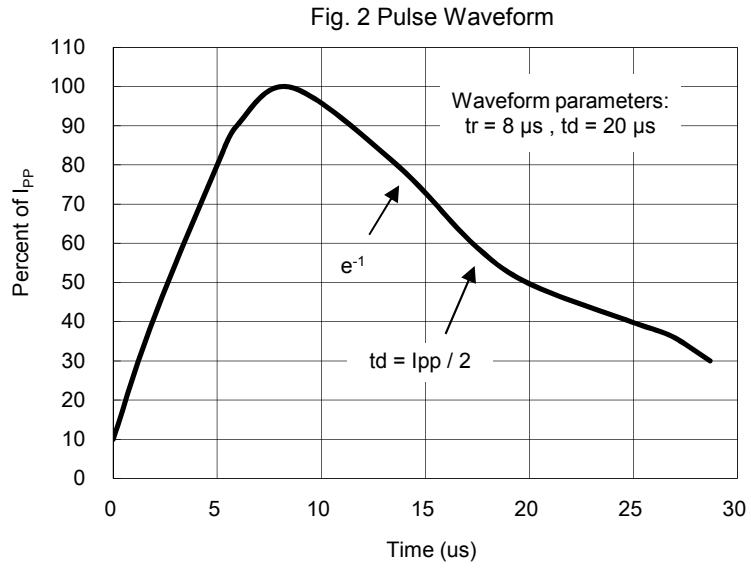


Fig. 3 Admissible Power Dissipation Curve

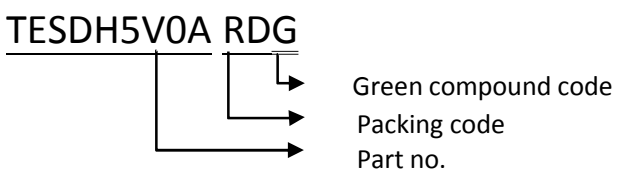
Fig. 4 Typical Junction Capacitance

Fig. 5 Clamping Voltage VS. Peak Pulse Current

Fig. 6 Insertion Loss

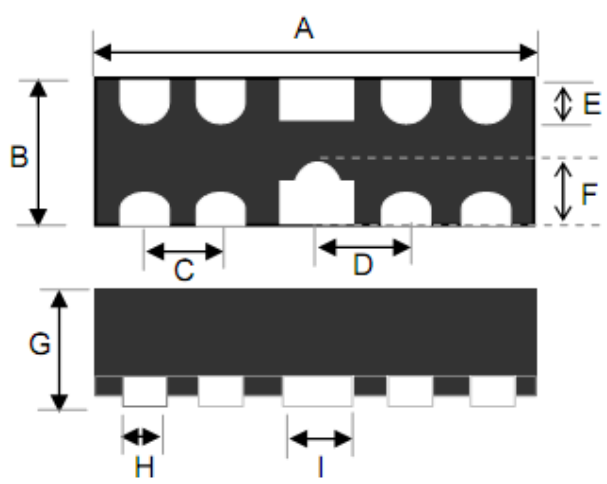
Small Signal Product

ORDER INFORMATION (EXAMPLE)



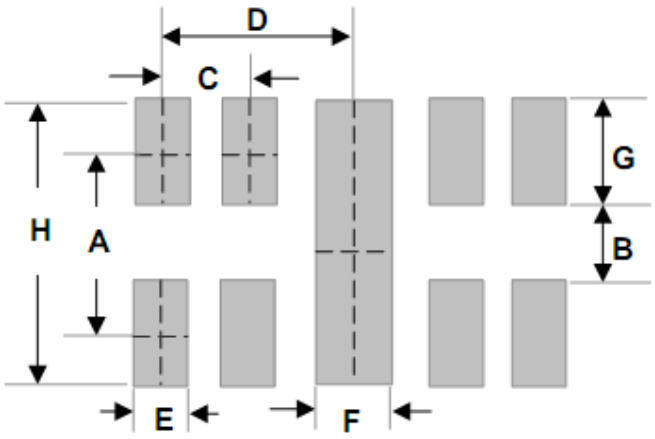
PACKAGE OUTLINE DIMENSIONS

2510P10 (DSON10)



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.40	2.60	0.094	0.102
B	0.90	1.10	0.035	0.043
C	0.50 REF		0.020 REF	
D	0.63 REF		0.025 REF	
E	0.30	0.43	0.012	0.017
F	0.45	0.55	0.018	0.022
G	0.50	0.65	0.020	0.026
H	0.15	0.25	0.006	0.010
I	0.35	0.45	0.014	0.018

SUGGESTED PAD LAYOUT



DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
A	0.88	0.035
B	0.20	0.008
C	0.50	0.020
D	1.00	0.039
E	0.20	0.008
F	0.40	0.016
G	0.68	0.027
H	1.55	0.061

Note: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

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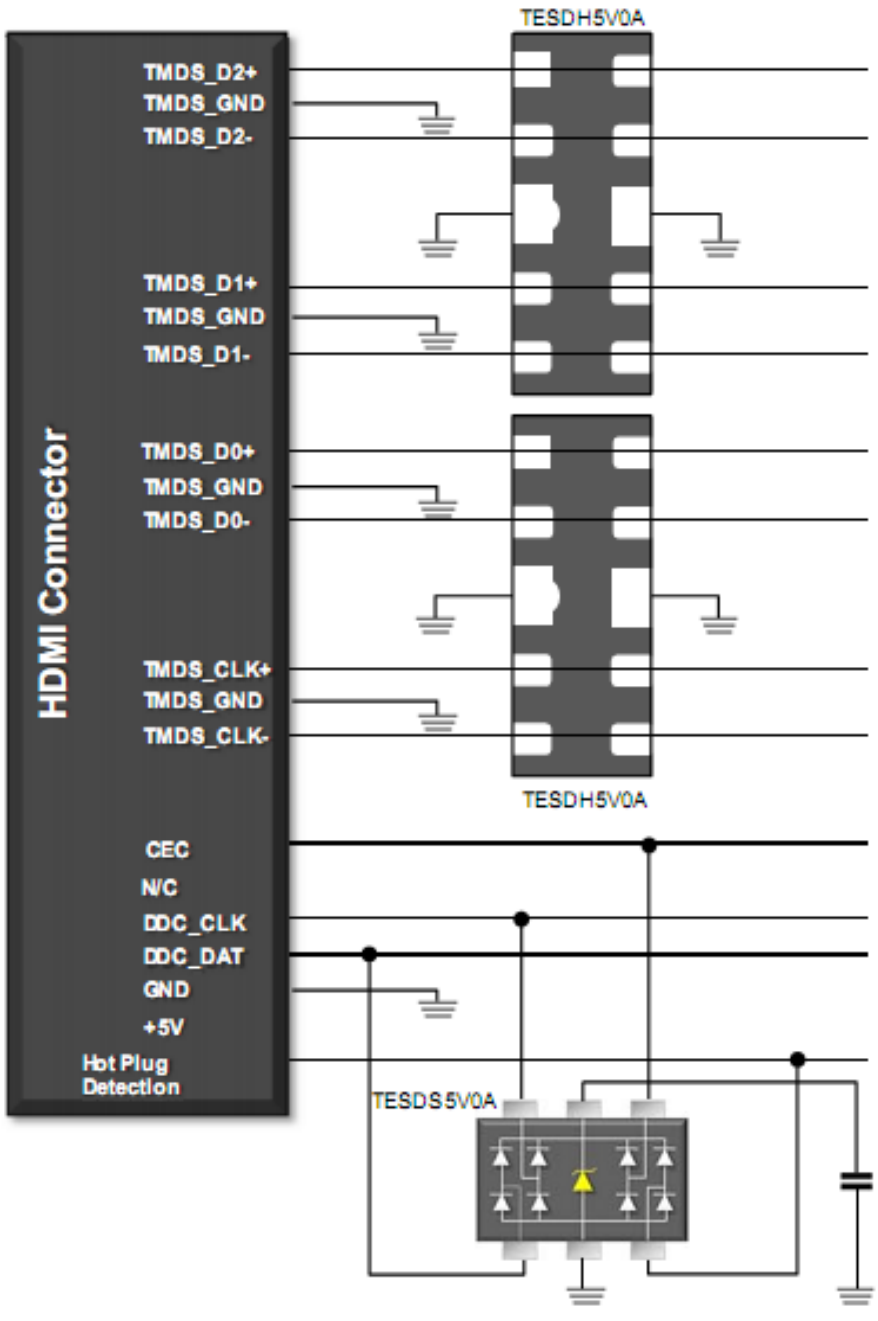
APPLICATIONS INFORMATION

◇ Designed for protection of high-speed interfaces such as HDMI
◇ Ultra low capacitance between the paris while being rated to handle >±8kV ESD contact discharges and >±15kV air discharge
◇ Each device in a leadless package that is less than 1.1mm wide
◇ Designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity
◇ TESDH5V0A is ultra low capacitance ESD protection array designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD, CDE (Cable Discharge Events), and EFT (electrical fast transients)
◇ The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for applications of high speed interface, ex HDMI, DisplayPortTM, MDDI, and eSATA interfaces

CIRCUIT BOARD LAYOUT RECOMMENDATIONS FOR HDMI APPLICATION

◇ The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6)
◇ Signal line enters at pin 1 and exits at pin 10 and the PCB trace connects pin 1 and 10 together. Ground is connected at pin 3 and 8.
◇ One large ground pad should be used in lieu of two separate pads



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