Bi-directional ESD Protection Diode

DESCRIPTIONS

The TESDL3V3B23P1Q0 is Bidirectional ESD rated clamping cell to protect power interfaces, or one control line, or one low speed data line in an electronic system. It has been specifically designed to protect sensitive electronic components which are connected to power and control lines from over-voltage damage by Electrostatic Discharging (ESD), and Lightning.

TESDL3V3B23P1Q0 is a unique design which includes proprietary clamping cells in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

The TESDL3V3B23P1Q0 may be used to provide ESD protection up to ±30kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 8.2A (8/20μs) according to IEC61000-4-5.

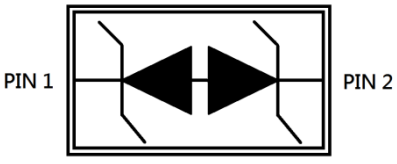
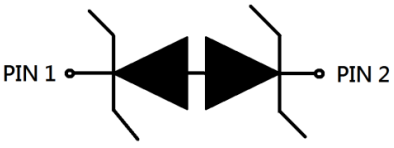
FEATURES

- ESD protect for 1 line with bidirectional.
- Provide ESD protection for each channel to IEC61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC61000-4-5 (Lightning) 8.2A (8/20μs)
- Suitable for 3.3V and below, operating voltage applications
- Ultra small package saves board space.
- Protect one I/O line or one power line.
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free

APPLICATION

- Computers and peripherals
- Control Signal Lines Protection
- Power lines on PCB Protection
- Serial and Parallel Ports Protection

Pb-Free RoHS COMPLIANT HALOGEN FREE

PACKAGE: DFN0603-2L	PIN CONFIGURATION	CIRCUIT DIAGRAM
		

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)			
PARAMETER	**SYMBOL**	**VALUE**	**UNIT**
Peak pulse power (tp = 8/20us)	P_{PK}	70	W
Peak pulse current (tp = 8/20us)	I_{PP}	8.2	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	kV
ESD according to IEC61000-4-2 contact discharge		±30	kV
Junction temperature range	T_J	-55 to +150	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse working voltage		V_{RWM}	-	-	3.3	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	4	-	-	V
Reverse leakage current	V_{RWM} = 3.3V	I_R	-	-	100	nA
Clamping voltage(1)	I_{PP} = 4.0A, tp = 8/20us	V_C	-	-	7.3	V
	I_{PP} = 8.2A, tp = 8/20us		-	-	8.5	V
Clamping voltage(2)	I_{TLP} = 4A, tp = 100ns	V_{CL}	-	5.72	-	V
	I_{TLP} = 16A, tp = 100ns		-	9.51	-	V
Junction capacitance	1MHz, V_R = 0V	C_J	-	17	23	pF
Dynamic resistance(2)		R_{DYN}	-	0.32	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: Z_0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. RDYN is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	**PACKAGE**	**PACKING**
TESDL3V3B23P1Q0 M3G	DFN0603-2L	10,000 / 7" Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

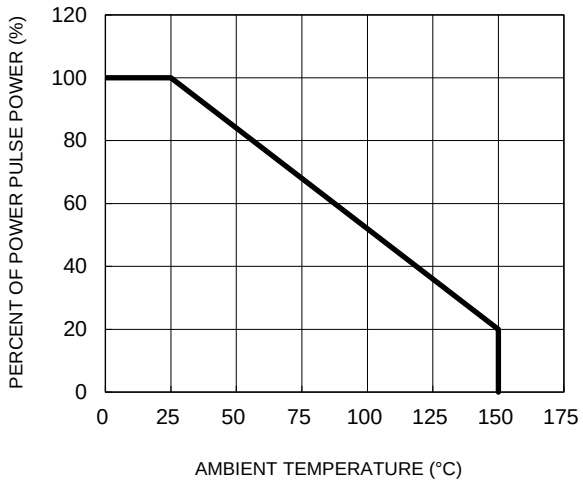


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

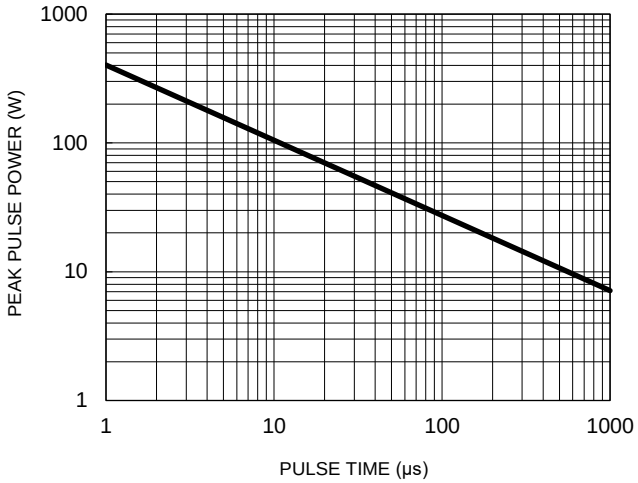


Fig.3 Clamping Voltage vs. Peak Pulse Current

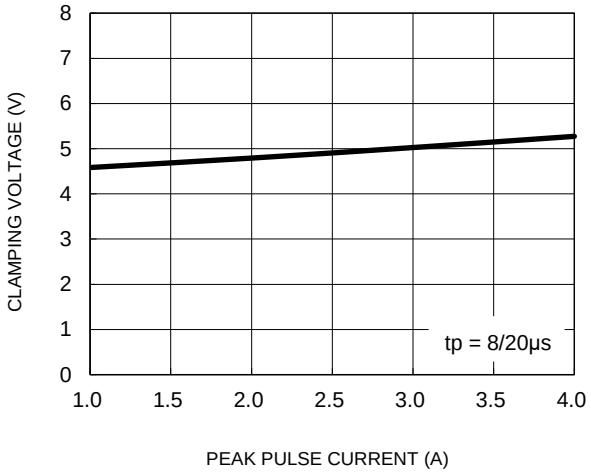


Fig.4 Capacitance vs. Reverse Voltage

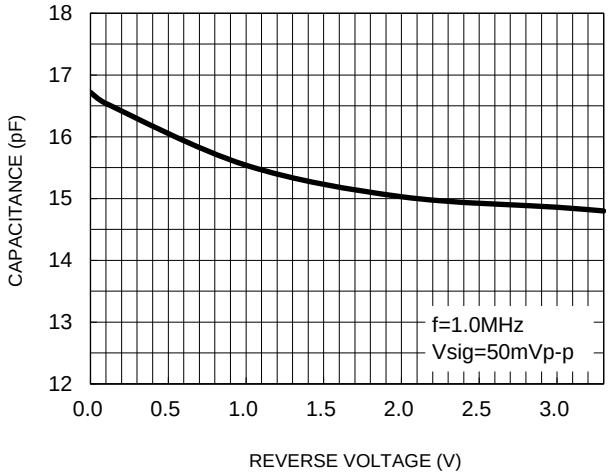
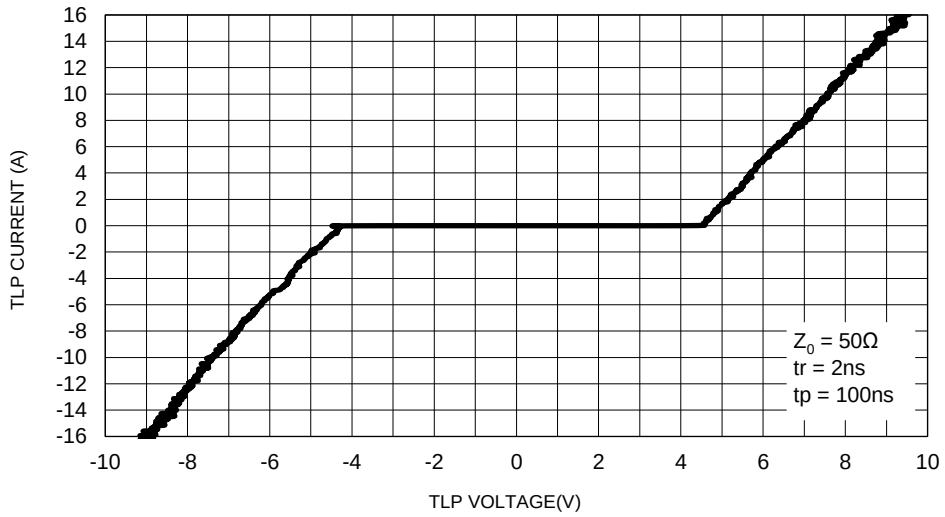


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 8/20μs pulse waveform per IEC61000-4-5

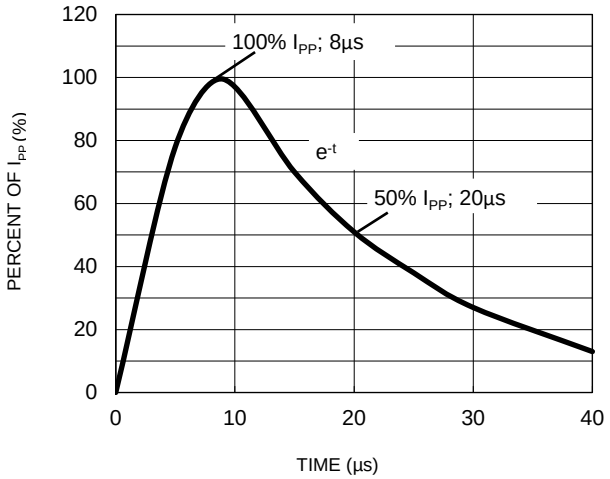
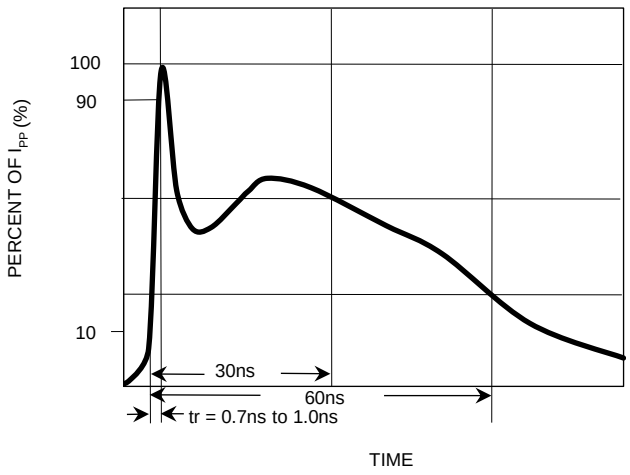


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

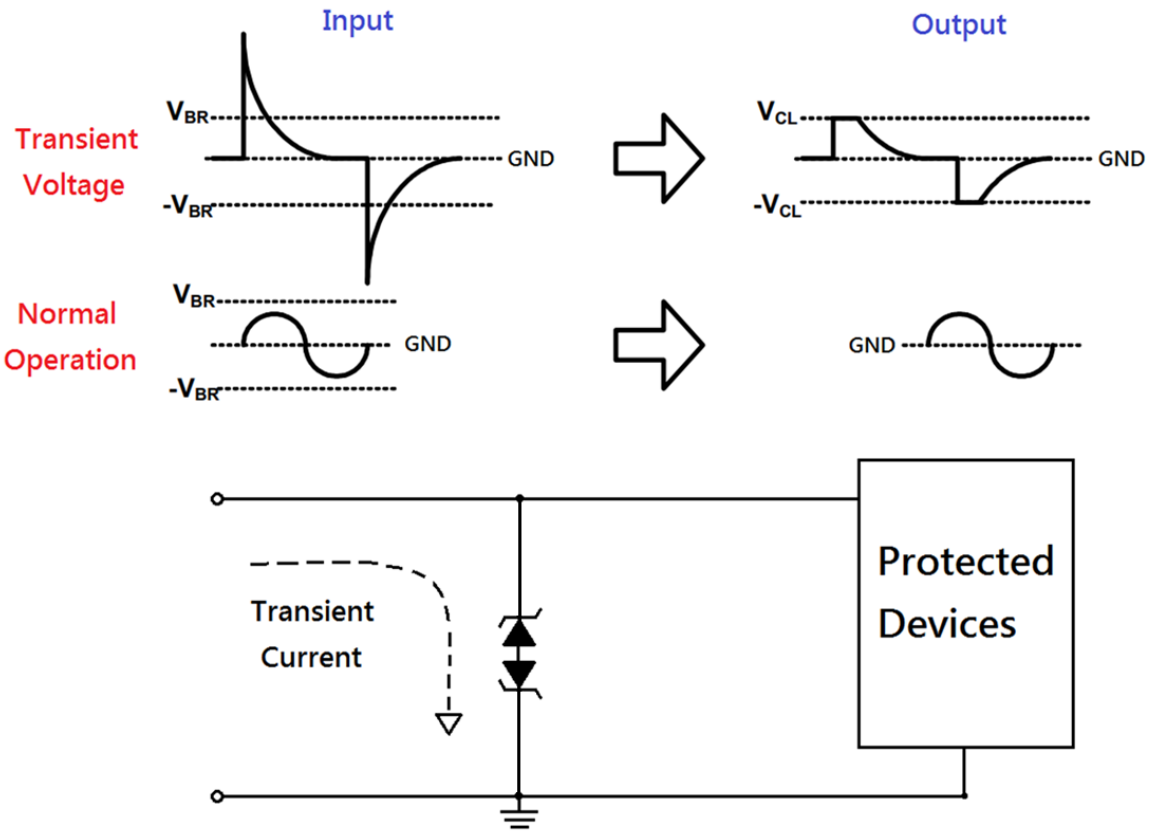
Device Connection

The TESDL3V3B23P1Q0 is designed to protect one line against system ESD Lightning pulses by clamping it to an acceptable reference. It provides bidirectional protection.
The usage of the TESDL3V3B23P1Q0 is shown in Fig1.Protected line, such as data line, control line, or power line. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of TESDL3V3B23P1Q0 should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

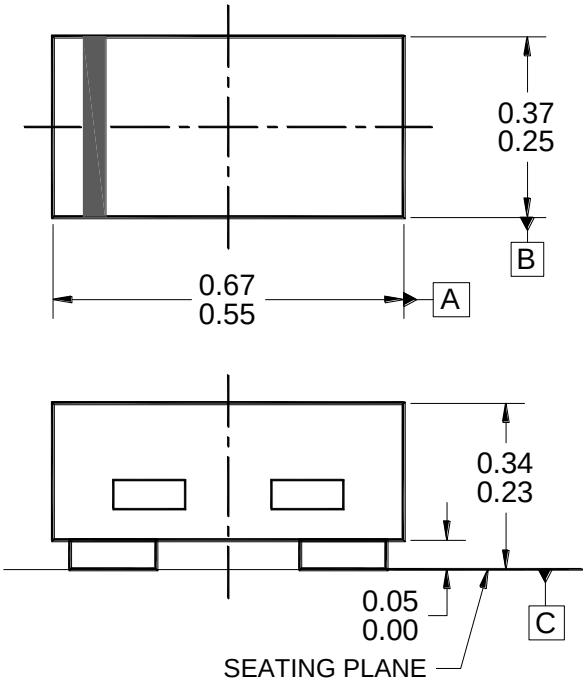
- Let the path length between the protected lines and the TESDL3V3B23P1Q0 minimize.
- Place the TESDL3V3B23P1Q0 near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

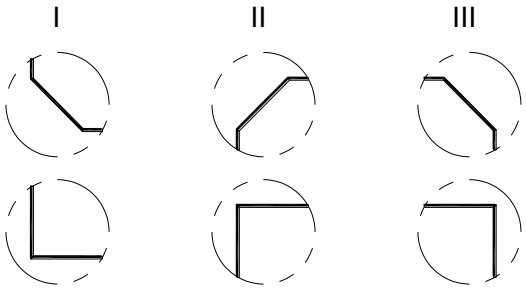
Fig.1 ESD protection by TESDL3V3B23P1Q0



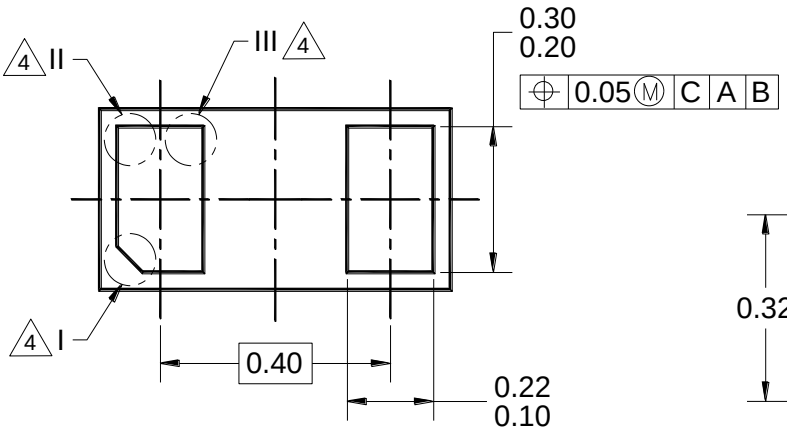
PACKAGE OUTLINE DIMENSIONS

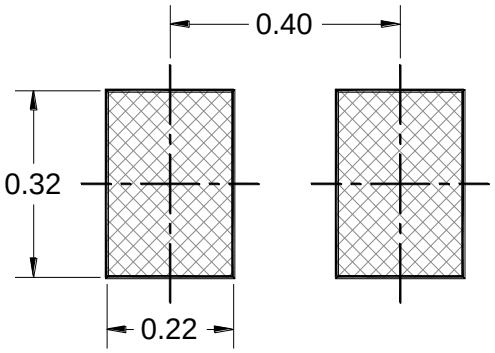
DFN0603-2L



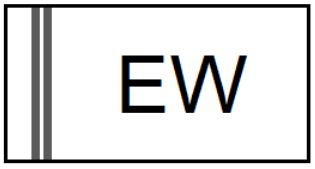


CATHODE TERMINAL
CORNER NOTCH OPTION





SUGGESTED PAD
LAYOUT



MARKING DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE SIZE CODE REFERENCE:
   EIA (inch) NAME: 0201 (0.024in x 0.012in)
   IEC (metric) NAME: 0603 (0.6mm x0.3mm)

4 CATHODE TERMINAL MAY HAVE CHAMFER NOTCH OR FULL 90 DEGREES CORNER.

5. DWG NO. REF: HQ2SD07-DFN0603-067 REV B.

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