

Small Signal Product

Ultra Low Capacitance ESD Protection Array

FEATURES

- Meet IEC61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Protects two directional I/O lines
- Working voltage: 5V
- Low leakage, low operating and clamping voltage
- Ultra low capacitance
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

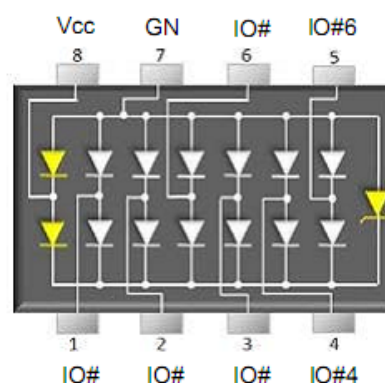


MSOP-08



MECHANICAL DATA

- Case: MSOP-08 small outline plastic package
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- Molding Compound Flammability Rating: UL 94V-0
- High temperature soldering guaranteed : 260°C/10s
- Weight: 25 \pm 0.5 mg
- Marking code: UC68M



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T _A =25°C unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20μs waveform)	P _{PP}	200	W
Peak Pulse Current (tp=8/20μs)	I _{PP}	6	A
ESD per IEC 61000-4-2 (Air)	V _{ESD}	± 15	KV
ESD per IEC 61000-4-2 (Contact)		± 8	
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

PARAMETER		SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage		V _{RWM}	-	5	V
Reverse Breakdown Voltage	I _R = 1 mA	V _(BR)	6.5	-	V
Reverse Leakage Current	V _R = 5 V	I _R	-	0.5	μA
Clamping Voltage	I _{PP} = 1 A	V _C	-	9.8	V
	I _{PP} = 6 A		-	15	
Junction Capacitance	V _R = 0 V , f = 1.0 MHz	C _J	0.5		pF

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RATINGS AND CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 Admissible Power Dissipation Curve

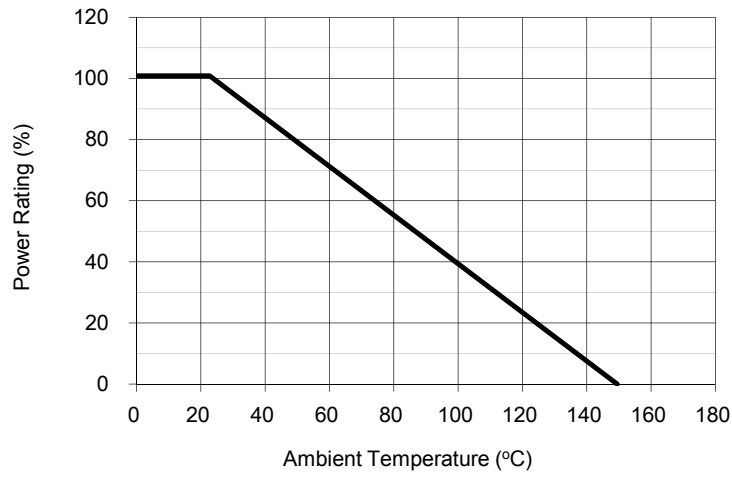


Fig. 2 Pulse Waveform

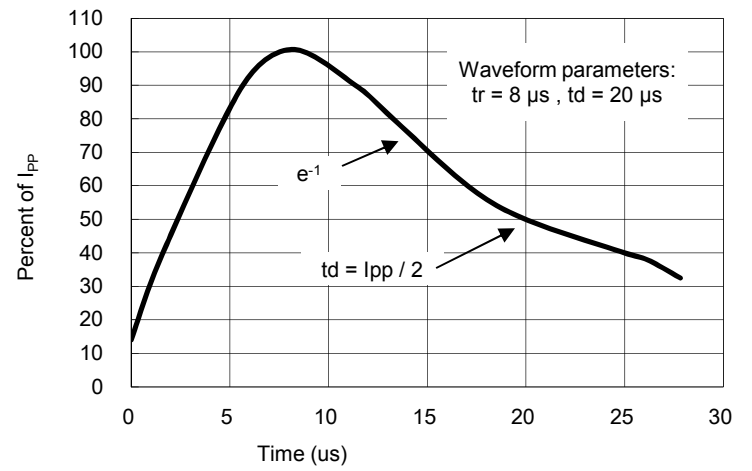


Fig. 3 Clamping Voltage VS. Peak Pulse Current

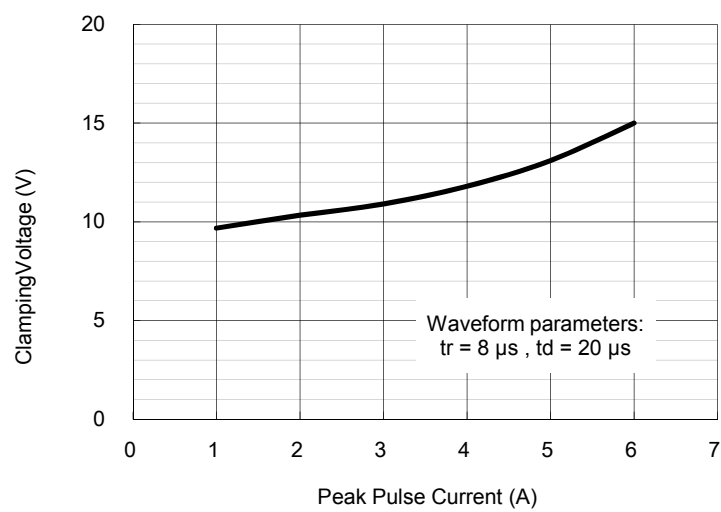
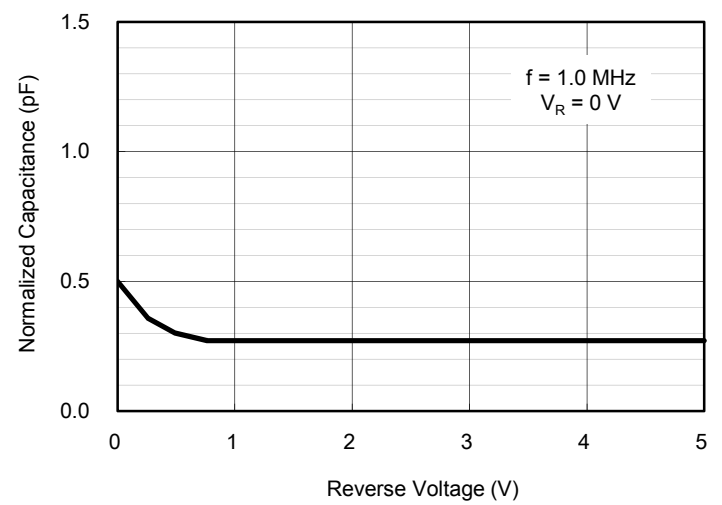


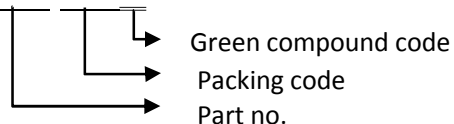
Fig. 4 Typical Junction Capacitance



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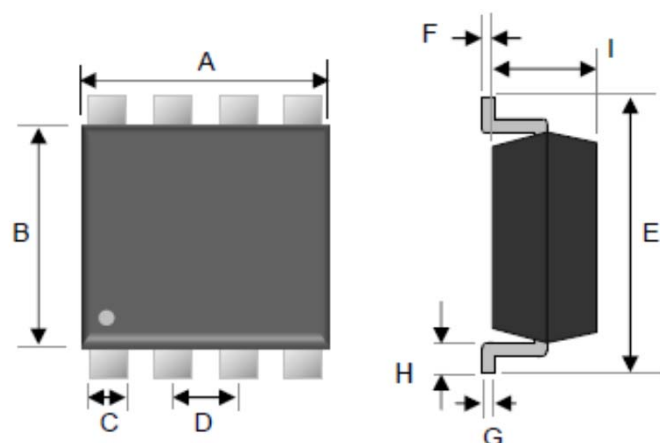
ORDER INFORMATION (EXAMPLE)

TESDM5V0A RMG



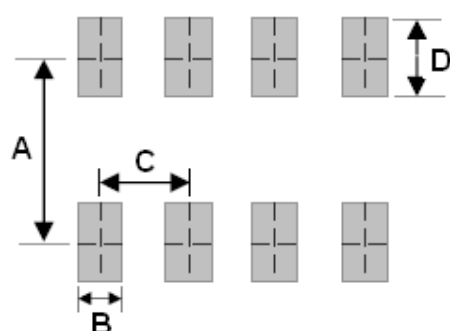
PACKAGE OUTLINE DIMENSIONS

MSOP-08



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.22	0.38	0.009	0.015
D	0.65 REF		0.0256 REF	
E	4.75	5.05	0.187	0.199
F	-	0.25	-	0.010
G	0.13	0.23	0.005	0.009
H	0.40	0.66	0.016	0.026
I	0.75	0.95	0.030	0.037

SUGGEST PAD LAYOUT



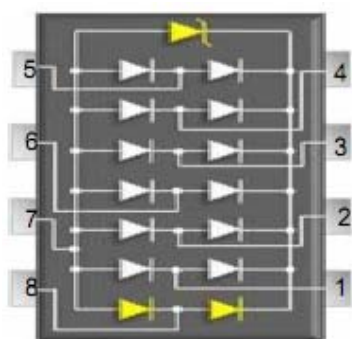
DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
A	4.80	0.189
B	0.41	0.016
C	0.65	0.026
D	1.02	0.040

Note: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

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APPLICATIONS INFORMATION

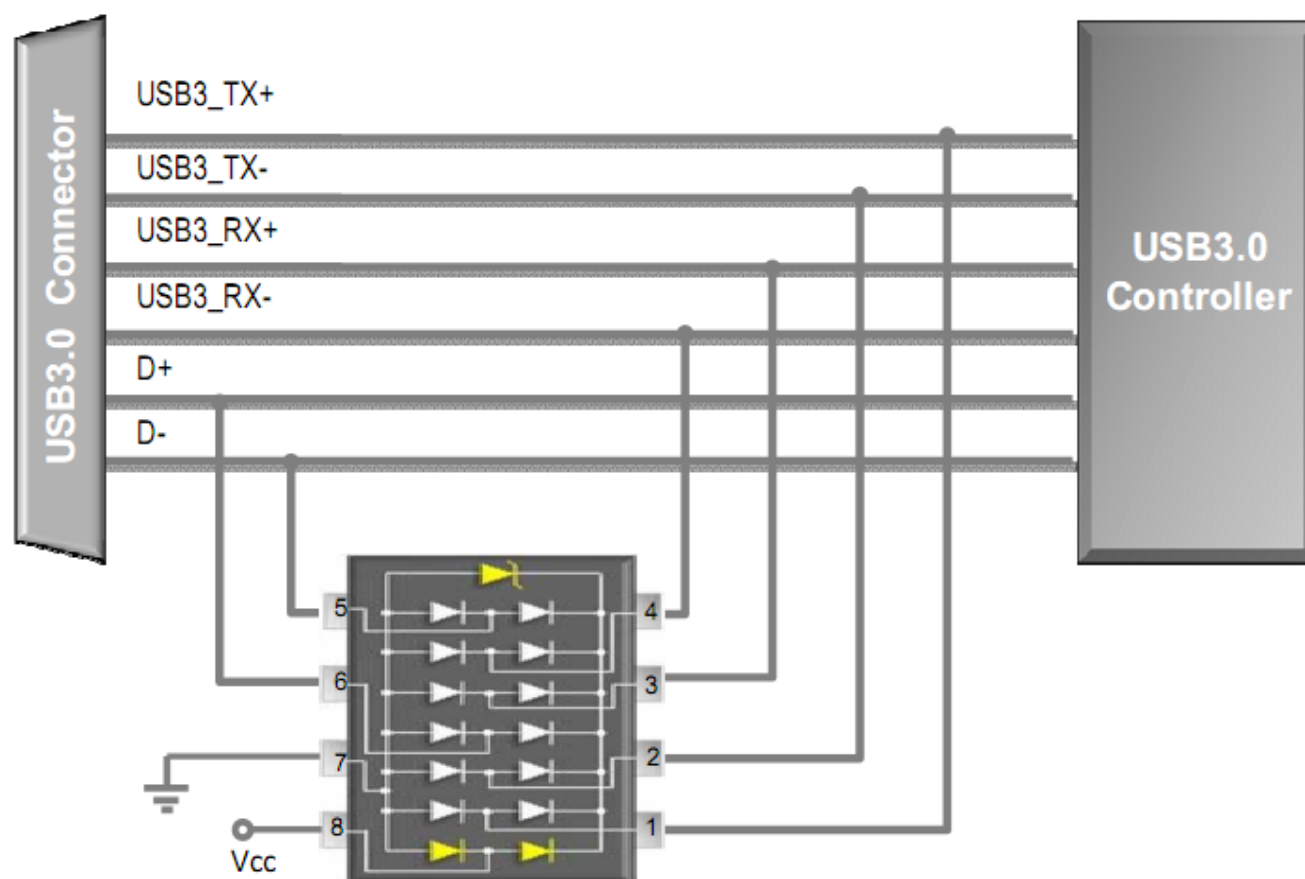
- Applications for Microprocess based equipment
- IEEE1394 Firewire Ports
- ATM Interfaces
- High Definition Multi-Media Interface(HDMI)
- Digital Video Interface (DVI)
- Video Graphs Cards
- Designed for protection of high-speed interfaces such as USB3.0
- Ultra low capacitance between the pairs while being rated to handle $>\pm 8\text{kV}$, ESD contact discharges and $>\pm 15\text{kV}$ air discharge
- TESDM5V0A is ultra low capacitance ESD protection array designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD, CDE (Cable Discharge Events), and EFT(electrical fast transients)



Pin	Definition
1, 2, 3, 4, 5, 6	I/O Lines
7	Ground
8	Vcc

TYPICAL APPLICATION

Schematic Diagram for USB 3.0 Protection



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