TFA9887

Audio system with adaptive sound maximizer and speaker protection

Rev. 1 — 11 July 2012 Product short data sheet

1. General description

The TFA9887 is an audio system consisting of a high efficiency class-D audio amplifier, and embedded DSP with a sophisticated speaker-boost and protection algorithm and an intelligent DC-to-DC converter. It can safely deliver 2.65 W (RMS; THD = 1 %) output power into a 4 Ω speaker that is nominally only rated for 0.5 W. The integrated intelligent DC-to-DC converter allows the system to deliver this power from a battery voltage of 3.6 V. The audio input interface is I^2S and the control settings are communicated via an I^2C-bus interface.

The TFA9887 guarantees safe speaker operation under all operating conditions. It maximizes acoustic output while ensuring diaphragm displacement and voice coil temperature do not exceed rated limits. The processing is capable of providing a significant improvement in sound volume and quality, while also ensuring reliable operation. This function is based on and adaptive model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures the quality of the audio signal is always optimized.

Adaptive DC-to-DC conversion boosts the supply voltage only when necessary (when the output signal level is high). This maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption. The TFA9887 also adapts the amplifier gain to limit battery current when the battery voltage is low.

The device features low RF susceptibility because it has a digital input interface that is insensitive to clock jitter. The second order closed loop architecture used in a class-D audio amplifier provides excellent audio performance and high supply voltage ripple rejection.

The TFA9887 is available in a 29-bump WLCSP (Wafer Level Chip-Size Package) with a 400 μm pitch.

2. Features and benefits

- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
  - Fully embedded software, no additional license fee or porting required.
  - Total integrated solution that includes DSP, amplifier, DC-to-DC, sensing and more.
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit

- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Output power: 2.65 W (RMS) into 4 Ω at 3.6 V supply voltage (THD = 1 %)
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Bandwidth extension option to increase low frequency response
- Intelligent DC-to-DC converter maximizes audio headroom from any supply level and limits current consumption at low battery voltages
- Compatible with standard Acoustic Echo Cancellers (AECs)
- High efficiency and low-power dissipation
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- Wide supply voltage range (fully operational from 2.5 V to 5.5 V)
- Two I^2S inputs to support two audio sources
- I^2C-bus control interface (400 kHz)
- Dedicated speech mode with speech activity detector
- Speaker current and voltage monitoring (via the I^2S-bus) for Acoustic Echo Cancellation (AEC) at the host
- Fully short-circuit proof across the load and to the supply lines
- Sample frequencies from 8 kHz to 48 kHz supported
- 3 bit clock/word select ratios supported (32x, 48x, 64x)
- Option to route I^2S input direct to I^2S output to allow a second I^2S output slave device to be used in combination with the TFA9887
- TDM interface supported
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- ‘Pop noise' free at all mode transitions

3. Applications

- Mobile phones
- Tablets
- Ultrabooks and Notebooks
- Portable gaming devices
- Portable Navigation Devices (PND)
- MP3 players and portable media players

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin V_{BAT} and in DC-to-DC converter coil; operating modes with load; DC-to-DC converter in Adaptive boost mode	-	1.55	-	mA
		on pin V_{BAT} and in DC-to-DC converter coil; Power-down mode	-	-	1	μA
I_{DDD}	digital supply current	on pin V_{DDD}; operating modes; speaker-boost and protection activated	-	20	-	mA
		on pin V_{DDD}; operating modes; CoolFlux DSP bypassed	-	4.8	-	mA
		on pin V_{DDD}; Power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V	-	10	-	μA
$P_{o(RMS)}$	RMS output power	CLIP = 00				
		R_L = 4 Ω; f_s = 48 kHz	-	2.55	-	W
		R_L = 4 Ω; f_s = 32 kHz	-	2.65	-	W
		R_L = 8 Ω; f_s = 48 kHz	-	1.5	-	W
		R_L = 8 Ω; f_s = 32 kHz	-	1.65	-	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9887UK	WLCSP29	wafer level chip-size package; 29 bumps; 3.19 × 2.07 × mm	TFA9887

6. Block diagram

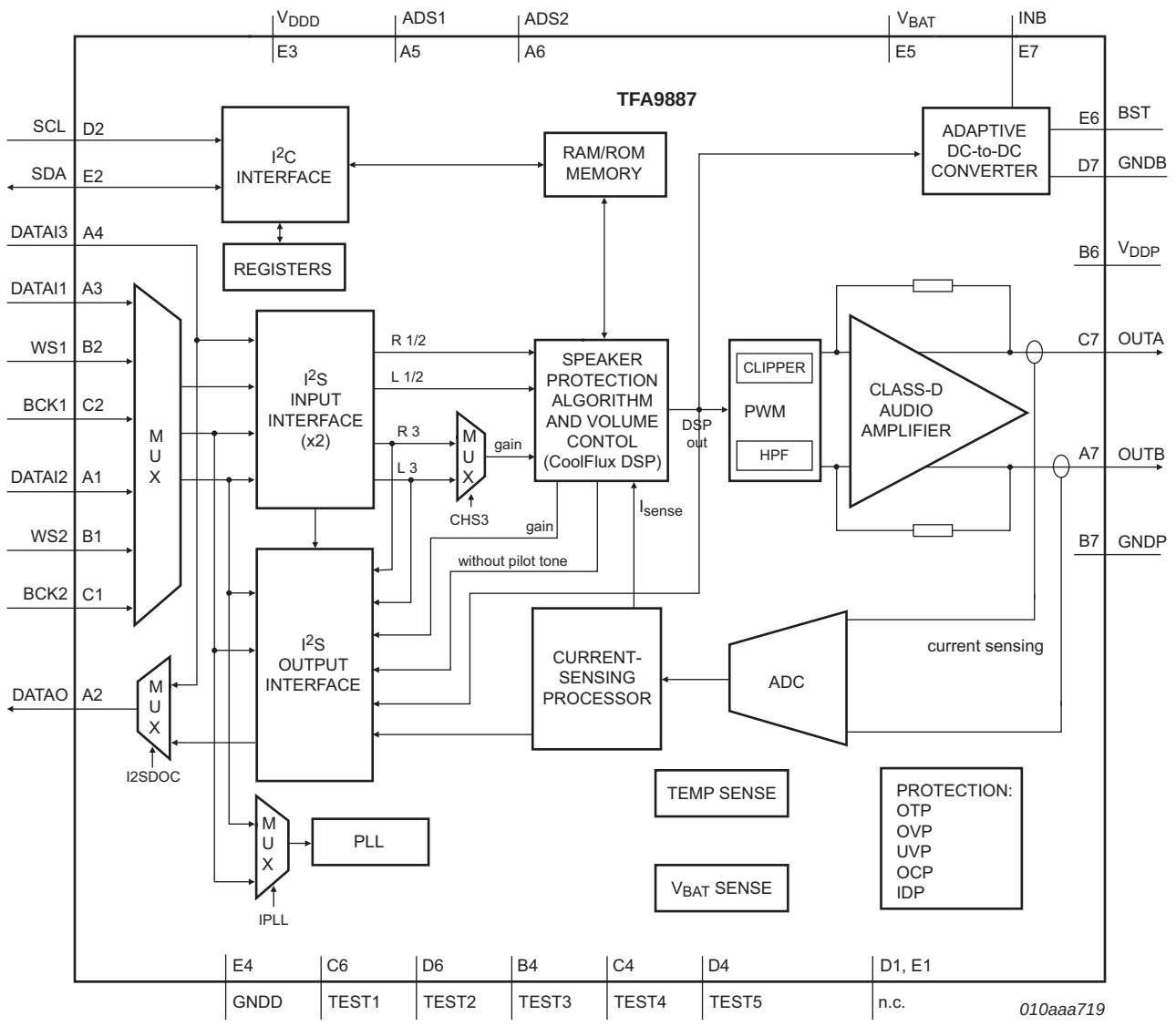
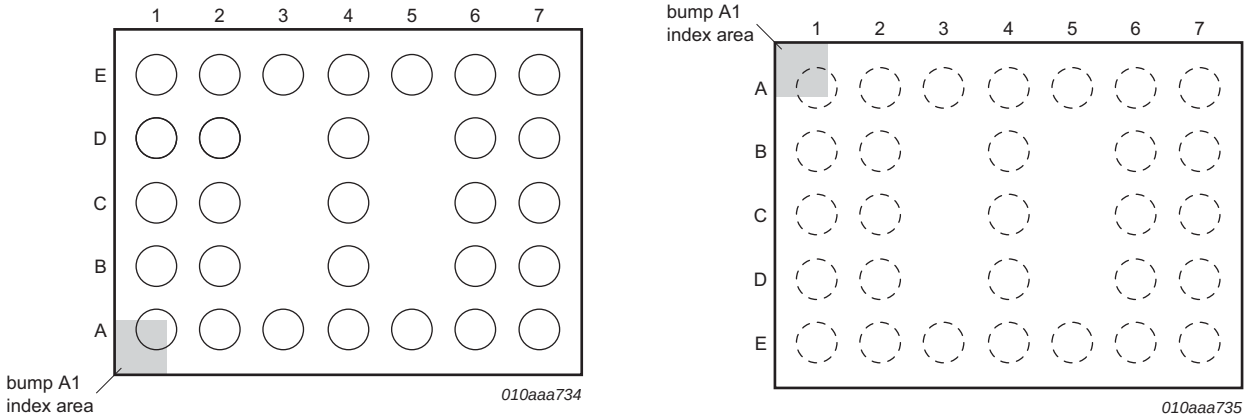


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



a. Bottom view

b. Transparent top view

Fig 2. Bump configuration

	1	2	3	4	5	6	7
A	DATAI2	DATAO	DATAI1	DATAI3	ADS1	ADS2	OUTB
B	WS2	WS1		TEST3		V_{DDP}	GNDP
C	BCK2	BCK1		TEST4		TEST1	OUTA
D	n.c.	SCL		TEST5		TEST2	GNDB
E	n.c.	SDA	V_{DDD}	GNDD	V_{BAT}	BST	INB

010aaa736

Transparent top view

Fig 3. Bump mapping

Table 3. Pinning

Symbol	Pin	Type	Description
DATAI2	A1	I	digital audio data input 2
DATAO	A2	O	digital audio data output
DATAI1	A3	I	digital audio data input 1
DATAI3	A4	I	digital audio data input 3
ADS1	A5	I	address select input 1
ADS2	A6	I	address select input 2
OUTB	A7	O	inverting output
WS2	B1	I	digital audio word select input 2
WS1	B2	I	digital audio word select input 1
	B3		
TEST3	B4	I	test signal input 3; for test purposes only, connect to PCB ground
	B5		
V_{DDP}	B6	P	power supply voltage
GNDP	B7	P	power ground
BCK2	C1	I	digital audio bit clock input 2
BCK1	C2	I	digital audio bit clock input 1
	C3		
TEST4	C4	O	test signal input 4; for test purposes only, connect to PCB ground
	C5		
TEST1	C6	I	test signal input 1; for test purposes only, connect to BST
OUTA	C7	O	non-inverting output
n.c.	D1	-	not connected; connect to D2 or to PCB ground
SCL	D2	I	I^2C-bus clock input
	D3		
TEST5	D4	I	test signal input 5; for test purposes only, connect to PCB ground
	D5		
TEST2	D6	I	test signal input 2; for test purposes only, connect to BST
GNDB	D7	P	boosted ground
n.c.	E1	-	not connected; connect to E2 or to PCB ground
SDA	E2	I/O	I^2C-bus data input/output
V_{DDD}	E3	P	digital supply voltage
GNDD	E4	P	digital ground
V_{BAT}	E5	I	battery supply voltage sense input
V_{BST}	E6	O	boosted supply voltage output
INB	E7	P	DC-to-DC boost converter input

8. Functional description

The TFA9887 is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated speaker-boost protection algorithm. Figure 1 is a block diagram of the TFA9887.

The device contains three I^2S input interfaces and one I^2S output interface. One of I^2S inputs DATAI1 and DATAI2 can be selected as the audio input stream. The third I^2S input, DATAI3, is provided to support stereo applications and the I^2S pass-through option. The pass-through option is provided to allow an I^2S output slave device (for example, a CODEC), connected in parallel with the TFA9887, to be routed directly to the audio host via the I^2S output.

The I^2S output signal on DATAO can be configured to transmit the DSP output signal, amplifier output current information, DATAI3 Left or Right signal information or amplifier gain information. The gain information can be used to facilitate communication between two devices in stereo applications.

The speaker-boost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of ±10 °C. Furthermore, advanced signal processing ensures the audio quality remains acceptable at all times.

The speaker-boost protection algorithm boosts the output sound pressure level within given mechanical, thermal and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high-quality music in quiet environments.

The frequency response of the TFA9887 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 8 are processed with 24-bit single precision.

At low battery voltage levels, the gain is automatically reduced to limit battery current.

The output volume can be controlled by the speaker-boost protection algorithm or by the host application (external). In the latter case, the boost features of the speaker-boost protection algorithm must be disabled to avoid neutralizing external volume control.

The speaker-boost protection algorithm output is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

The adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the speaker-boost protection algorithm. It switches to Follower mode ($V_{BST} = V_{BAT}$; no boost) when the audio output voltage is lower than the battery voltage.

8.1 Protection mechanisms

The following protection circuits are included in the TFA9887:

- OverTemperature Protection (OTP)

- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- OverCurrent Protection (OCP)
- Invalid Data Protection (IDP)

The reaction of the device to fault conditions differs depending on the protection circuit involved.

8.1.1 OverTemperature Protection (OTP)

OTP prevents heat damage to the TFA9887. It is triggered when the junction temperature exceeds $T_{act(th\_prot)}$. When this happens, the output stages are set floating. OTP is cleared automatically via an internal timer (approximately 200 ms), after which the output stages will start to operate normally again.

8.1.2 Supply voltage protection (UVP and OVP)

UVP is activated, setting the outputs floating, if V_{BAT} drops below the undervoltage protection threshold, $V_{P(uvp)}$. When the supply voltage rises above $V_{P(uvp)}$ again, the system will be restarted after approximately 200 ms.

OVP is activated, setting the power stages floating, if the power supply voltage (V_{DDP}) rises above the overvoltage protection threshold, $V_{P(ovp)}$. The power stages are re-enabled as soon as the supply voltage drops below $V_{P(ovp)}$ again. The system will be restarted after approximately 200 ms.

8.1.3 OverCurrent Protection (OCP)

OCP will detect a short circuit across the load or between one of the amplifier outputs and one of the supply lines. If the output current exceeds the overcurrent protection threshold ($I_{O(ocp)}$), it will be limited to $I_{O(ocp)}$ while the amplifier outputs are switching (the amplifier is not powered down completely). This is called current limiting. The amplifier can distinguish between an impedance drop at the loudspeaker and a low-ohmic short circuit across the load or to one of the supply lines. The impedance threshold depends on which supply voltage is being used:

8.1.4 Invalid Data Protection (IDP)

IDP checks if the word select signal is correctly connected to the TFA9887. It the bit clock/word select (BCK-to-WS) ratio is not stable, the IDP alarm is raised and the TFA9887 powers down.The TFA9887 starts up again automatically when the BCK-to-WS ratio stabilizes.

8.2 Battery supply voltage monitor

The voltage level at the battery connected to the TFA9887 can be monitored via the I^2C-bus. Status bits BATS in the Battery status register.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	–0.3	+5.5	V
V_{DDP}	power supply voltage	on pin V_{DDP}	–0.3	+5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	–0.3	+1.95	V
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	–2	+2	kV
		according to Charge Device Model (CDM)	–500	+500	V

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; natural convection	-	
		4-layer application board	60	K/W

11. Characteristics

11.1 DC Characteristics

Table 6. DC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 5.3 V; L_{BST} = 1 µH[1]; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	2.5	-	5.5	V
V_{DDP}	power supply voltage	on pin V_{DDP}	2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin V_{BAT} and in the DC-to-DC converter coil; operating modes with load; DC-to-DC converter in Adaptive boost mode	-	1.55	-	mA
		on pin V_{BAT} and in the DC-to-DC converter coil; Power-down mode	-	-	1	µA
I_{DDD}	digital supply current	on pin V_{DDD}; operating modes; speaker-boost protection activated	-	20	-	mA
		on pin V_{DDD}; operating modes; CoolFlux DSP bypassed	-	4.8	-	mA
		on pin V_{DDD}; Power-down mode; BCK1 = WS1 = DATAI1 = BCK2 = WS2 = DATAI2 = DATAI3 = 0 V	-	10	-	µA
Pins BCK1, WS1, DATA1, BCK2, WS2, DATAI2, DATAI3, ADS1, ADS2, SCL, SDA						
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	-	3.6	V

Table 6. DC characteristics *...continued*

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 5.3 V; L_{BST} = 1 µH[1]; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDD}$	V
C_{in}	input capacitance		-	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin	-	-	0.1	µA
Pins DATAO, SDA						
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA	-	-	V_{DDD} − 0.4	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	400	mV
Pins OUTA, OUTB						
R_{DSon}	drain-source on-state resistance	V_{DDP} = 5.3 V	-	100	-	mΩ
Protection						
$T_{act(th\_prot)}$	thermal protection activation temperature		130	-	150	°C
$V_{P(ovp)}$	overvoltage protection supply voltage	protection on V_{DDP}	5.5	-	6.0	V
$V_{P(uvp)}$	undervoltage protection supply voltage	protection on V_{BAT}	2.3	-	2.5	V
$I_{O(ocp)}$	overcurrent protection output current		1.45	-	-	A
DC-to-DC converter						
V_{BST}	voltage on pin BST	DCVO = 111; Boost mode	5.25	5.3	5.35	V

[1] L_{BST} = boot converter inductance; R_L = load resistance; L_L = load inductance (speaker).

11.2 AC characteristics

Table 7. AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 5.3 V; L_{BST} = 1 µH[1]; R_L = 4 Ω[1]; L_L = 20 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier output power						
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; CLIP = 00				
		R_L = 4 Ω; f_s = 48 kHz	-	2.55	-	W
		R_L = 4 Ω; f_s = 32 kHz	-	2.65	-	W
		R_L = 8 Ω; f_s = 48 kHz	-	1.5	-	W
		R_L = 8 Ω; f_s = 32 kHz	-	1.65	-	W
		THD+N = 10 %; CLIP = 00				
		R_L = 4 Ω; f_s = 48 kHz	-	3.75	-	W
		R_L = 4 Ω; f_s = 32 kHz	-	3.75	-	W
		R_L = 8 Ω; f_s = 48 kHz	-	2	-	W
		R_L = 8 Ω; f_s = 32 kHz	-	2	-	W
Amplifier output; pins OUTA and OUTB						
$\lvert V_{O(offset)} \rvert$	output offset voltage	absolute value	-	-	1	mV
Amplifier performance						
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)}$ = 100 mW; R_L = 8 Ω; L_L = 44 µH	-	0.03	0.1	%
$V_{n(o)}$	output noise voltage	A-weighted; DATAI1 = DATAI2 = 0 V				
		CoolFlux DSP bypassed	-	31	-	µV
		CoolFlux DSP enabled	-	45	-	µV
S/N	signal-to-noise ratio	V_O = 4.5 V (peak); A-weighted				
		CoolFlux DSP bypassed	-	100	-	dB
		CoolFlux DSP enabled	-	97	-	dB
PSRR	power supply rejection ratio	V_{ripple} = 200 mV (RMS); f_{ripple} = 217 Hz	-	90	-	dB
Amplifier power-up, power-down and propagation delays						
$t_{d(on)}$	turn-on delay time	PLL locked on BCK (IPLL = 0)				
		f_s = 8 kHz to 48 kHz	-	-	2	ms
		PLL locked on WS (IPLL = 1)				
		f_s = 48 kHz	-	-	6	ms
$t_{d(off)}$	turn-off delay time		-	-	10	µs
$t_{d(mute\_off)}$	mute off delay time		-	1	-	ms
$t_{d(soft\_mute)}$	soft mute delay time		-	1	-	ms

[1] L_{BST} = boot converter inductance; R_L = load resistance; L_L = load inductance (speaker).

12. Application information

12.1 Application diagram

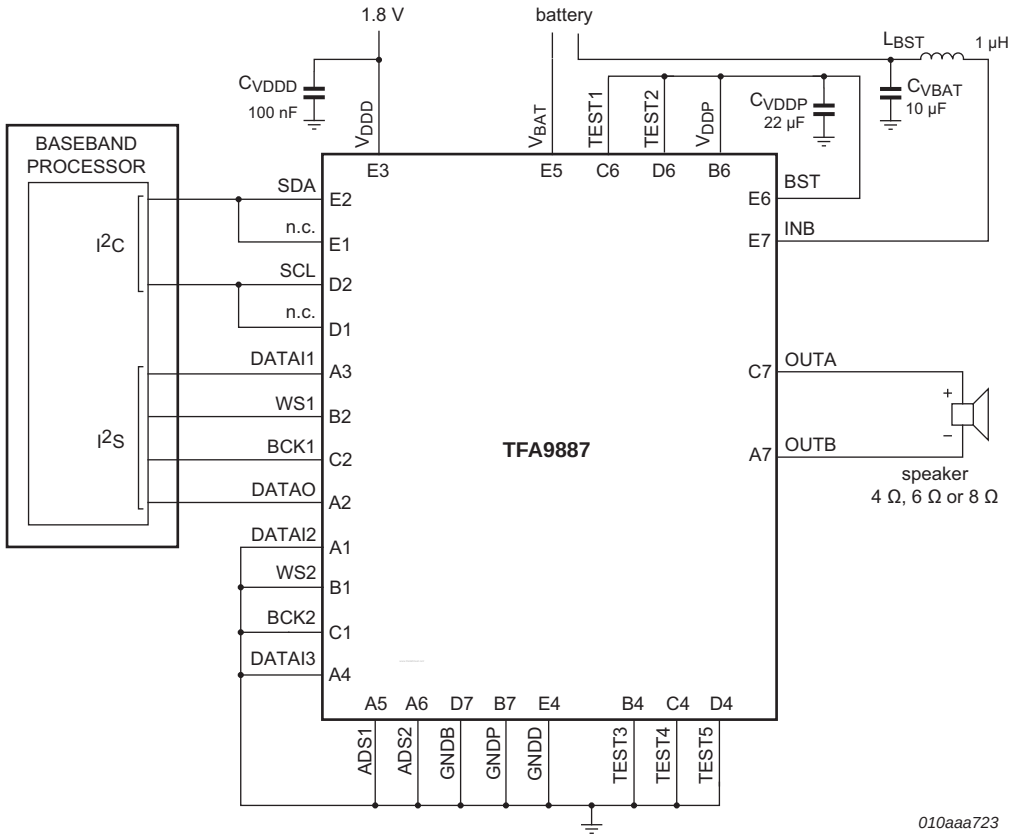
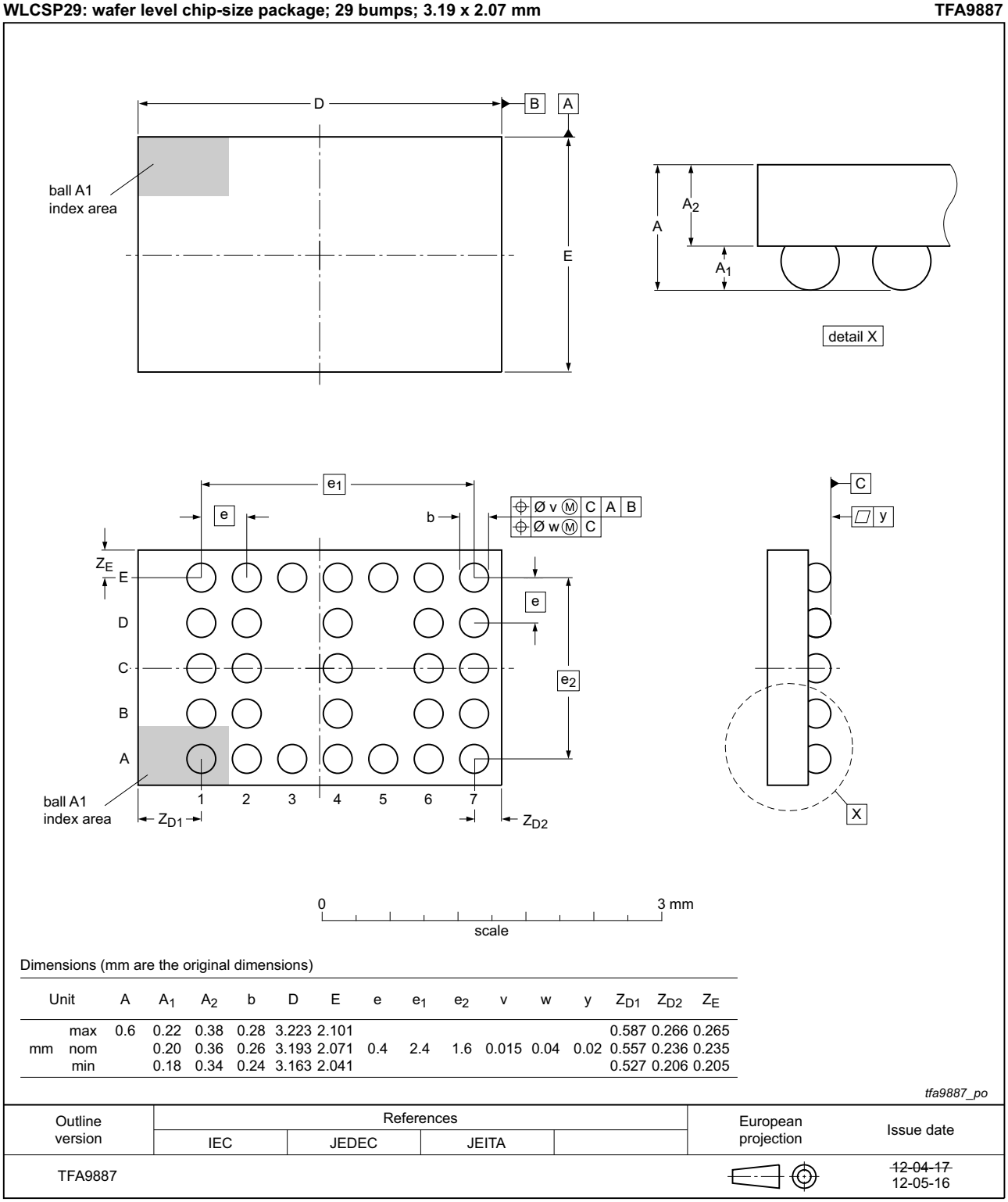


Fig 4. Typical mono application (simplified)

13. Package outline

WLCSP29: wafer level chip-size package; 29 bumps; 3.19 x 2.07 mm **TFA9887**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	Z_{D1}	Z_{D2}	Z_E
	max	0.6	0.22	0.38	0.28	3.223	2.101							0.587	0.266	0.265
mm	nom		0.20	0.36	0.26	3.193	2.071	0.4	2.4	1.6	0.015	0.04	0.02	0.557	0.236	0.235
	min		0.18	0.34	0.24	3.163	2.041							0.527	0.206	0.205

tfa9887_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
TFA9887						~~12-04-17~~ 12-05-16

Fig 5. Package outline TFA9887 (WLCSP29)

14. Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

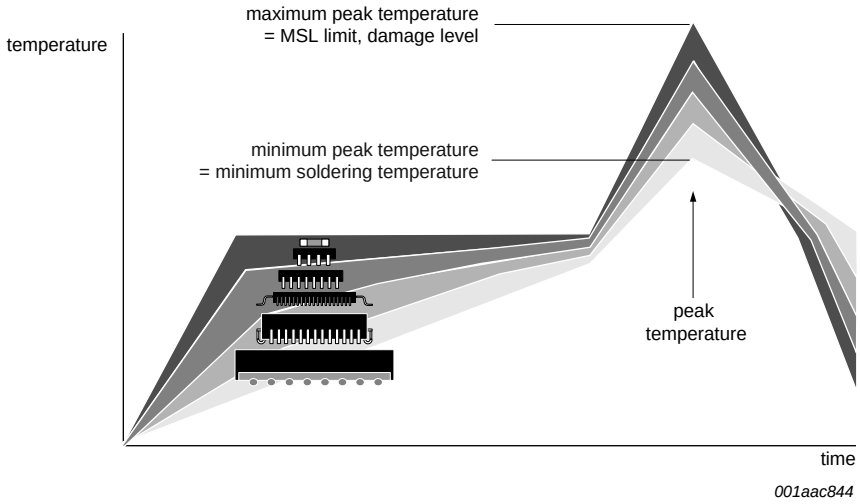
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 6) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8.

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 6.



MSL: Moisture Sensitivity Level

Fig 6. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9887_SDS v.1	20120711	Product short data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

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