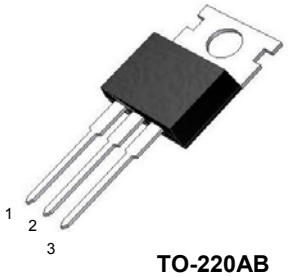
TAK CHEONG ®

SEMICONDUCTOR

N-Channel Power MOSFET

70A, 60V, 0.014Ω

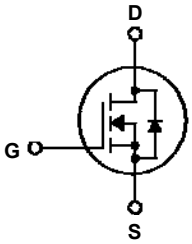


1 = Gate
2 = Drain
3 = Source

TO-220AB

DEVICE MARKING DIAGRAM

L = Tak Cheong Logo
xxyy = Monthly Date Code
TFPXXXX = Device Type



GENERAL DESCRIPTION

This N-Channel MOSFET is used an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance. This device is well suited for high efficiency switched mode power suppliers, active power factor correction, electronic lamp ballasts based half bridge topology.

FEATURES

- Avalanche energy specified
- Gate Charge (Typical 70nC)
- High Ruggedness

ABSOLUTE MAXIMUM RATINGS (T_C =25°C, unless otherwise noted)

Symbol	Parameter		Value	Units
V_{DSS}	Drain- Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±25	V
I_D	Drain Current		70	A
I_{DM}	Drain Current Pulsed		280	A
P_D	Power Dissipation	(Note 2)	158	W
	Derating Factor above 25℃		1.05	W/℃
E_{AS}	Single Pulsed Avalanche Energy	(Note 1)	800	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
T_J	Operating Junction Temperature		150	℃
T_{stg}	Storage Temperature Range		- 55 to +150	℃

Notes:

1. L=250uH, I_{AS}=70A, V_{DD}=25V, R_G=0Ω, Starting T_J=25℃.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. I_{SD} ≤ 70A, di/dt ≤ 300A/us, V_{DD} ≤ BV_{DSS}, Starting T_J=25℃.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.95	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	℃/W

ELECTRICAL CHARACTERISTICS

Off Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Sounce Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60V, V_{GS} = 0V	--	--	1	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 25V, V_{DS} = 0V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -25V, V_{DS} = 0V	--	--	-100	nA

On Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 250uA	2.0	--	4.0	V
$R_{DS(ON)}$	On-Resistance	V_{GS} = 10V, I_D = 35A	--	--	0.014	Ω

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ciss	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	--	2350	3050	pF
Coss	Output Capacitance		--	690	890	pF
Crss	Reverse Transfer Capacitance		--	160	200	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30V, I_D = 35A, R_G = 50 Ω (Note 4 & 5)	--	30	70	nS
tr	Turn-On Rise Time		--	60	130	nS
$t_{d(off)}$	Turn-Off Delay Time		--	125	260	nS
tr	Turn-Off Fall Time		--	95	200	nS
Qg	Total Gate Charge	V_{DS} = 48V, I_D = 70A, V_{GS} = 10V (Note 4 & 5)	--	70	90	nC
Qgs	Gate-Source Charge		--	18	--	nC
Qgd	Gate-Drain Charge		--	24	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min.	Typ,	Max.	Unit
I_S	Continuous Drain-Source Current	Integral Reverse p-n Junction Diode in the MOSFET	--	--	70	A
I_{SM}	Pulsed Drain-Source Current		--	--	280	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 70A	--	--	1.5	V
Trr	Reverse Recovery Time	V_{GS} = 0V, I_S = 70A, dI_F / dt = 100A/uS (Note 4)	--	62	--	nS
Qrr	Reverse Recovery Charge		--	110	--	uC

Notes:
4. Pulse Test: Pulse width < 300us, Duty cycle ≤ 2%.
5. Basically not affected by working temperature.

TYPICAL CHARACTERISTICS

Fig 1. On-State Characteristics

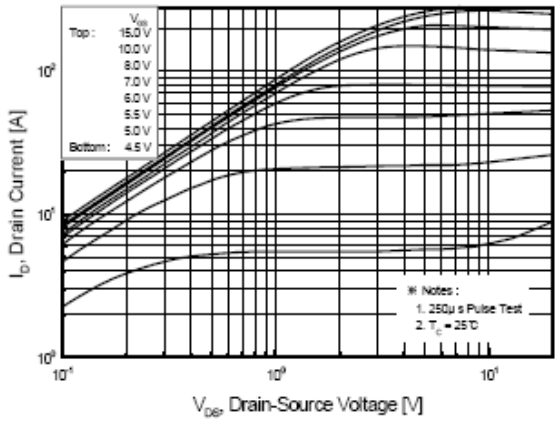


Fig 2. Transfer Characteristics

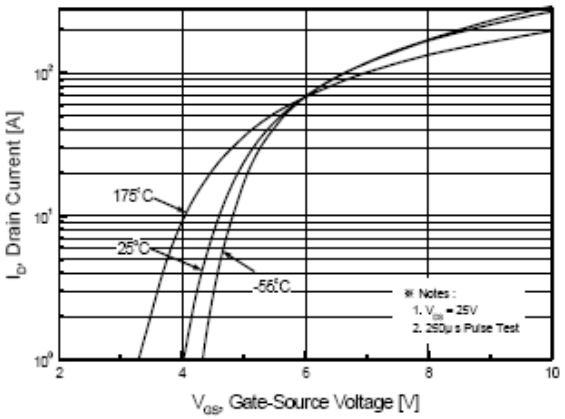


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

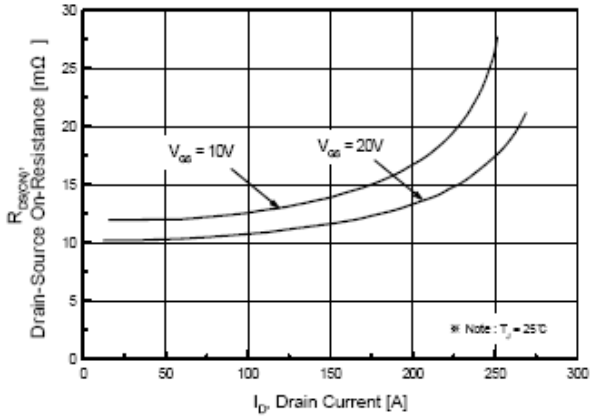


Fig 4. On State Current vs. Allowable Case Temperature

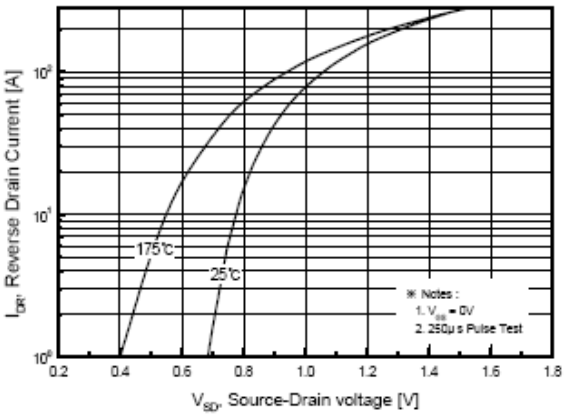


Fig 5. Capacitance Characteristics

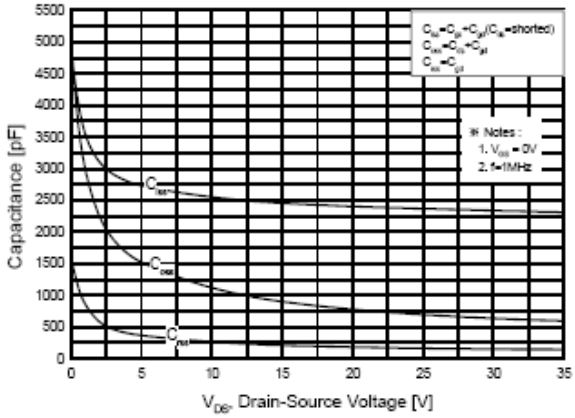


Fig 6. Gate Charge Characteristics

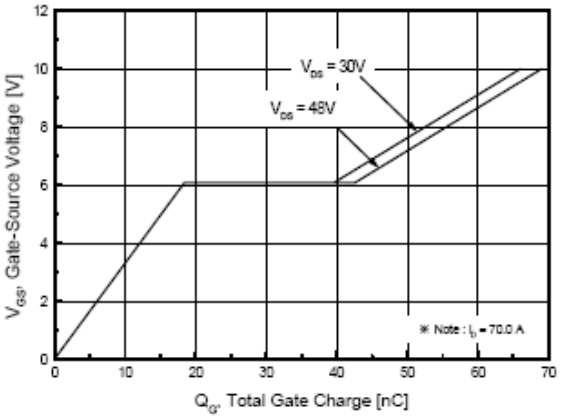


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

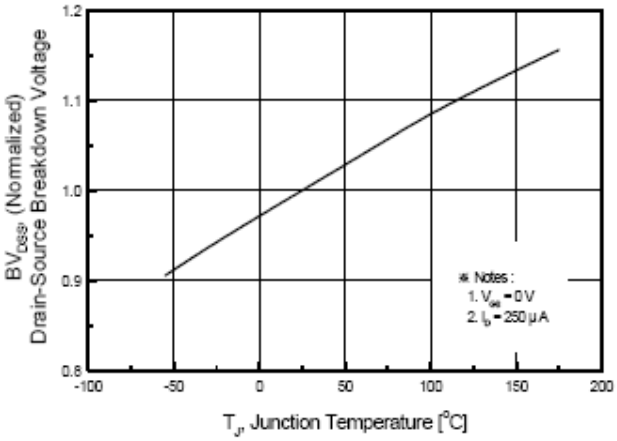


Fig 8. On-Resistance Variation vs. Junction Temperature

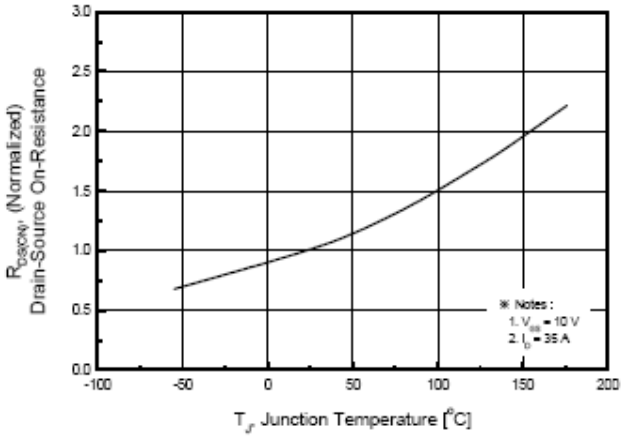


Fig 9. Maximum Safe Operating Area

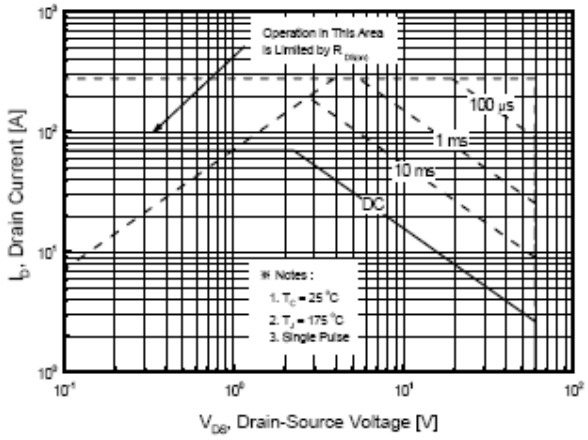


Fig 10. Maximum Drain Current vs. Case Temperature

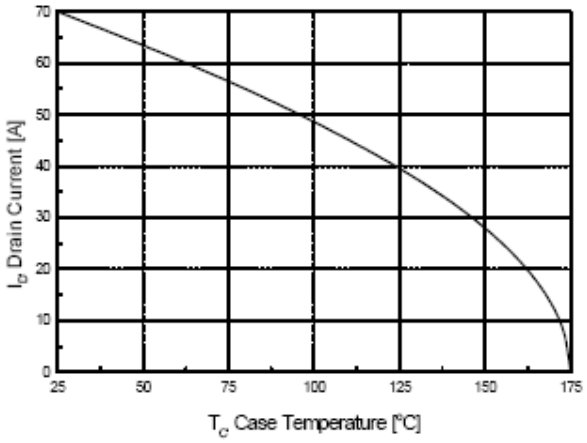


Fig 11. Transient Thermal Response Curve

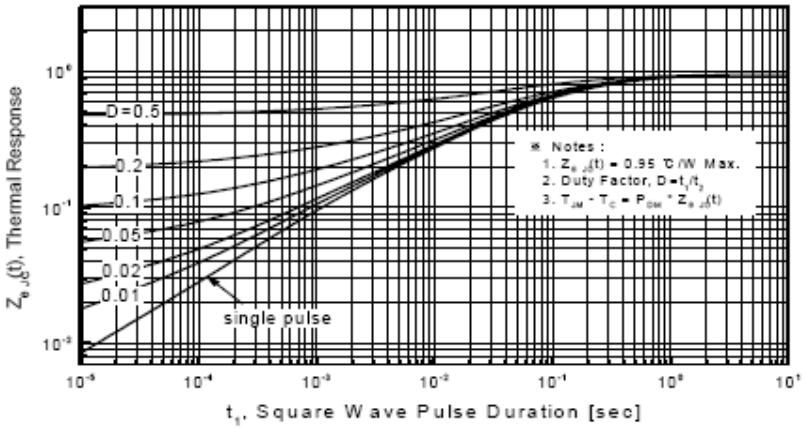


Fig. 12. Gate Charge Test Circuit & Waveforms

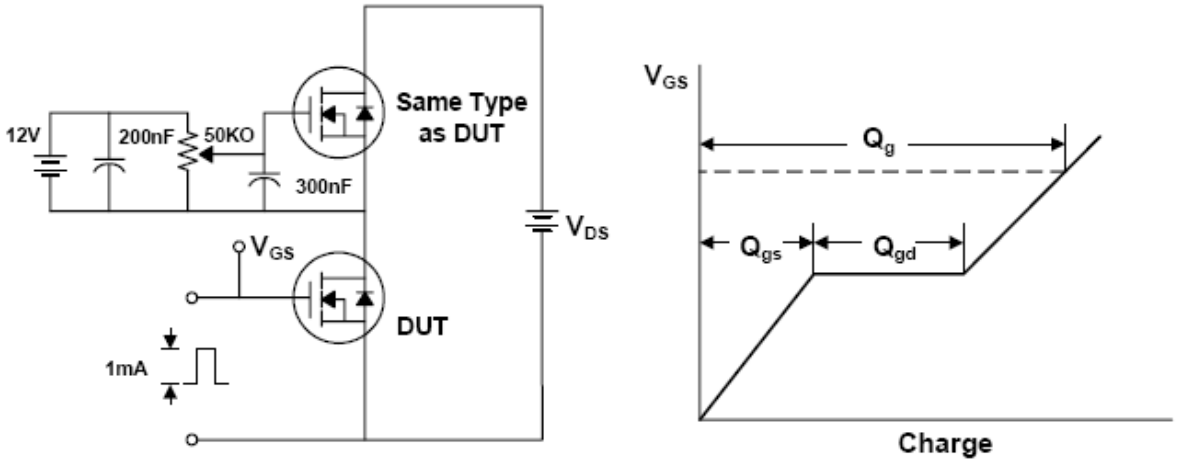


Fig 13. Switching Time Test Circuit & Waveforms

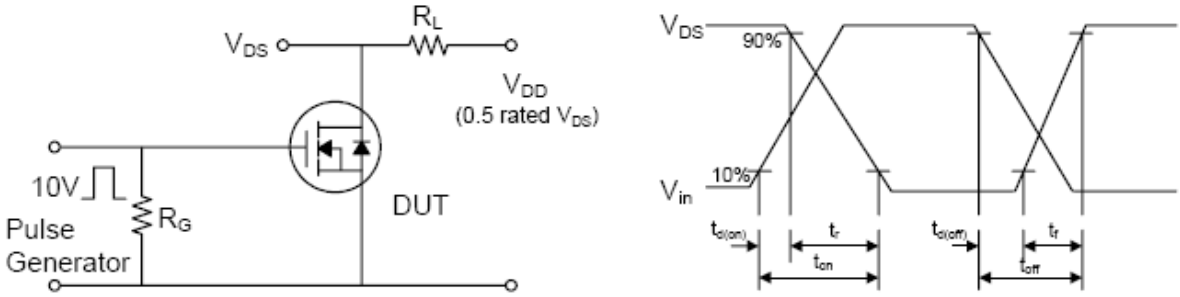


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

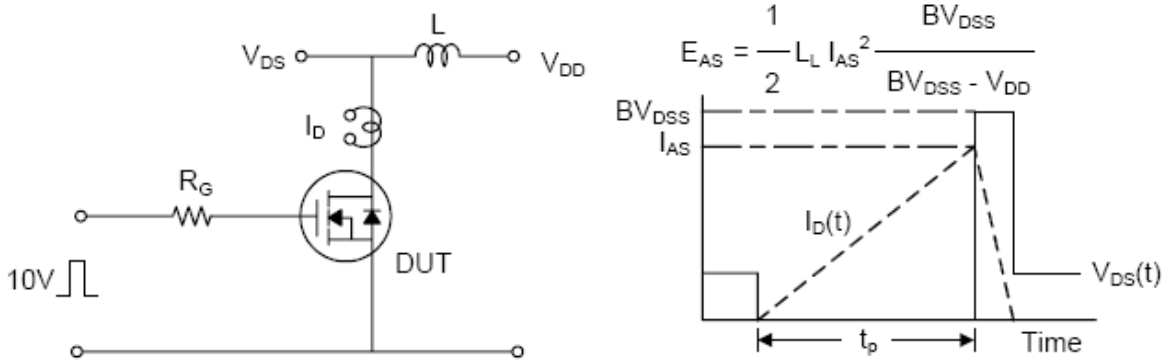
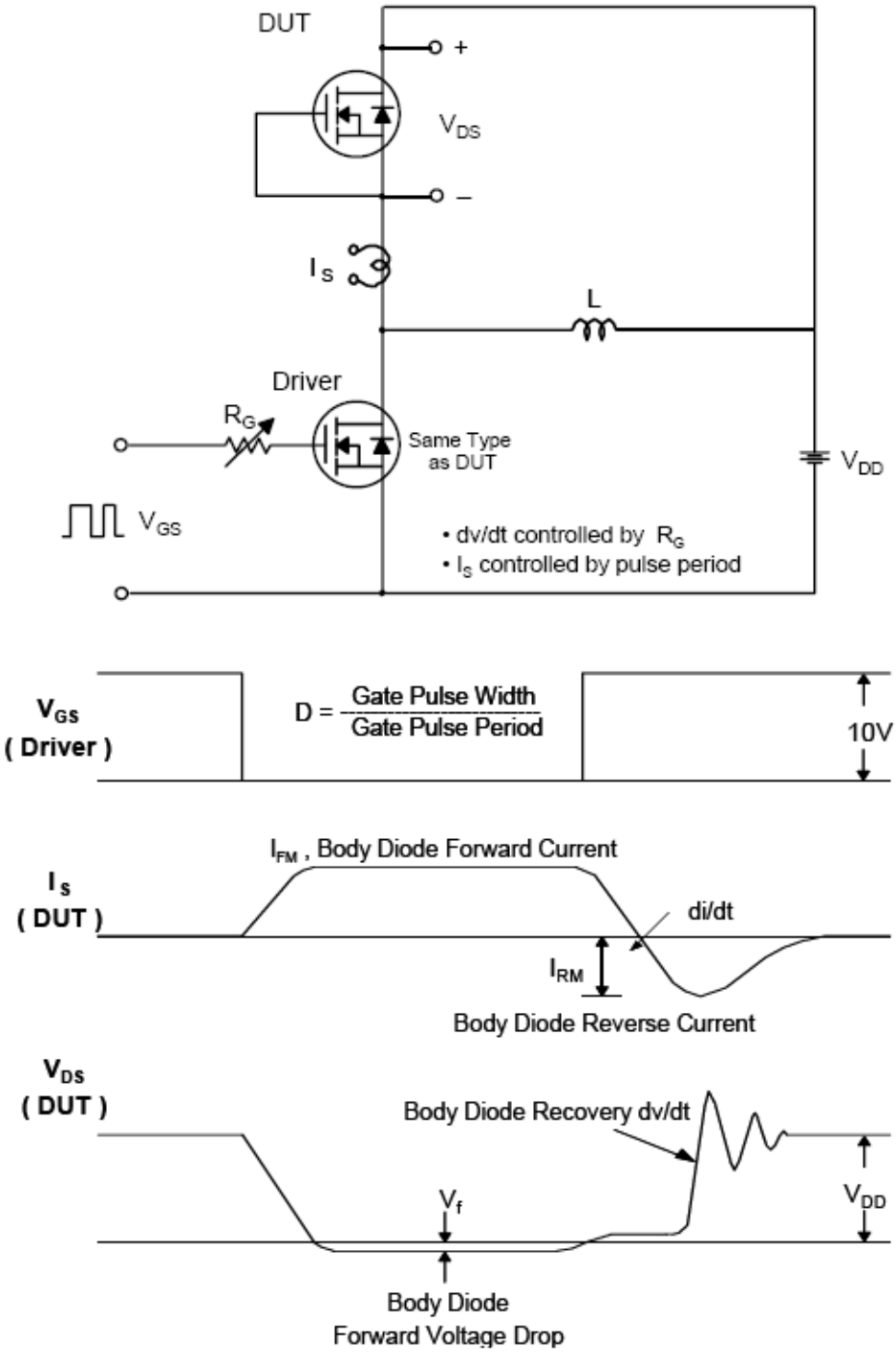
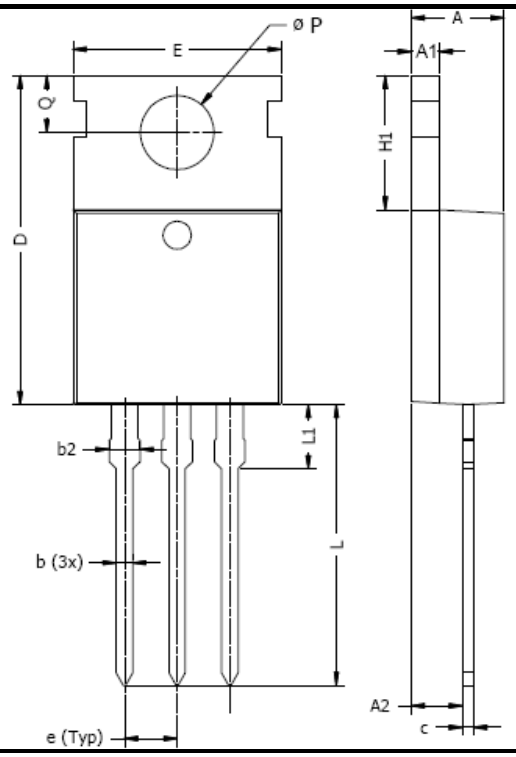


Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO220AB PACKAGE OUTLINE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.60	4.80	0.142	0.189
A1	1.20	1.40	0.047	0.055
A2	2.03	2.90	0.080	0.114
b	0.40	1.00	0.016	0.039
b2	1.20	1.78	0.047	0.070
c	0.36	0.60	0.014	0.024
D	14.22	16.50	0.560	0.650
e	2.34	2.74	0.092	0.108
E	9.70	10.60	0.382	0.417
H1	5.84	6.85	0.230	0.270
L	12.70	14.70	0.500	0.579
L1	2.70	3.30	0.106	0.130
ØP	3.50	4.00	0.138	0.157
Q	2.54	3.40	0.100	0.134

NOTE: Above package outline conforms to JEDEC TO-220AB

NOTICE

The information presented in this document is for reference only. Tak Cheong reserves the right to make changes without notice for the specification of the products displayed herein.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Tak Cheong Semiconductor Co., Ltd., or anyone on its behalf, assumes no responsibility or liability for any damagers resulting from such improper use of sale.

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