

N-Channel Power MOSFET

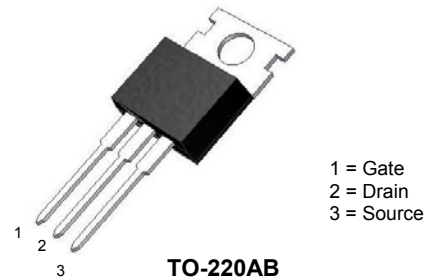
7.2A, 650V, 1.5Ω

General Description

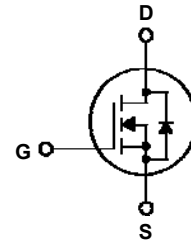
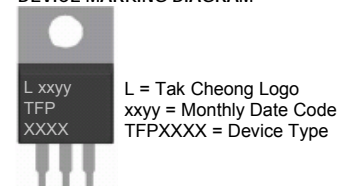
The N-Channel MOSFET is used an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance. This device is well suited for high efficiency switched mode power suppliers, active power factor correction, electronic lamp ballasts based half bridge topology.

Features

- Robust high voltage termination
- Avalanche energy specified
- Diode is characterized for use in bridge circuits
- Source to Drain diode recovery time comparable to a discrete fast recovery diode.



TO-220AB



ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

Symbol	Parameter	Value	Units
V _{DSS}	Drain- Source Voltage	650	V
V _{GSS}	Gate-Source Voltage	±30	V
I _D	Drain Current	7.2	A
I _{DM}	Drain Current Pulsed	28.8	A
P _D	Power Dissipation (Note 2)	137	W
	Derating factor above 25°C	1.1	W/°C
E _{AS}	Single Pulsed Avalanche Energy (Note 1)	274	mJ
E _{AR}	Repetitive Avalanche Energy (Note 2)	13.7	mJ
T _J	Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature Range	- 55 to +150	°C

Notes:

1. L=9mH, I_{AS}=7.2A, V_{DD}=50V, R_G=50 Ω, Starting T_J=25°C
2. Repetitive Rating: Pulse width limited by maximum junction temperature.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	0.91	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

ELECTRICAL CHARACTERISTICS
Off Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650V, V_{GS} = 0V$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30V, V_{DS} = 0V$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30V, V_{DS} = 0V$	--	--	-100	nA

On Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
$R_{DS(ON)}$	On-Resistance	$V_{GS} = 10V, I_D = 3.6A$	--	0.9	1.5	Ω

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	--	1150	1490	pF
C_{oss}	Output Capacitance		--	110	145	pF
C_{rss}	Reverse Transfer Capacitance		--	30	39	pF

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 325V, I_D = 7.2A,$ $R_G = 25\Omega$ (Note 3 & 4)	--	24	58	nS
t_r	Turn-On Rise Time		--	60	130	nS
$t_{d(off)}$	Turn-Off Delay Time		--	100	210	nS
t_f	Turn-Off Fall Time		--	64	138	nS
Q_g	Total Gate Charge	$V_{DS} = 520V, I_D = 7.2A,$	--	35	46	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10V$	--	5.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 3 & 4)	--	15	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.2	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	28.8	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 7.2A$	--	--	1.5	V
T_{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_S = 7.2A,$ $dI_F / dt = 100A/\mu S$	--	500	--	nS
Q_{rr}	Reverse Recovery Charge	(Note 3)	--	2.8	--	μC

Notes:

- Pulse Test: Pulse width < 300 μs , Duty cycle $\leq 2\%$.
- Basically not affected by working temperature.

TYPICAL CHARACTERISTICS

Fig 1. On-State Characteristics

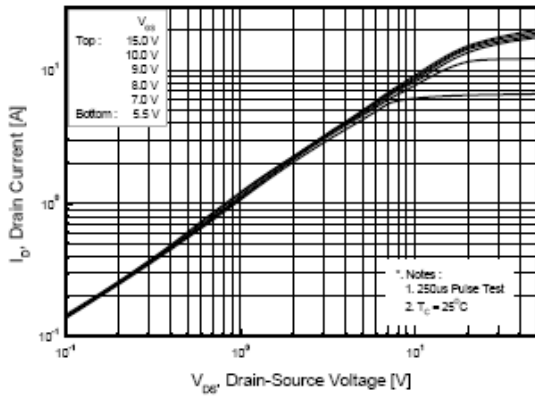


Fig 2. Transfer Characteristics

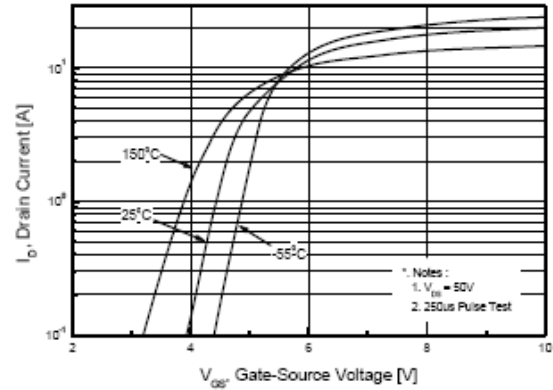


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

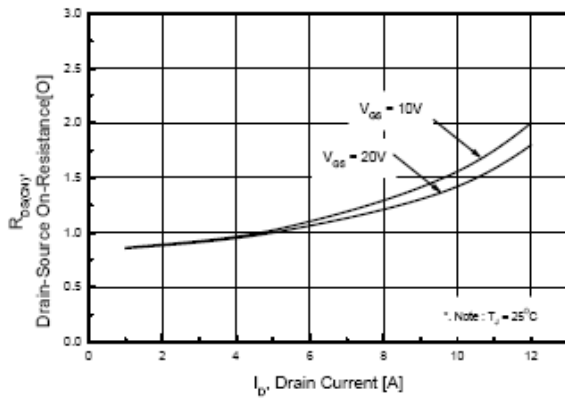


Fig 4. On State Current vs. Allowable Case Temperature

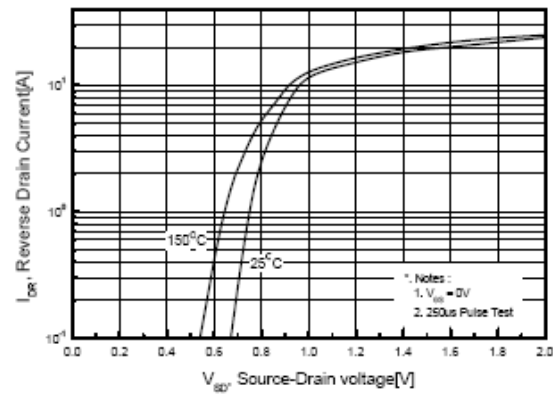


Fig 5. Capacitance Characteristics

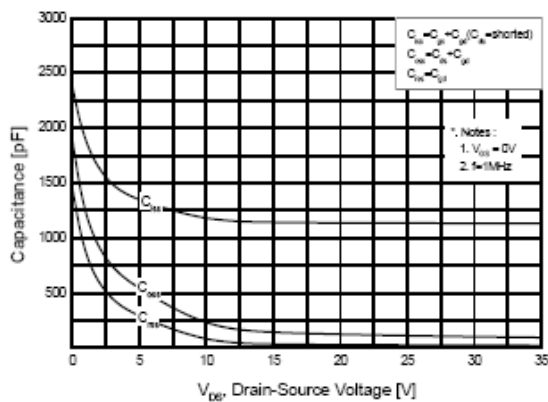


Fig 6. Gate Charge Characteristics

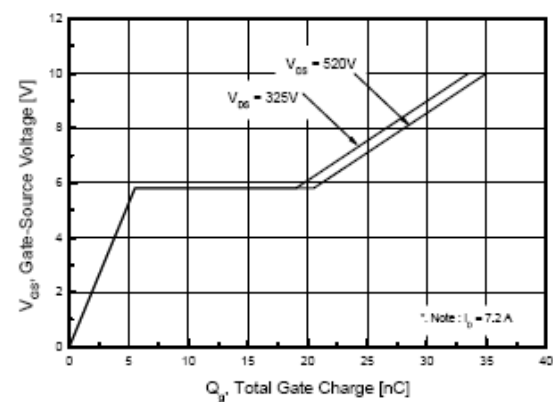


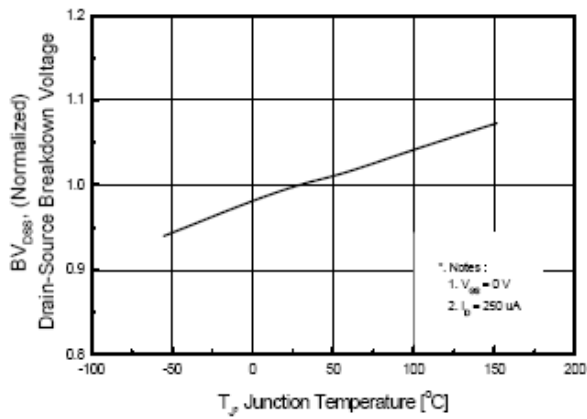
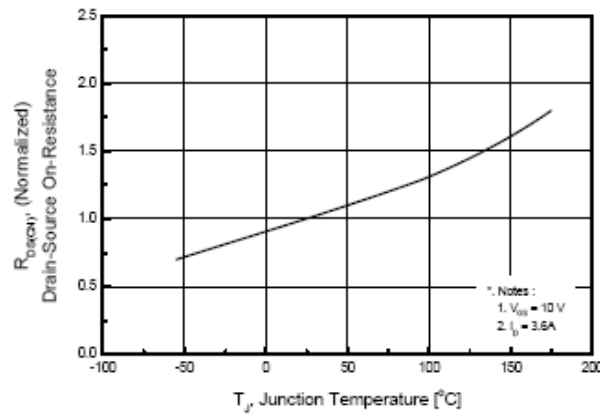
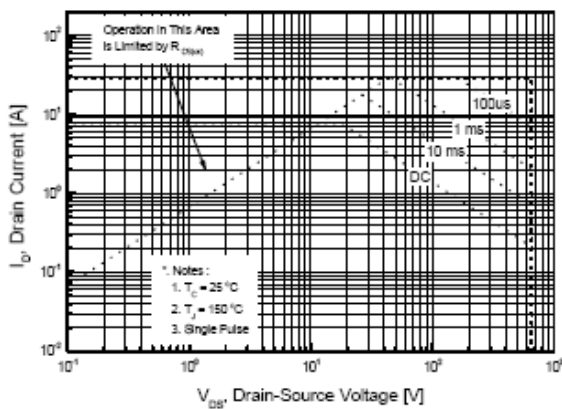
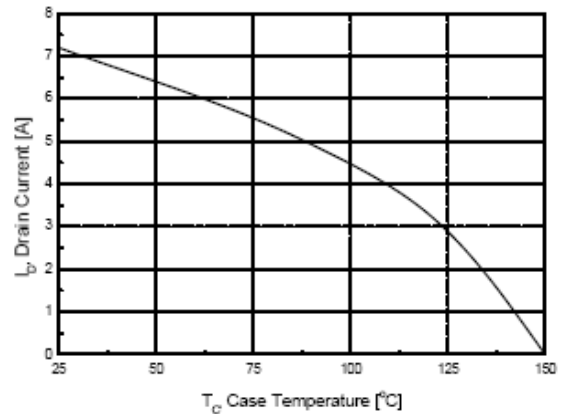
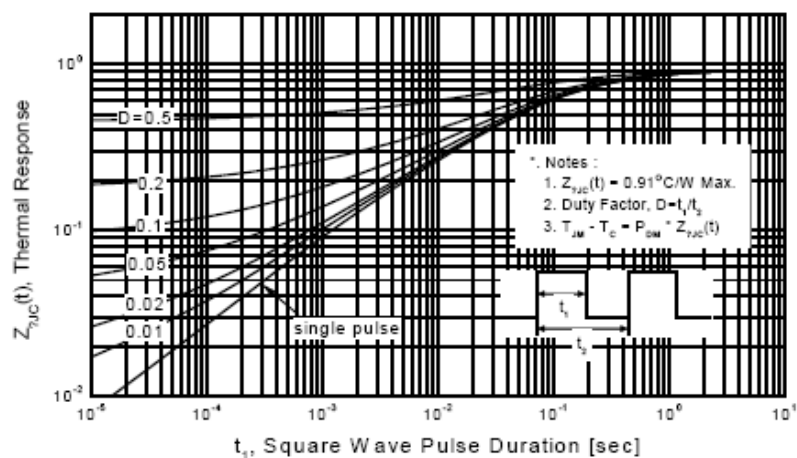
Fig 7. Breakdown Voltage Variation vs. Junction Temperature

Fig 8. On-Resistance Variation vs. Junction Temperature

Fig 9. Maximum Safe Operating Area

Fig 10. Maximum Drain Current vs. Case Temperature

Fig 11. Transient Thermal Response Curve


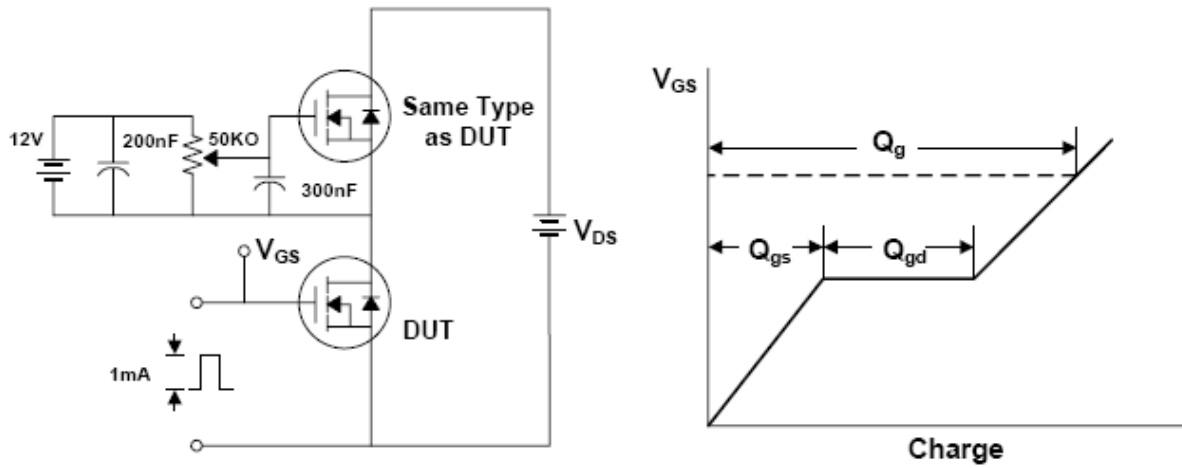
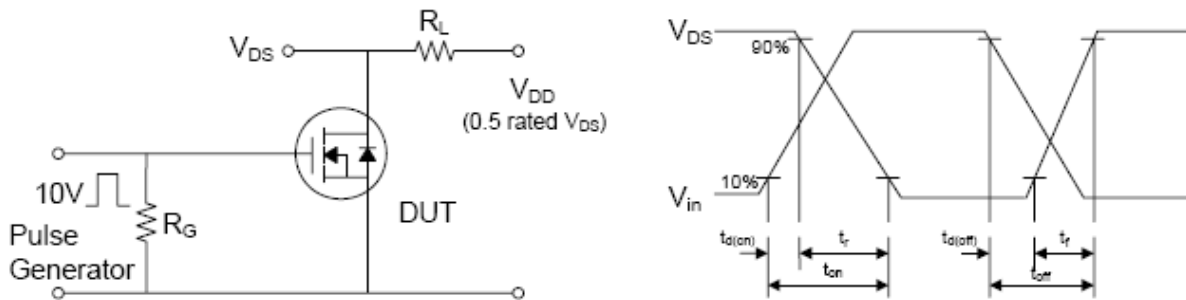
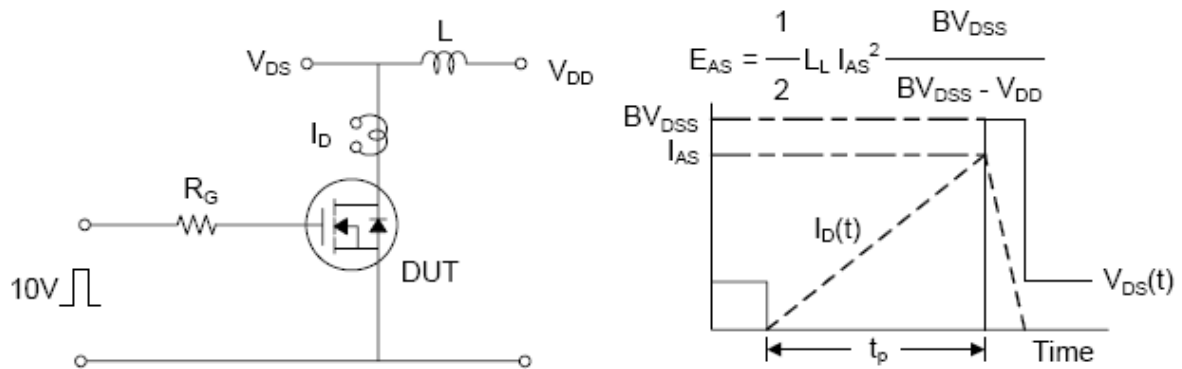
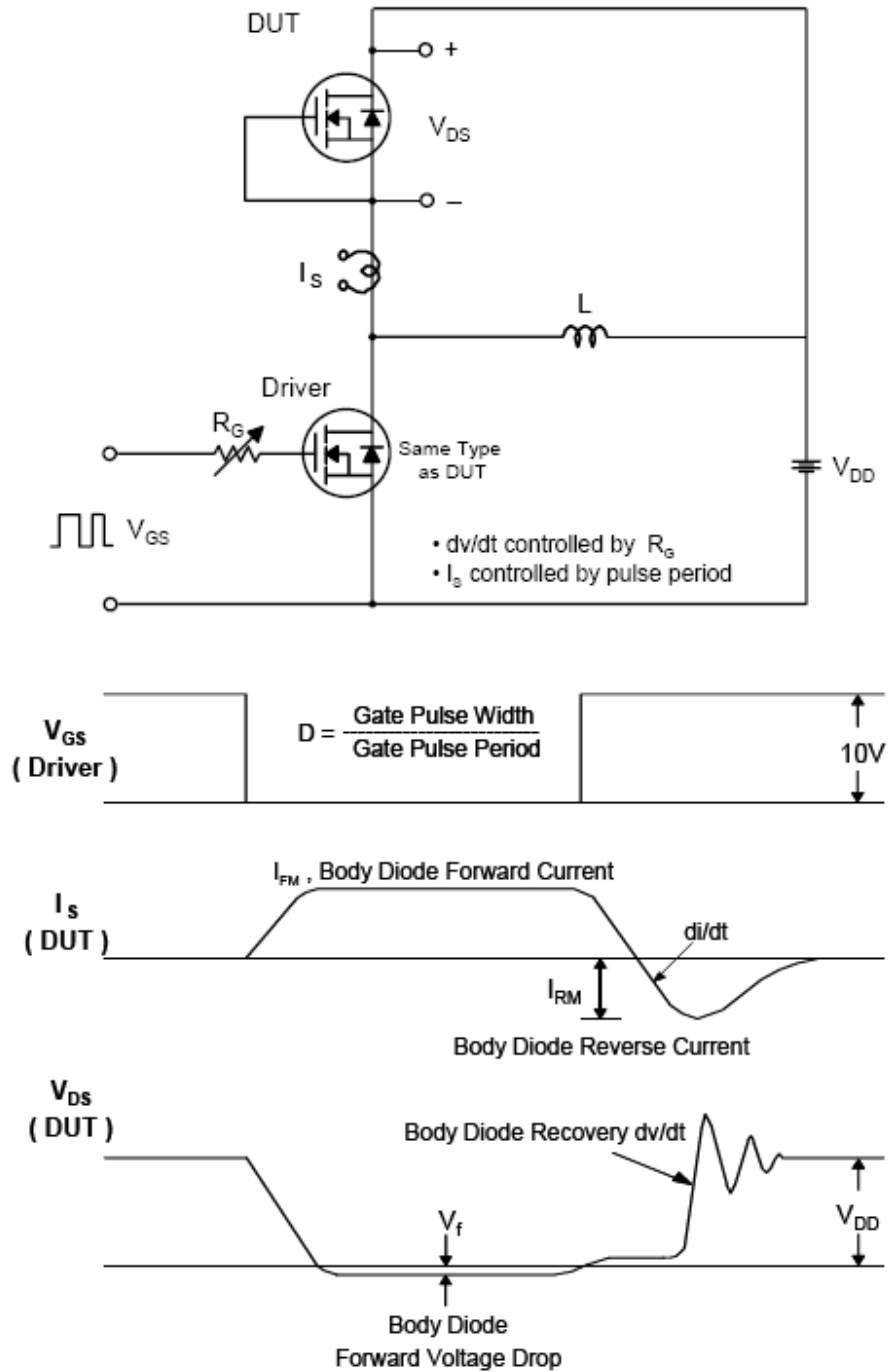
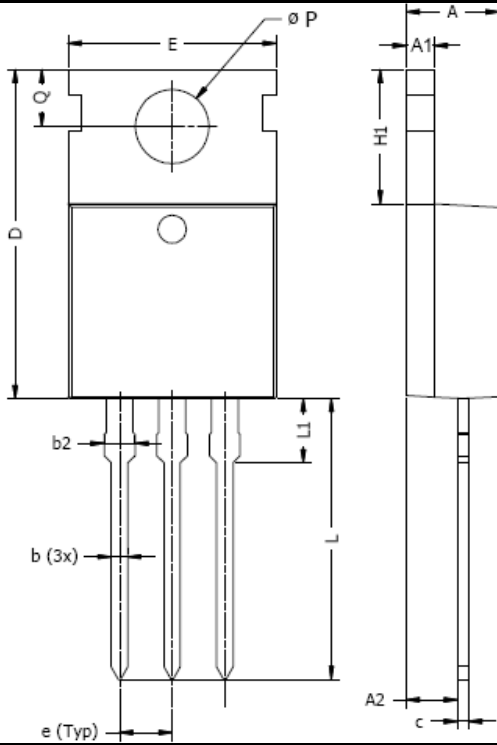
Fig. 12. Gate Charge Test Circuit & Waveforms

Fig 13. Switching Time Test Circuit & Waveforms

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms


Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



TO220AB PACKAGE OUTLINE



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.60	4.80	0.142	0.189
A1	1.20	1.40	0.047	0.055
A2	2.03	2.90	0.080	0.114
b	0.40	1.00	0.016	0.039
b2	1.20	1.78	0.047	0.070
c	0.36	0.60	0.014	0.024
D	14.22	16.50	0.560	0.650
e	2.34	2.74	0.092	0.108
E	9.70	10.60	0.382	0.417
H1	5.84	6.85	0.230	0.270
L	12.70	14.70	0.500	0.579
L1	2.70	3.30	0.106	0.130
ØP	3.50	4.00	0.138	0.157
Q	2.54	3.40	0.100	0.134

NOTE: Above package outline conforms to JEDEC TO-220AB

NOTICE

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