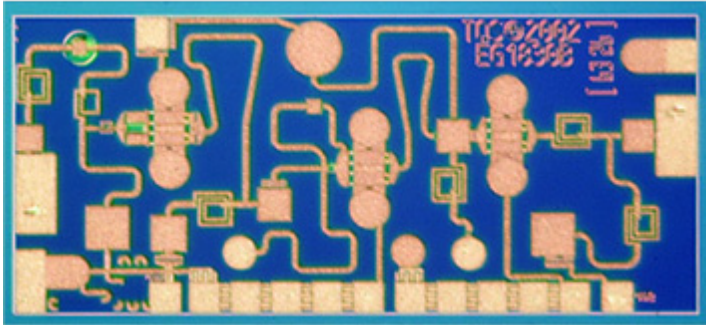


**12-18 GHz Ku-Band 3-Stage Driver Amplifier**

**TGA2507**

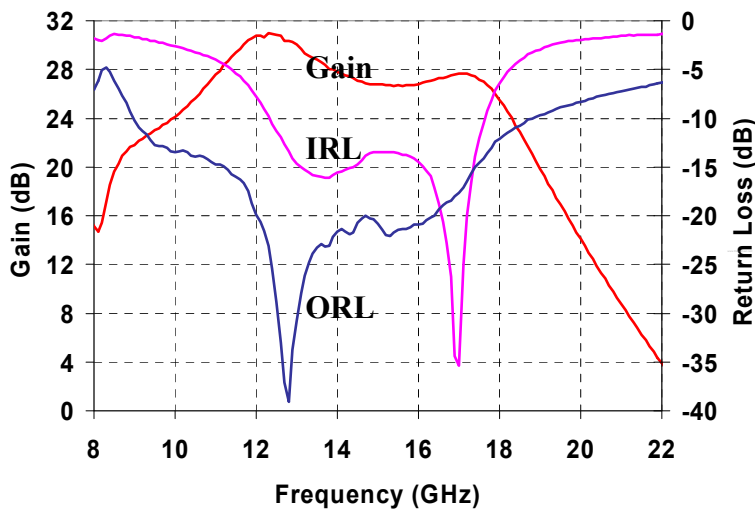


**Key Features**

- 12-18 GHz Bandwidth
- 28 dB Nominal Gain
- 20 dBm P1dB
- Bias: 5,6,7 V, 80 ± 10% mA Self Bias
- 0.5 um 3MI mmW pHEMT Technology
- Chip Dimensions: 1.80 x 0.83 x 0.1 mm (0.071 x 0.031 x 0.004) in

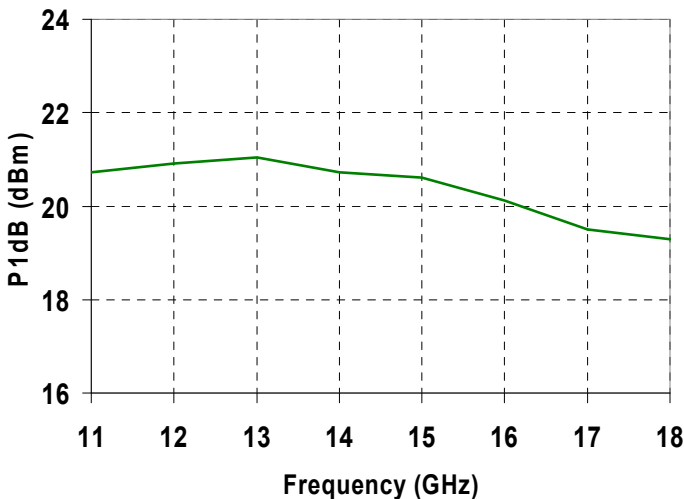
**Preliminary Measured Data**

Bias Conditions:  $V_d = 6\text{ V}$ ,  $I_d = 80\text{ mA}$



**Primary Applications**

- Point to Point Radio
- Military Ku-Band
- Ku-Band Space
- VSAT



Note: Datasheet is subject to change without notice.

**TABLE I  
MAXIMUM RATINGS 1/**

SYMBOL	PARAMETER	VALUE	NOTES
V <sup>+</sup>	Positive Supply Voltage	8 V	<u>2/</u>
I <sup>+</sup>	Positive Supply Current	114 mA	<u>2/</u>
P <sub>IN</sub>	Input Continuous Wave Power	20 dBm	
P <sub>D</sub>	Power Dissipation	0.91 W	<u>2/ 3/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>4/ 5/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 3/ When operated at this power dissipation with a base plate temperature of 70° C, the median life is 1.8 E+6 hrs.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 5/ These ratings apply to each individual FET.

**TABLE II  
DC PROBE TESTS  
(T<sub>A</sub> = 25 °C Nominal)**

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	VALUE
V <sub>BVGS3</sub>	Breakdown Voltage gate-source	-30	-11	V
V <sub>BVGD3</sub>	Breakdown Voltage gate-drain	-30	-11	V
V <sub>P2</sub>	Pinch-off Voltage	-1.5	-0.3	V
V <sub>P3</sub>	Pinch-off Voltage	-1.5	-0.3	V

**TABLE III**  
**ELECTRICAL CHARACTERISTICS**  
(Ta = 25 °C, Nominal)

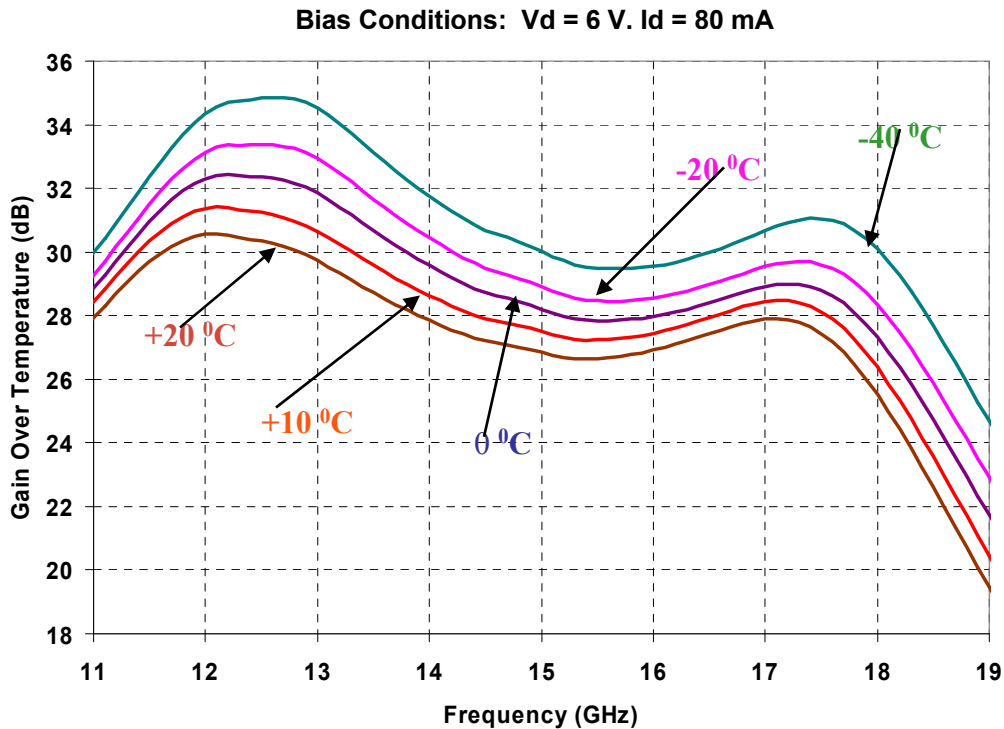
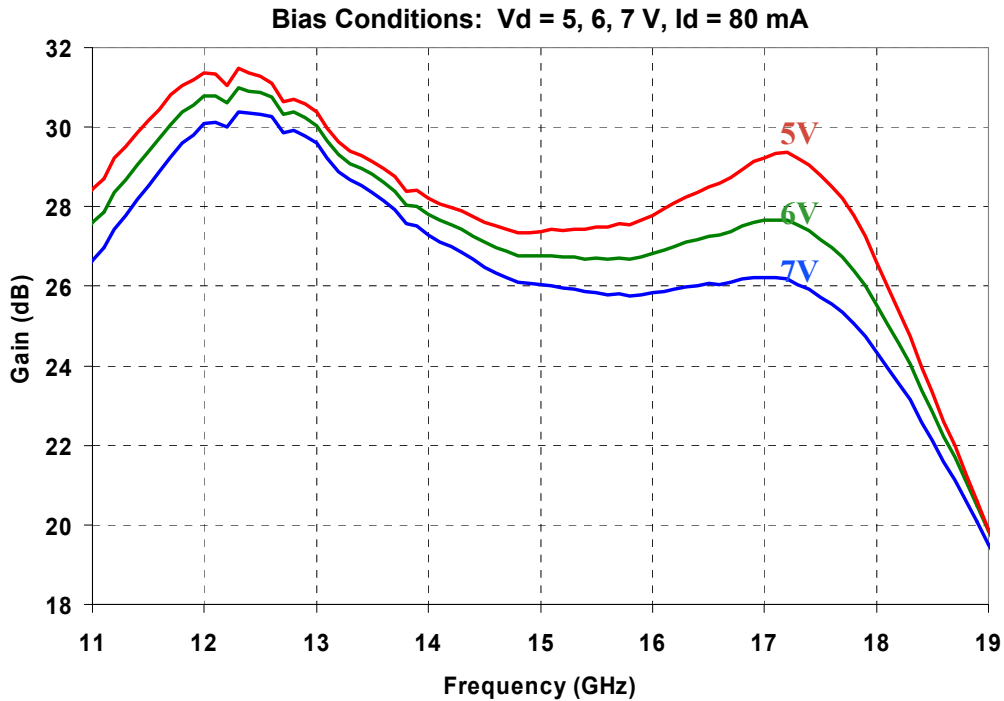
PARAMETER	TYPICAL	UNITS
Drain Operating	6	V
Quiescent Current	80 ± 10% Self Bias	mA
Small Signal Gain	28	dB
Input Return Loss	15	dB
Output Return Loss	20	dB
Output Power @ 1 dB Compression Gain	20	dBm

**TABLE IV**  
**THERMAL INFORMATION**

Parameter	Test Conditions	T <sub>CH</sub> (°C)	R <sub>θJC</sub> (°C/W)	T <sub>M</sub> (HRS)
R <sub>θJC</sub> Thermal Resistance (channel to backside of carrier)	Vd = 6 V Id = 80 mA Pdiss = 0.48 W	108	80	5.2 E+7

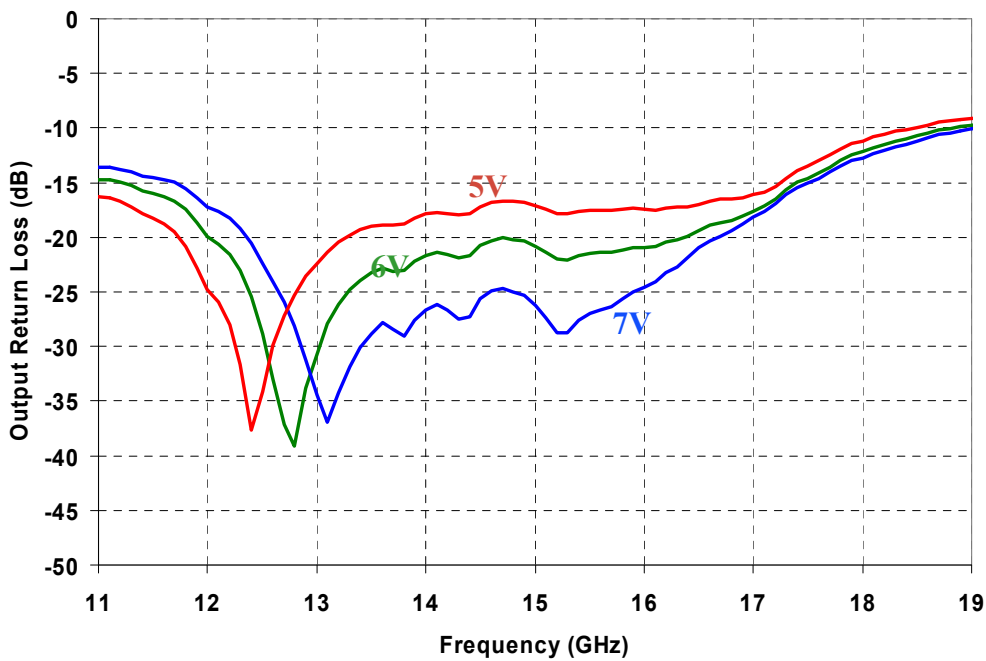
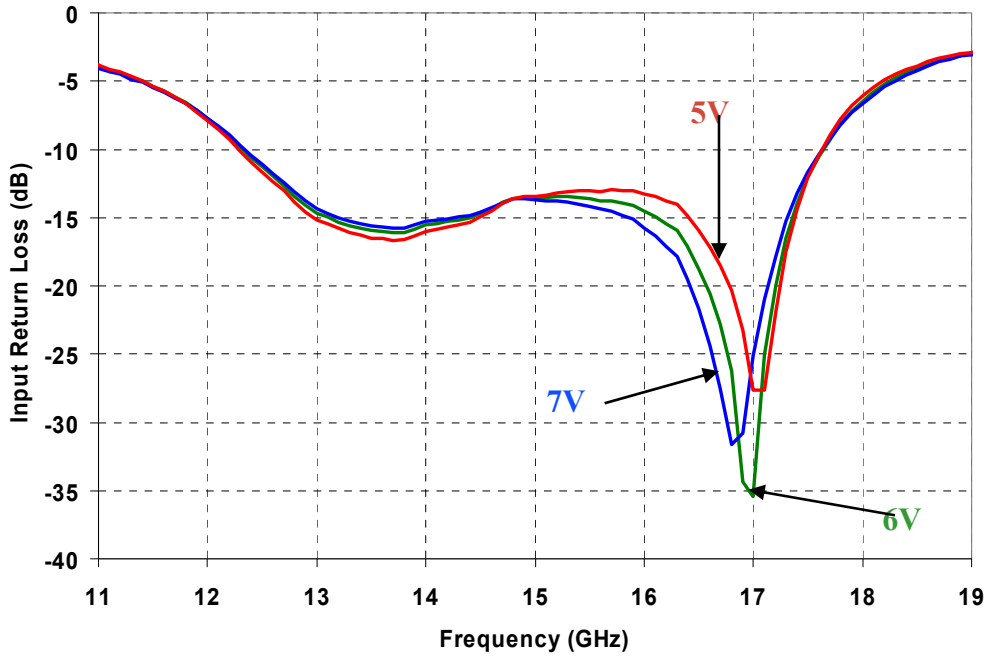
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

## Preliminary Measured Data

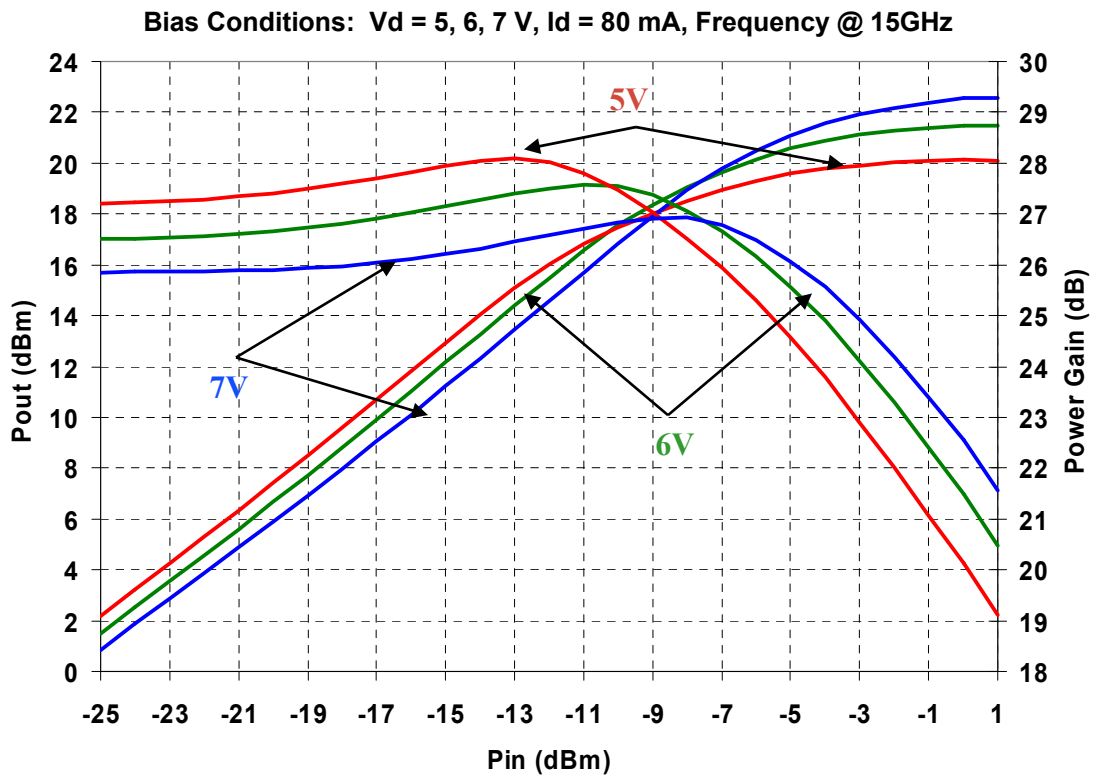
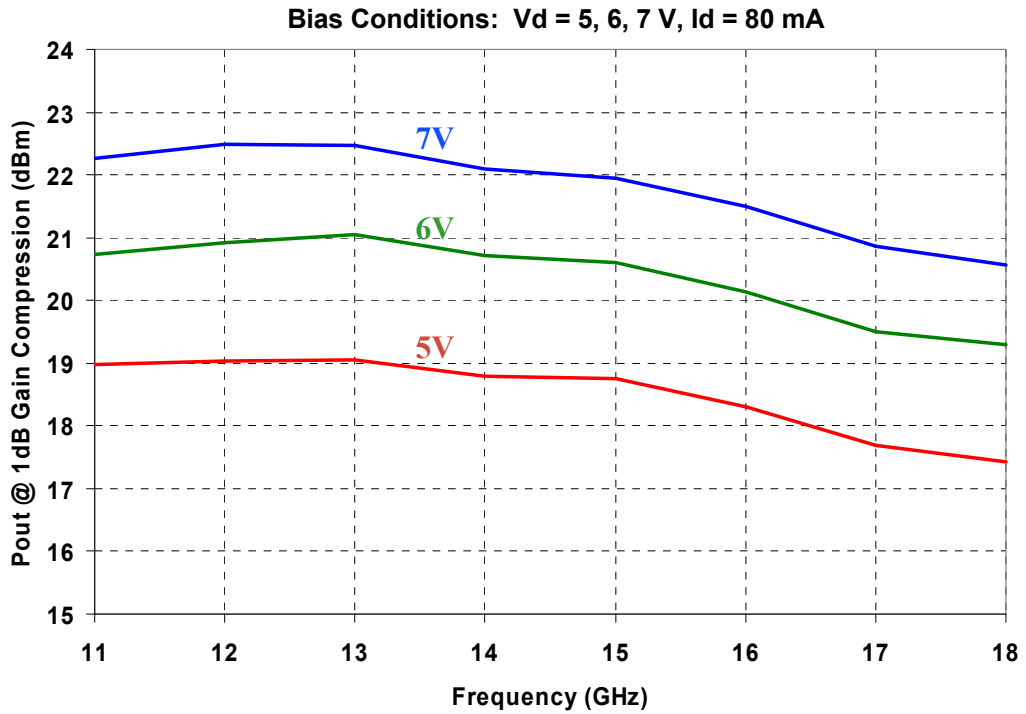


### Preliminary Measured Data

Bias Conditions:  $V_d = 5, 6, 7 \text{ V}$ ,  $I_d = 80 \text{ mA}$

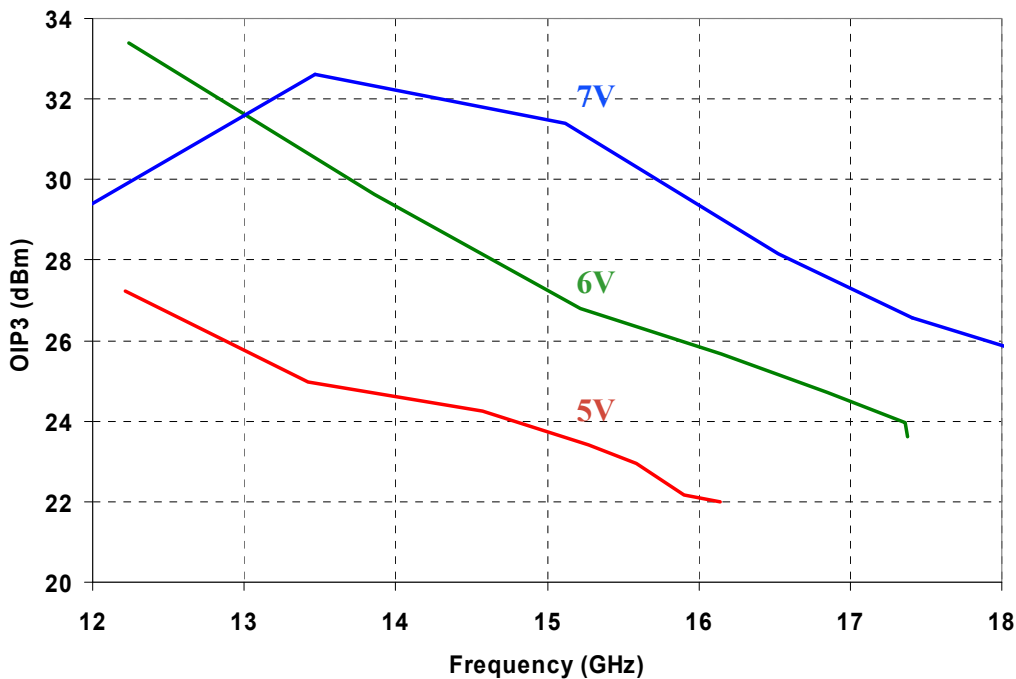


**Preliminary Measured Data**

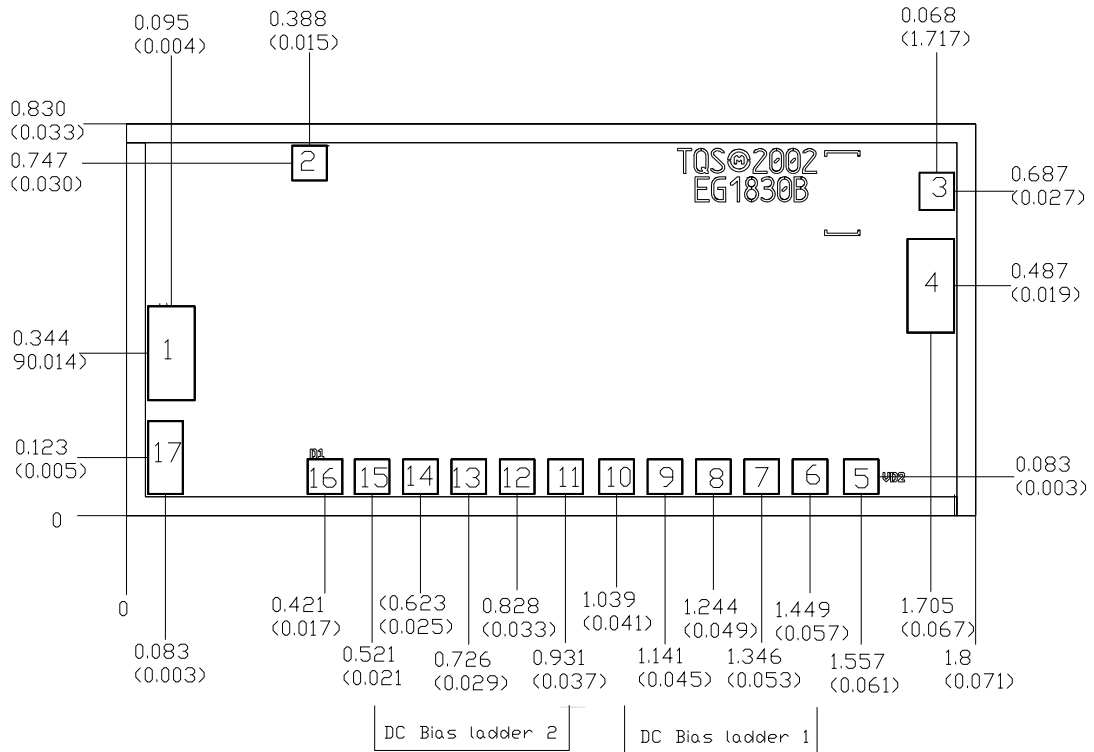


### Preliminary Measured Data

Bias Conditions:  $V_d = 5, 6, 7 \text{ V}$ ,  $I_d = 80 \text{ mA}$



**Mechanical Drawing**



Units: millimeters (inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

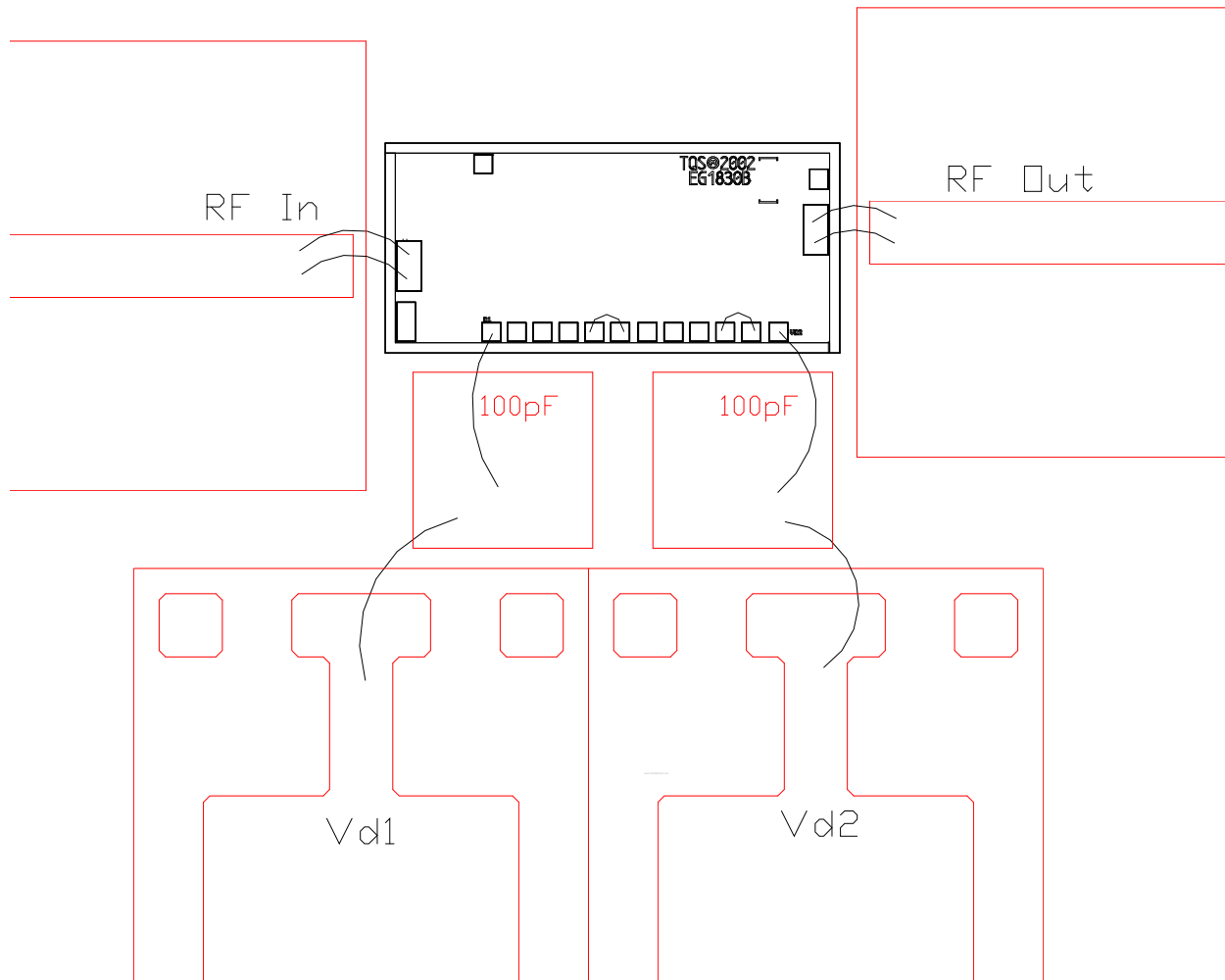
GND is back side of MMIC

Bond pad #1	(RF In)	0.100 x 0.200	(0.004 x 0.008)
Bond pad #2	(N/C)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #3	(N/C)	0.075 x 0.081	(0.003 x 0.003)
Bond pad #4	(RF Out)	0.100 x 0.200	(0.004 x 0.008)
Bond pad #5	(Vd2)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #6 thru #10	(DC Bias ladder 1)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #11 thru #15	(DC Bias ladder 2)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #16	(Vd1)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #17	(N/C)	0.075 x 0.155	(0.003 x 0.006)

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**



**Chip Assembly Diagram**



This configuration is for a self-bias logic pad current search with connections for bin #1. See Table IV for alternate bin # to get the current of typical  $80 \pm 10\%$  mA.

**TABLE V**  
**PAD CONNECTIONS**

<b>BIN No.</b>	<b>DC BIAS LADDER 1</b>	<b>DC BIAS LADDER 2</b>
1	Pad 6 to Pad 7	Pad 11 to Pad 12
2	Pad 6 to Pad 8	Pad 11 to Pad 13
3	Pad 6 to Pad 9	Pad 11 to Pad 14
4	Pad 6 to Pad 10	Pad 11 to Pad 15

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200°C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***