

4 - 14 GHz balanced LNA

TGA2512-SM



Self Bias



Gate Bias

Key Features

- Typical Frequency Range: 4 - 14 GHz
- 2.3 dB Nominal Noise Figure
- 25 dB Nominal Gain
- 15 dB AGC Range
- 13 dBm Nominal P1dB
- 24dBm Nominal OIP3
- Bias: 5 V, 160 mA Gate Bias
5 V, 90 mA Self Bias
- Package Dimensions:
4.0 x 4.0 x 0.9 mm

Primary Applications

- X-Band Radar
- EW, ECM
- Point-to-Point Radio

Product Description

The TriQuint TGA2512-SM is a packaged X-band balanced LNA with AGC amplifier for EW, ECM, and RADAR receiver or driver amplifier applications. The TGA2512-SM provides excellent noise performance with typical midband NF of 2.3dB, and high gain, 25dB from 4-14GHz

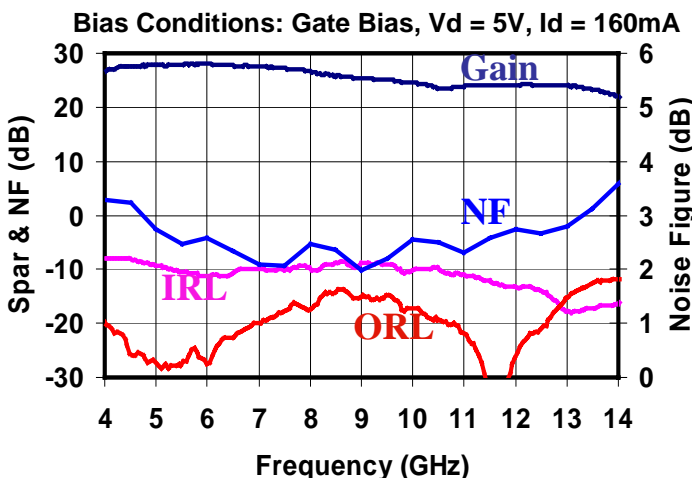
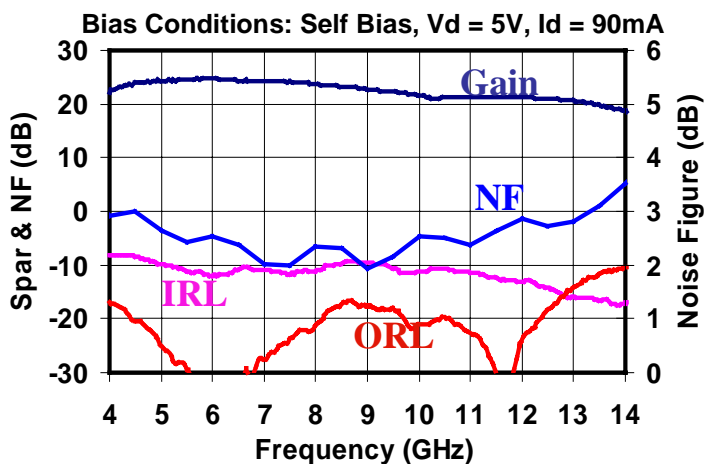
The TGA2512-SM is designed for maximum ease of use. TGA2512-SM can handle up to 21dBm input power reliably, while the build-in gain control provides 15dB of typical gain control range. The part can be used in self-biased mode, with a single +5V supply connection, or in gate biased mode, allowing the user to control the current for a particular application.

In self-biased mode the TGA2512-SM achieves 6dBm typical P1dB, while in gate-biased mode the typical P1dB is over 13dBm.

Lead-Free & RoHS compliant.

Evaluation boards are available.

Measured Data



Note: Device is early in the characterization process prior to finalizing all electrical specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V _d	Drain Voltage	[3.5 + (0.0125)(I _d)] V	2/ 3/
V _g	Gate Voltage Range	-1 TO +0.5 V	
I _d	Drain Current (gate biased)	240 mA	2/
I _g	Gate Current	7.04 mA	
P _{IN}	Input Continuous Wave Power	21 dBm	
P _D	Power Dissipation	See note 4/	2/
T _{CH}	Operating Channel Temperature	117 °C	5/
T _M	Mounting Temperature (30 Seconds)	260 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	
T _{CASE}	Package Operating Temperature	-40 to 110 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Unit for I_d is A

4/ For a median life time of 1E+6 hrs, Power dissipation is limited to:

$$P_D(\text{max}) = (117 \text{ }^\circ\text{C} - T_{\text{BASE}} \text{ }^\circ\text{C}) / \theta_{\text{JC}} \text{ (}^\circ\text{C/W)}$$

Where T_{BASE} is the base plate temperature.

$$\theta_{\text{JC}} \text{ for self bias is } 28.2 \text{ }^\circ\text{C/W}$$

$$\theta_{\text{JC}} \text{ for gate bias is } 37.6 \text{ }^\circ\text{C/W}$$

5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
ELECTRICAL CHARACTERISTICS

(Ta = 25 °C, Nominal)

PARAMETER	Gate Bias	Self Bias	UNITS
Frequency Range	4 - 14	4 - 14	GHz
Drain Voltage, Vd	5.0	5.0	V
Drain Current, Id	160	90	mA
Gate Voltage, Vg	-0.1	-	V
Small Signal Gain, S21	25	22	dB
Input Return Loss, S11	10	10	dB
Output Return Loss, S22	20	20	dB
Noise Figure, NF	2.3	2.3	dB
Output Power @ 1dB Gain Compression, P1dB	13	6	dBm
OIP3	24	16	dBm
Temperature Gain Coefficient	-0.02	-0.02	dB/°C

Note: Table II Lists the RF Characteristics of typical devices as determined by fixtured measurements.

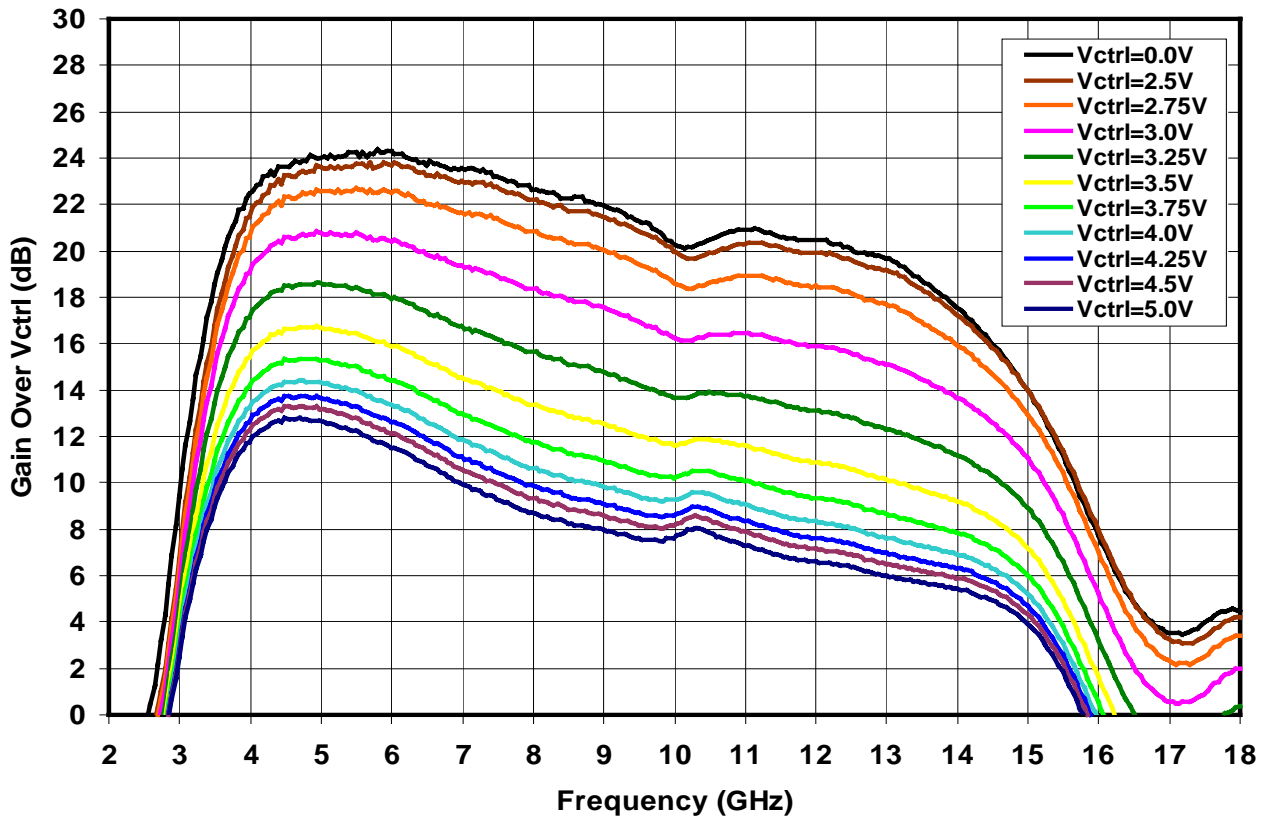
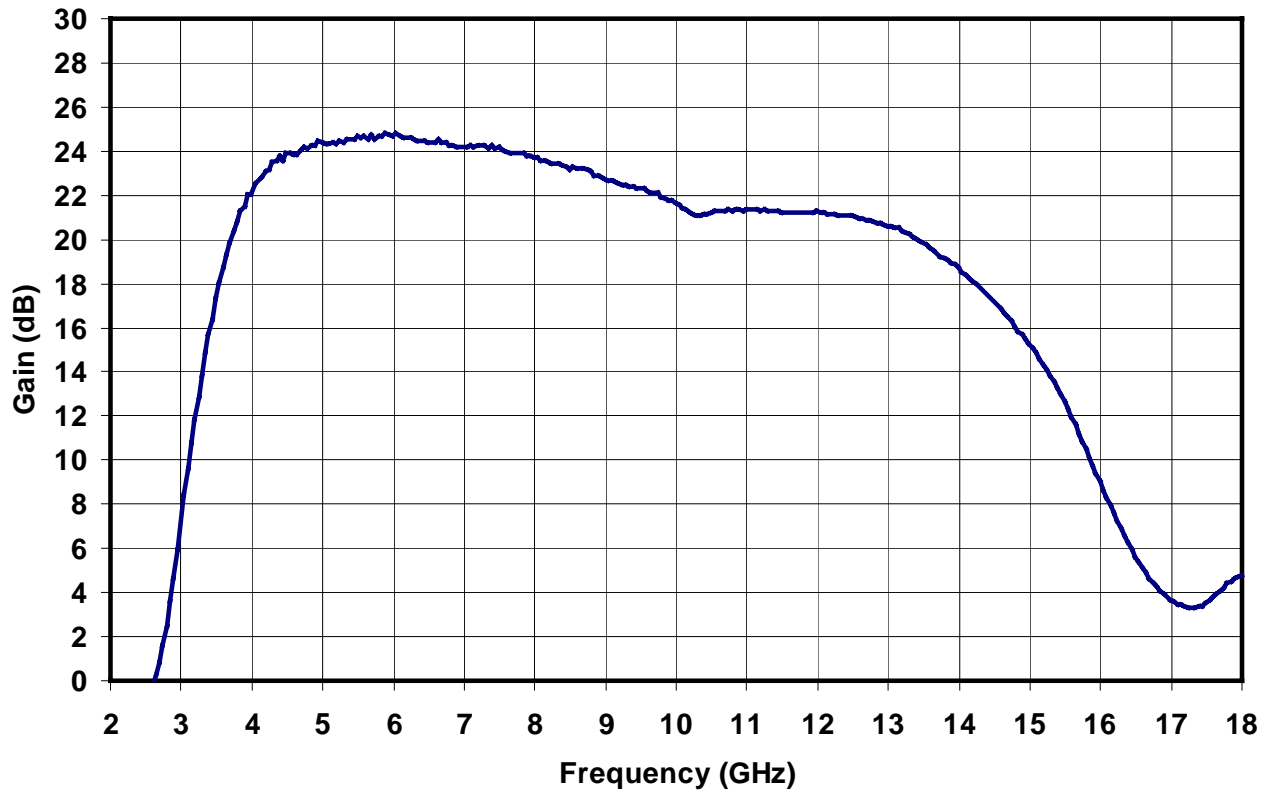
TABLE III
THERMAL INFORMATION

PARAMETER	TEST CONDITIONS	T _{CH} (°C)	θ _{JC} (°C/W)	T _M (HRS)
θ _{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 160 mA Gate Bias P _{diss} = 0.80 W	100	37.6	5.8E+6
θ _{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 90 mA Self Bias P _{diss} = 0.45 W	82.7	28.2	4.1E+7

Note: Worst case condition with no RF applied, 100% of DC power is dissipated, Case Temperature @ 70 °C

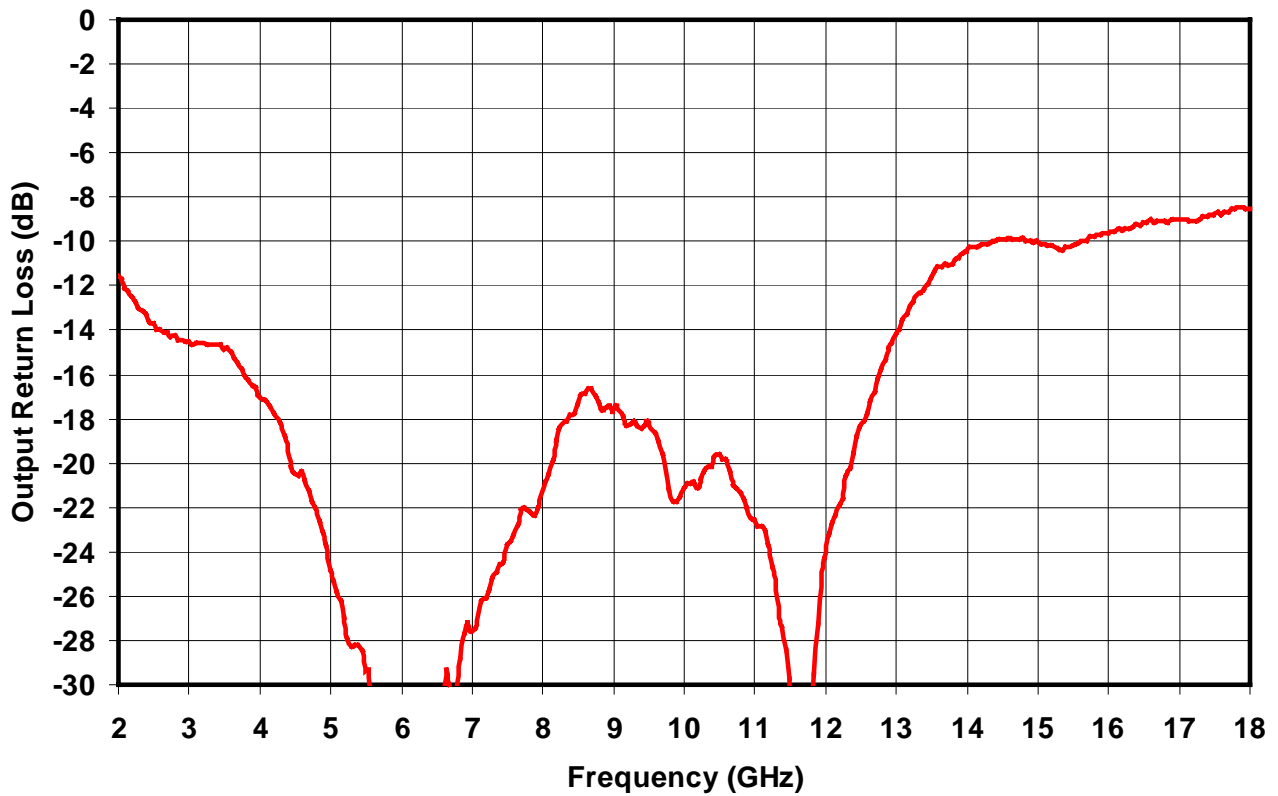
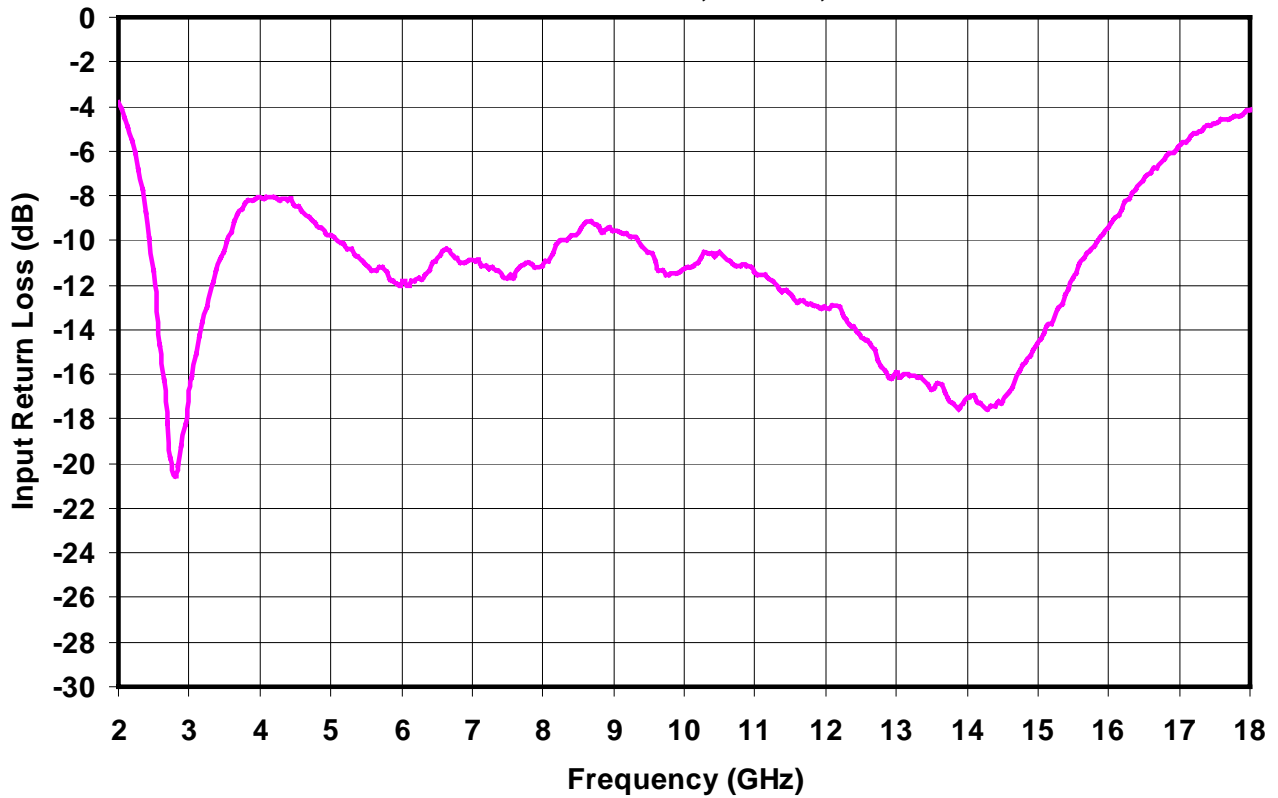
Measured Data

Bias Conditions: **Self Bias**, $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$



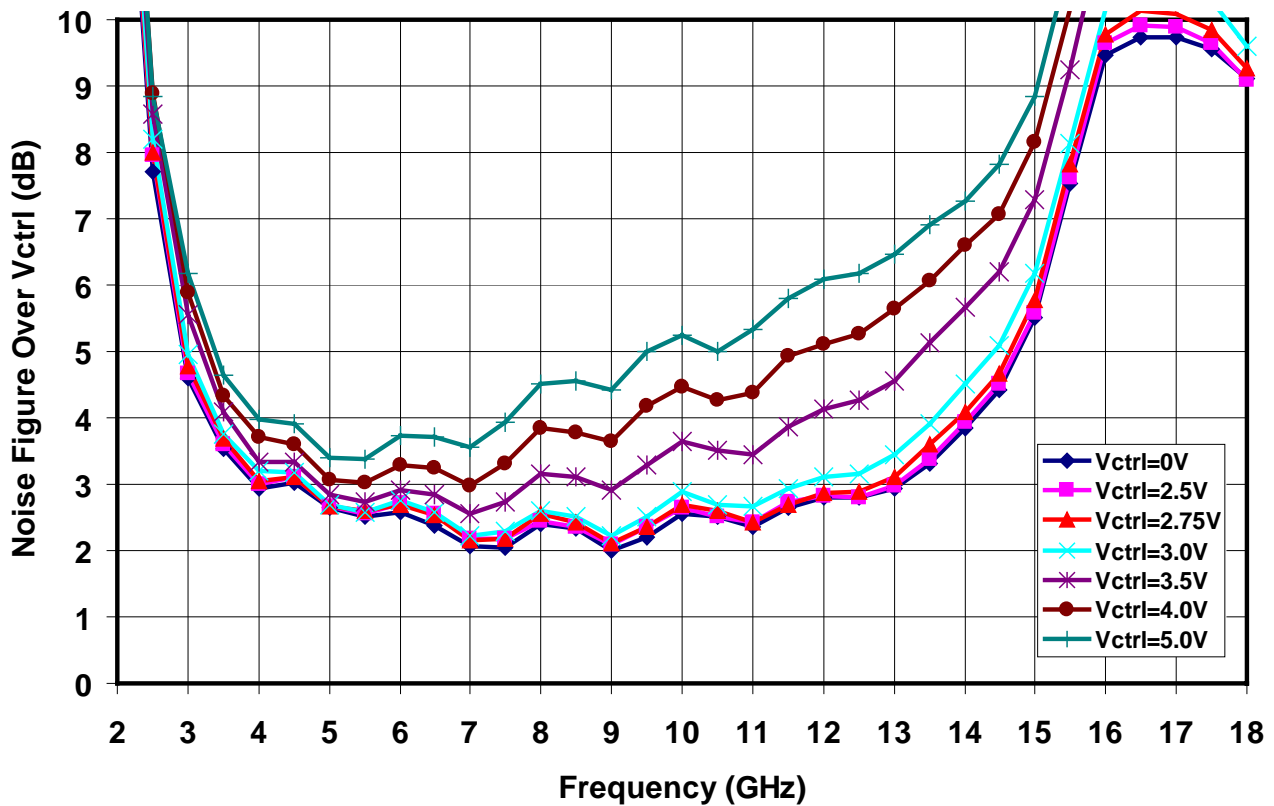
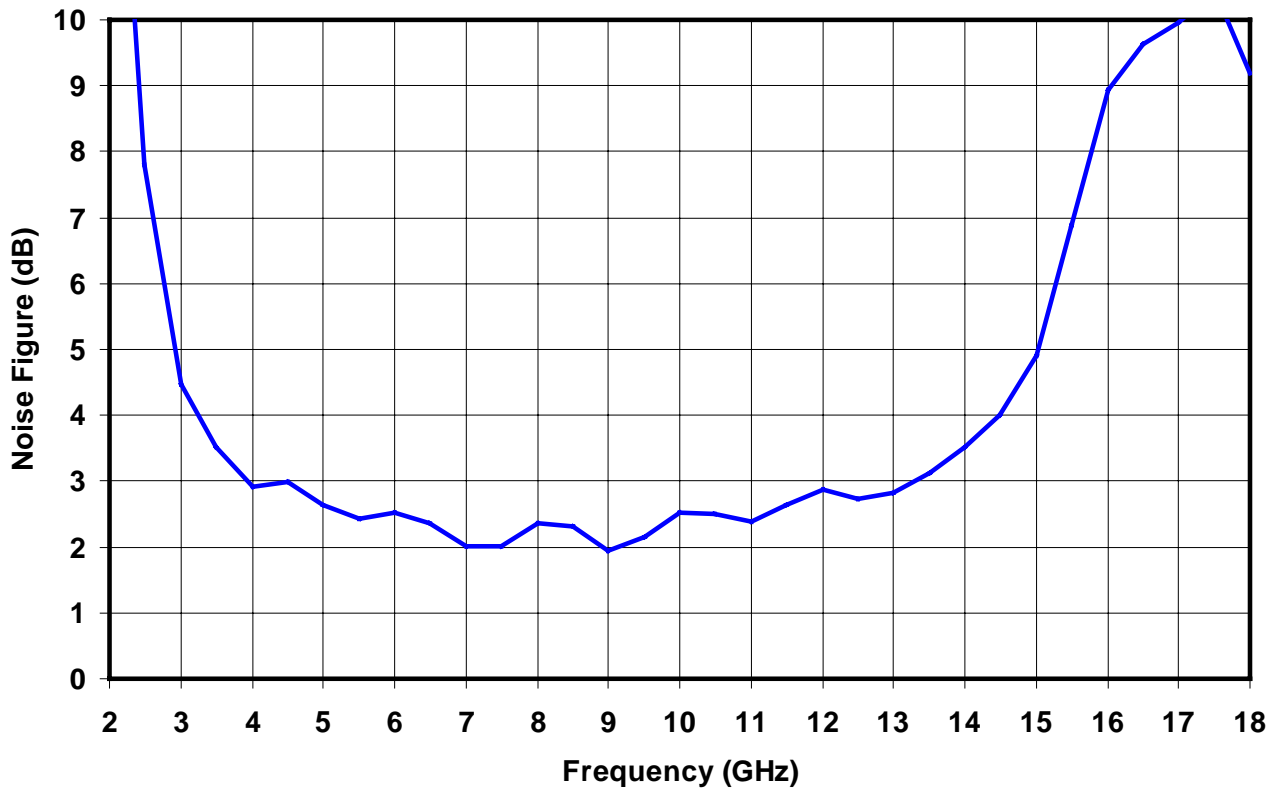
Measured Data

Bias Conditions: **Self Bias**, $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$



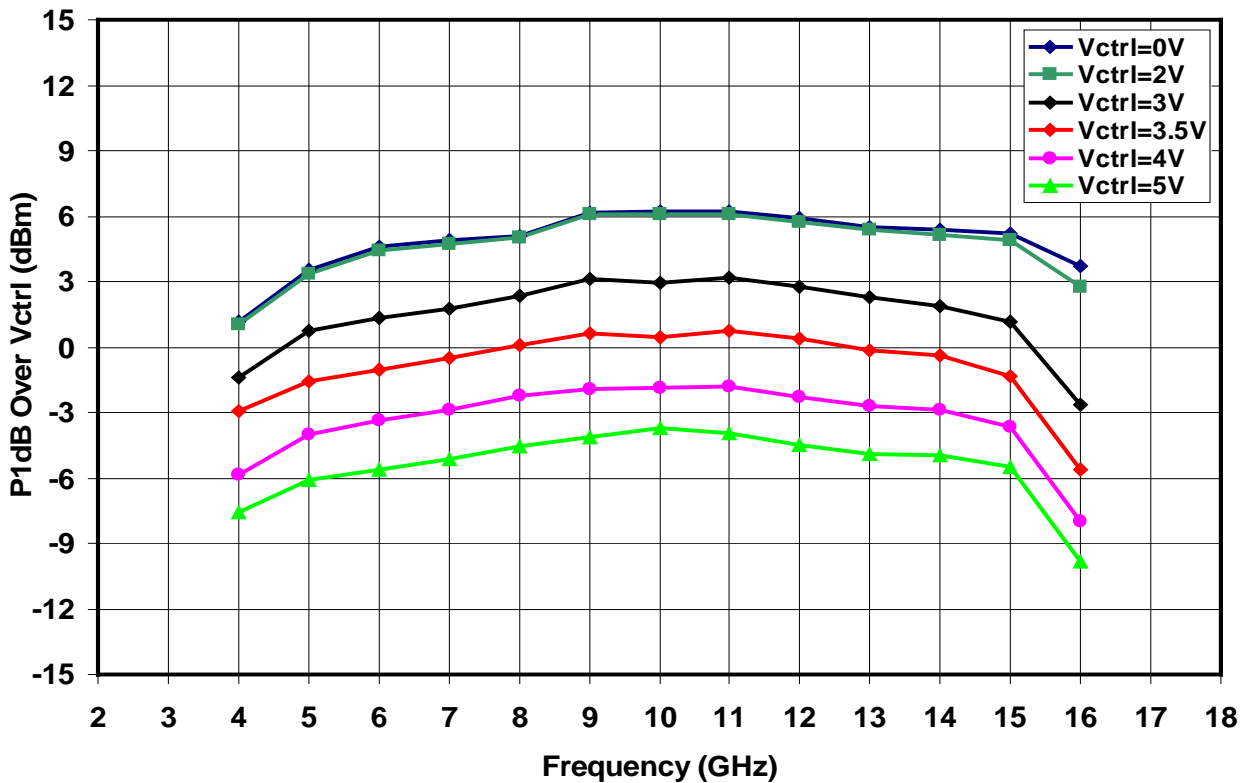
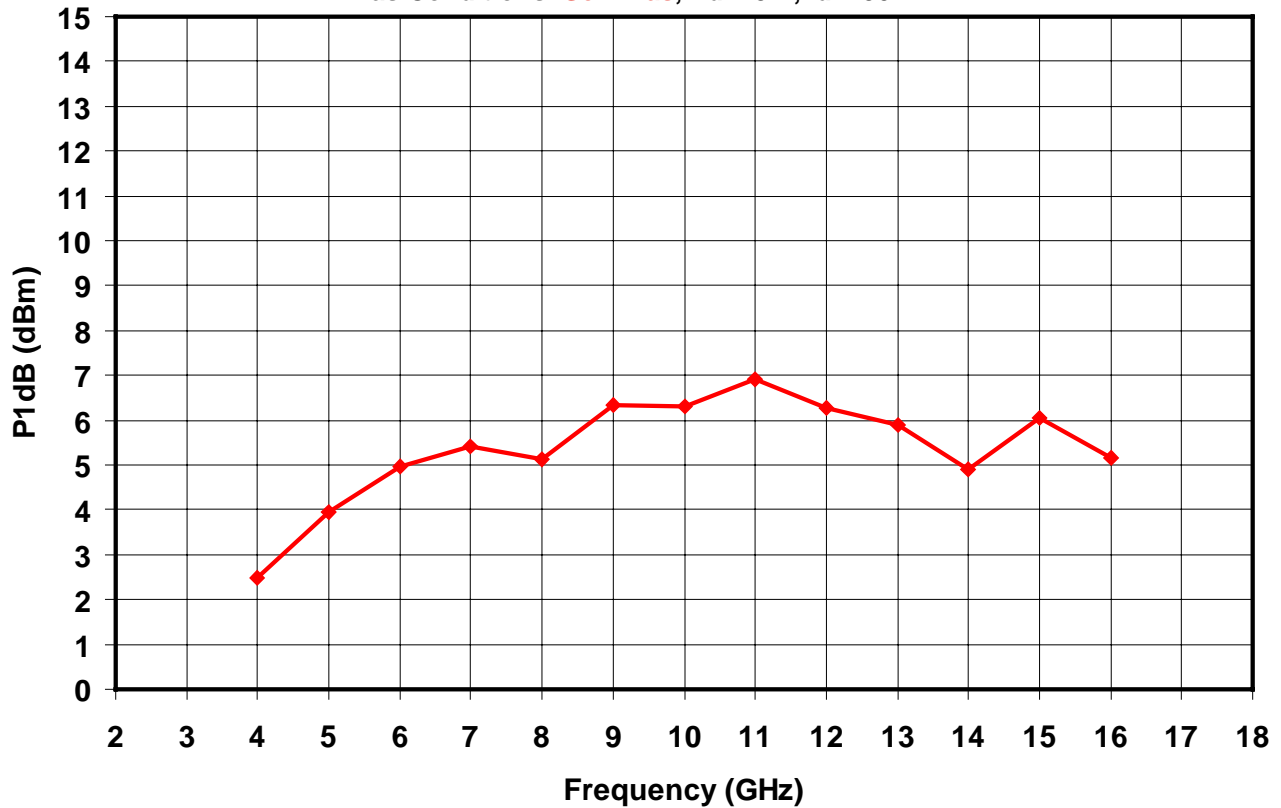
Measured Data

Bias Conditions: **Self Bias**, $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$



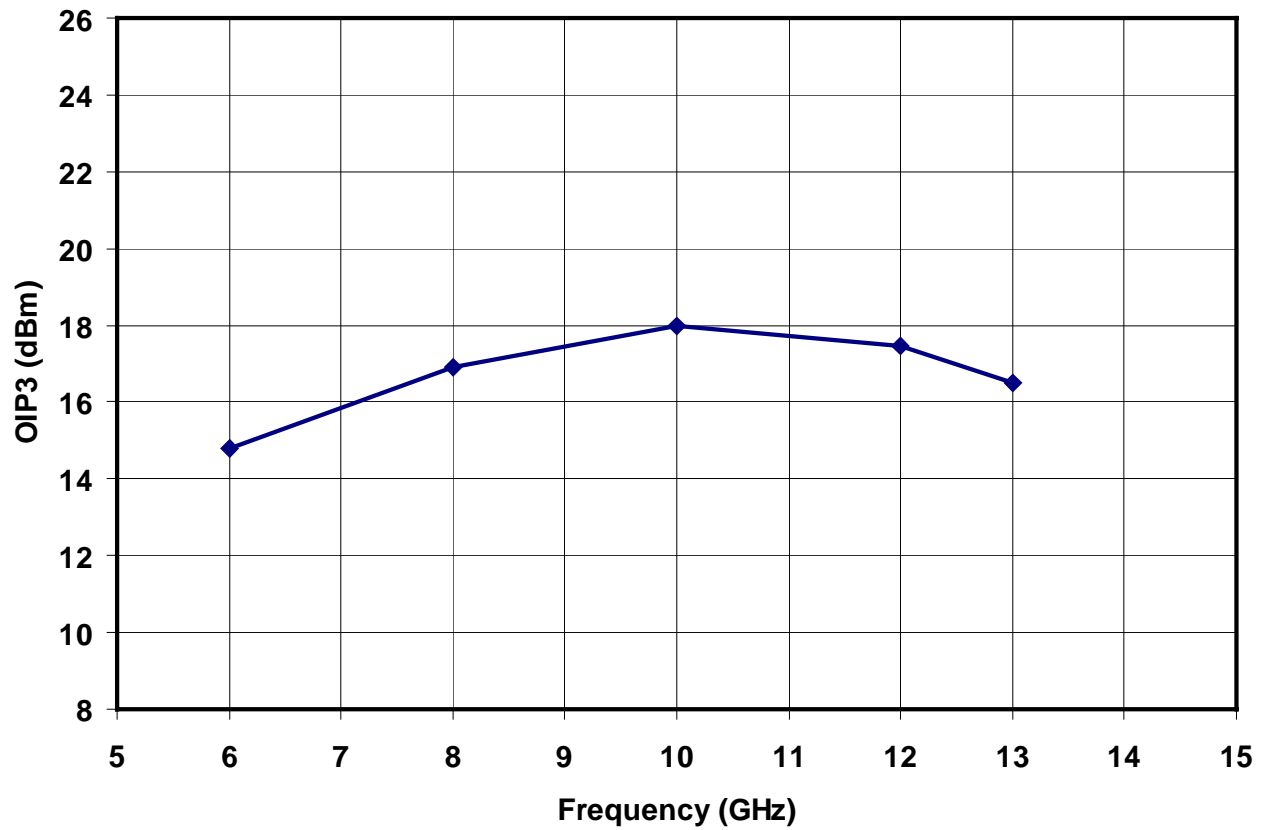
Measured Data

Bias Conditions: **Self Bias**, $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$



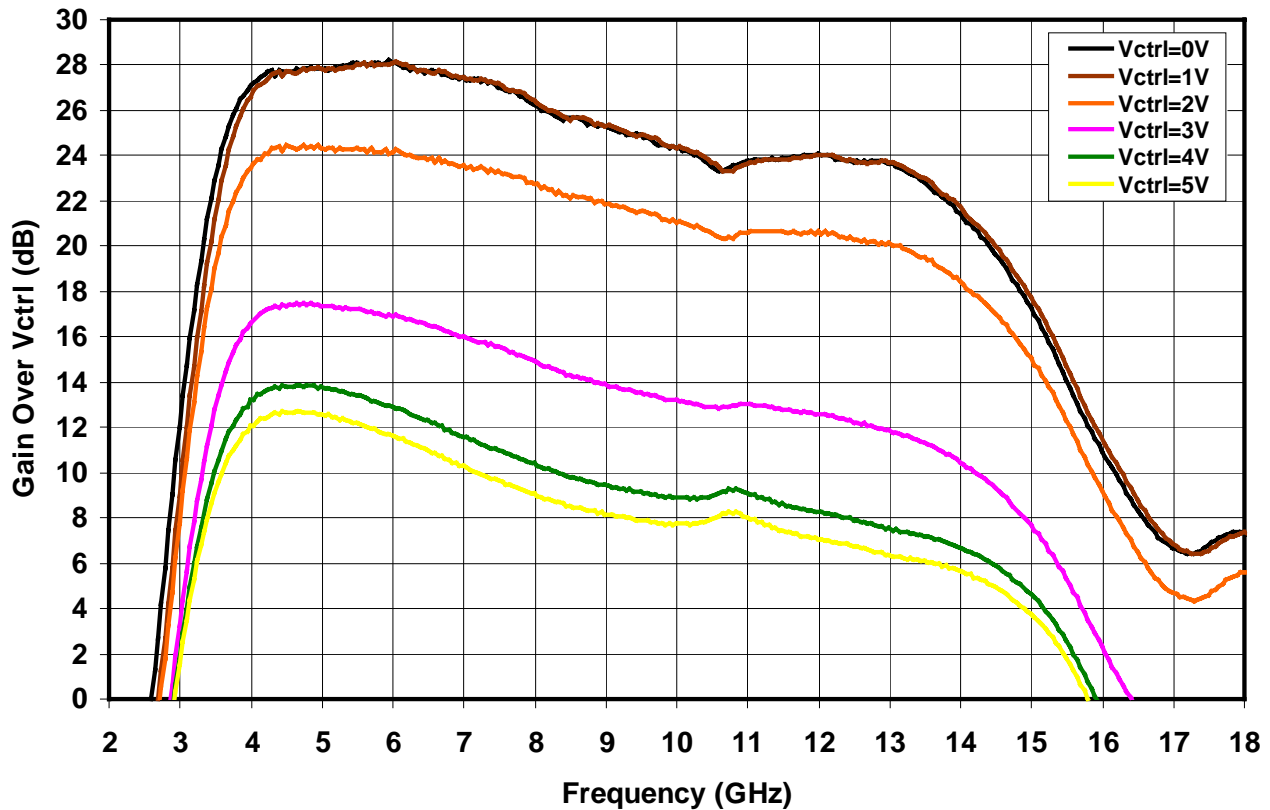
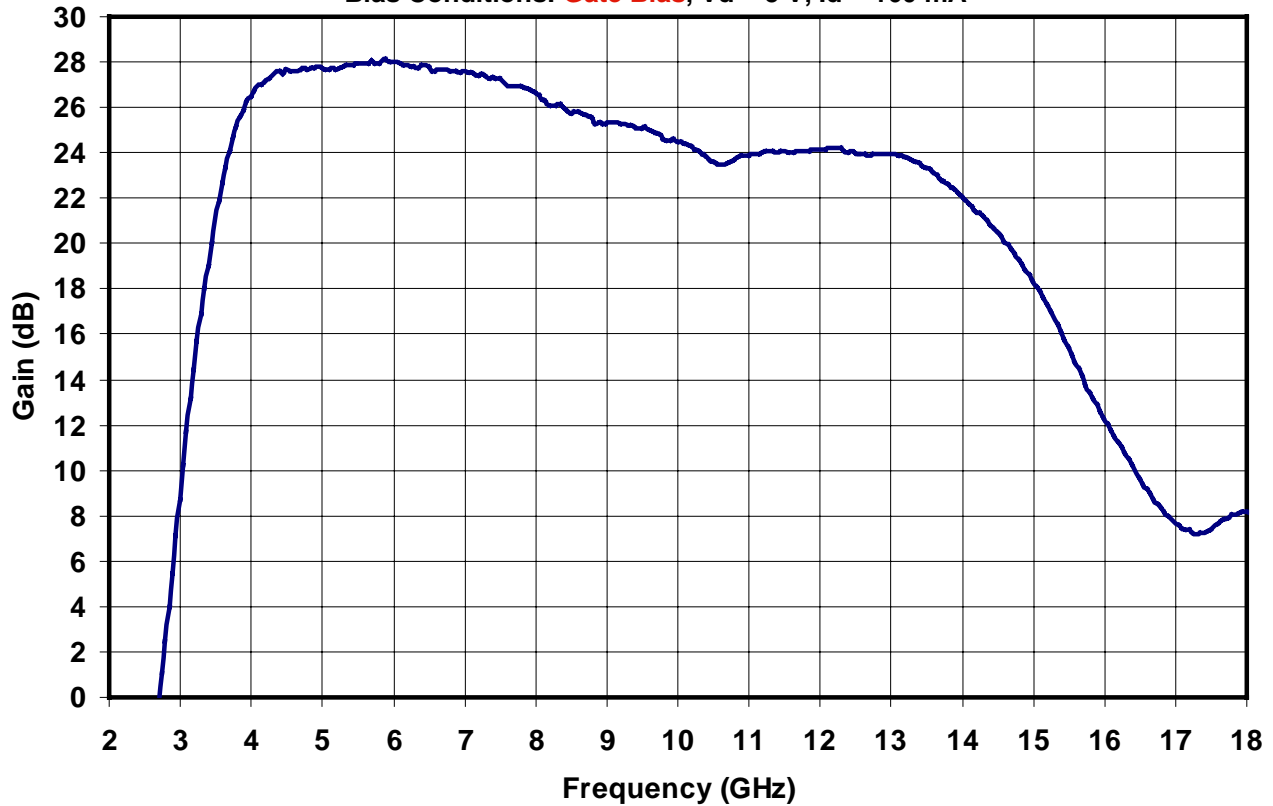
Measured Data

Bias Conditions: **Self Bias**, $V_d = 5\text{ V}$, $I_d = 90\text{ mA}$



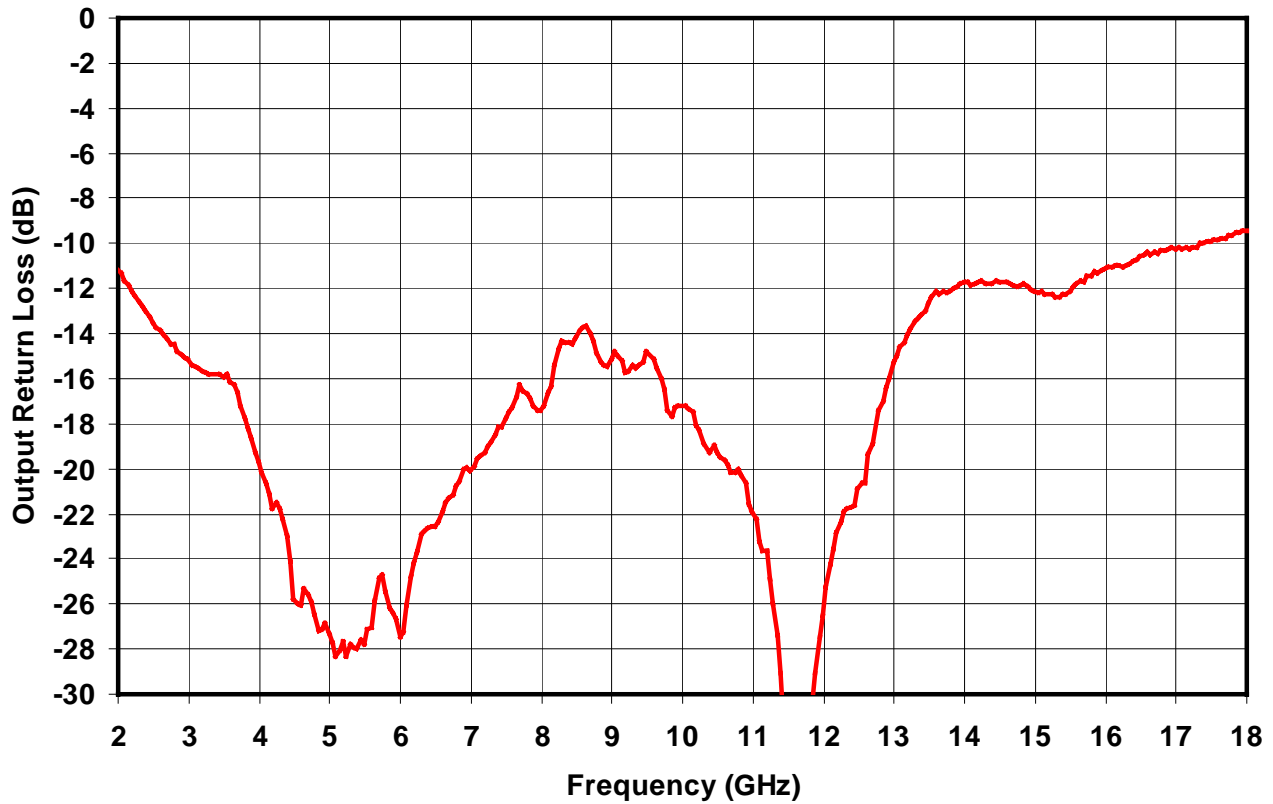
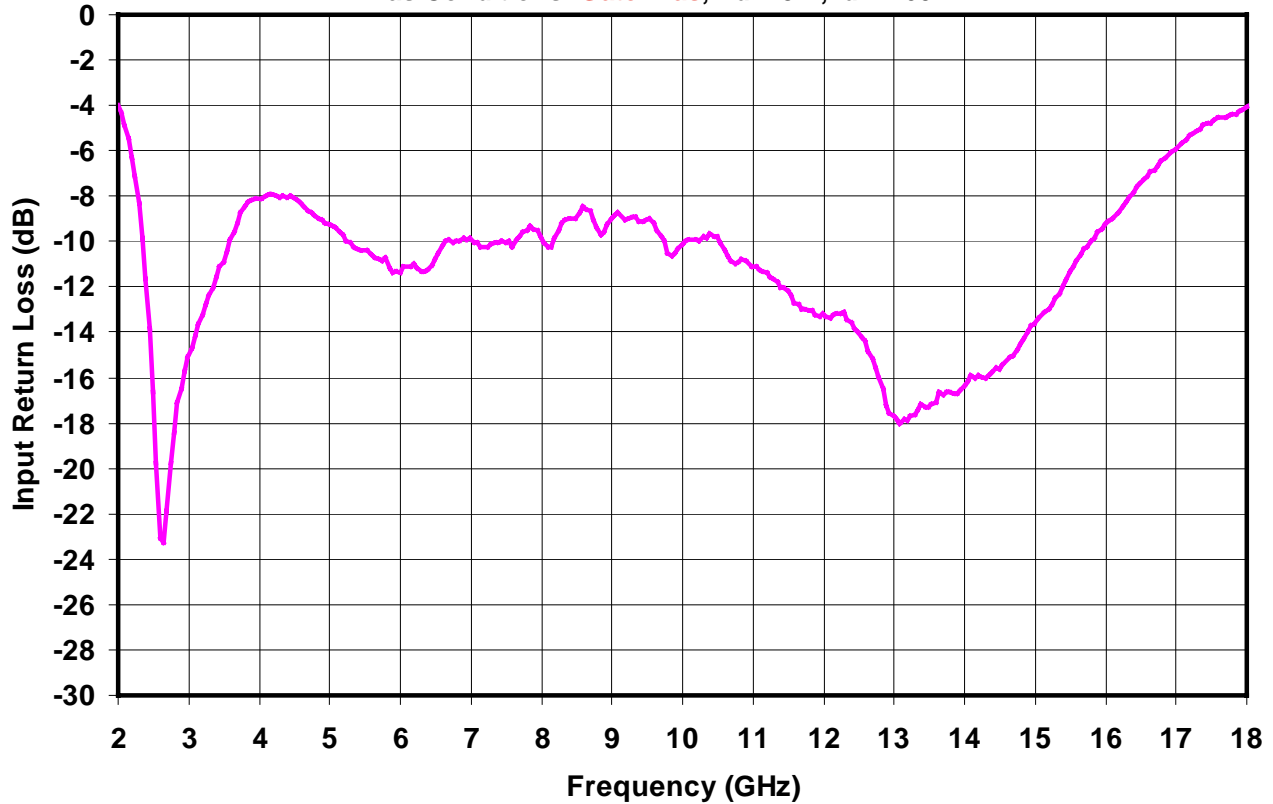
Measured Data

Bias Conditions: **Gate Bias**, $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$



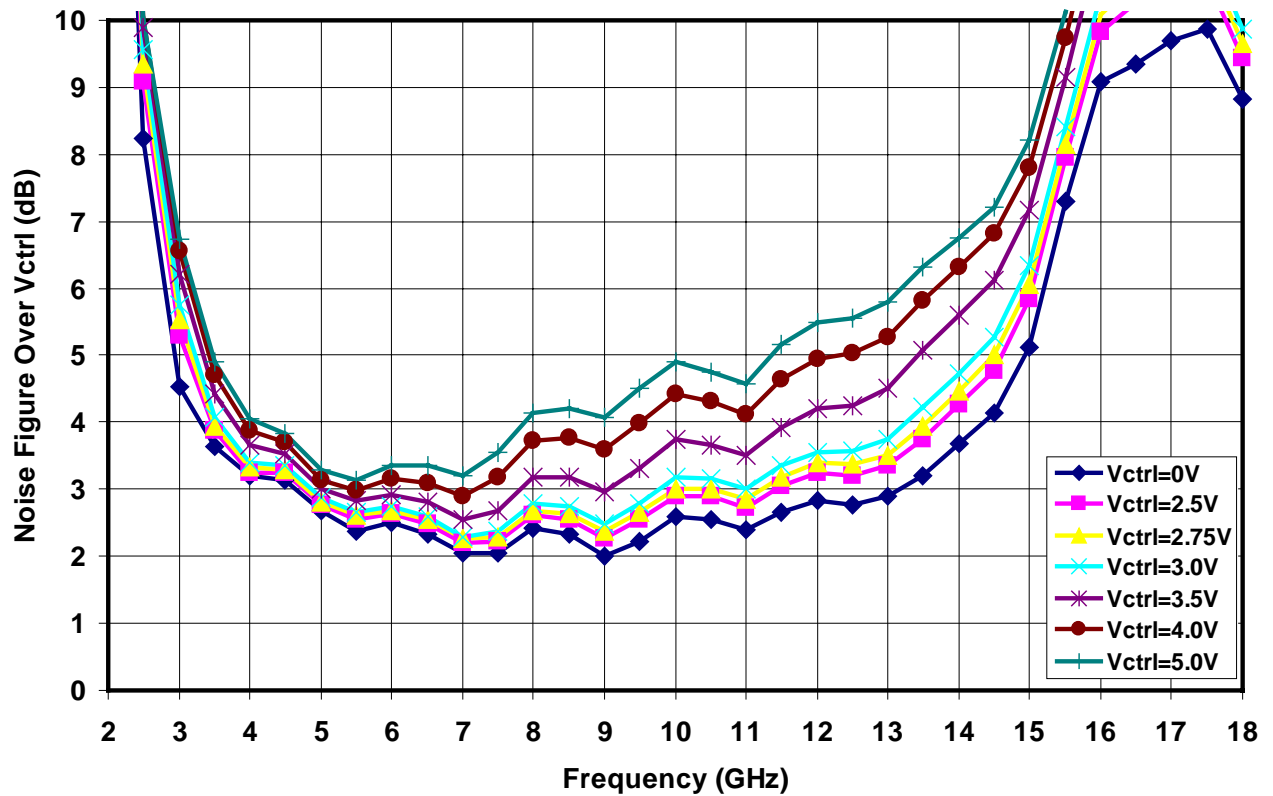
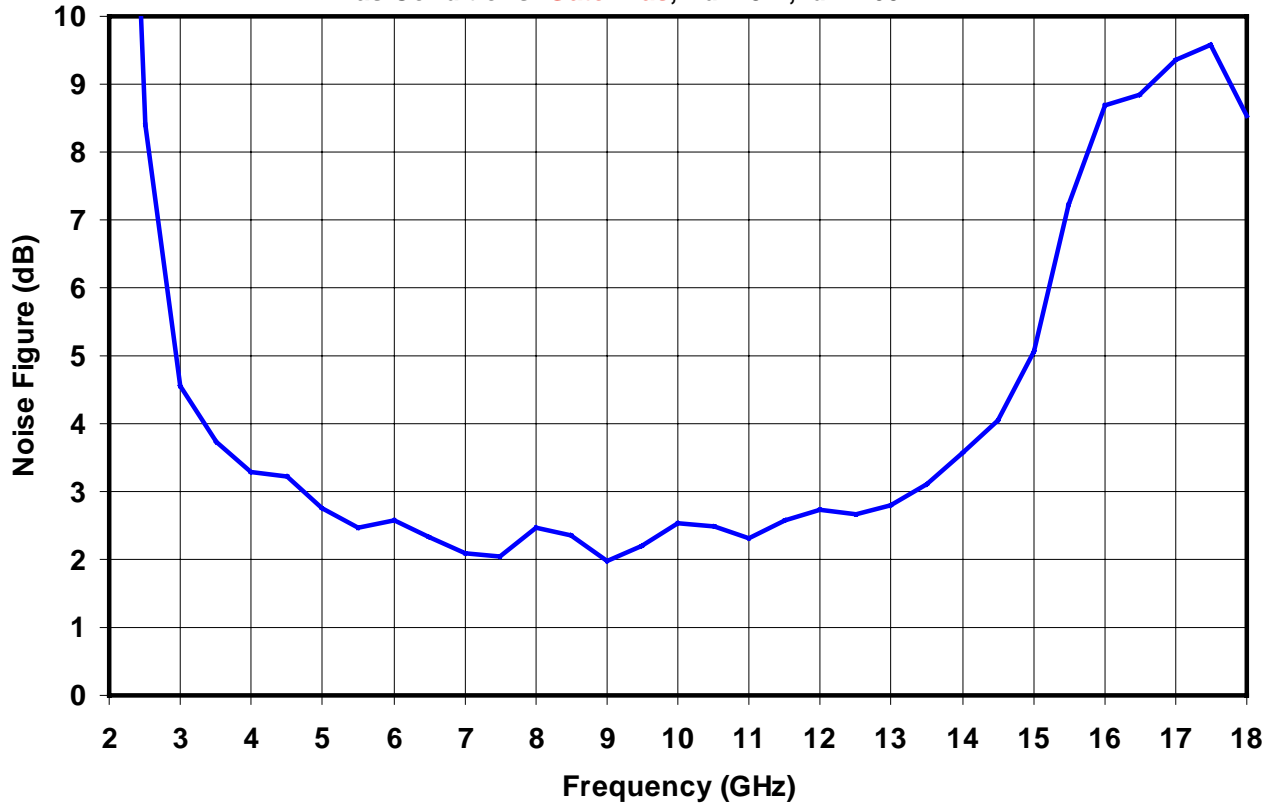
Measured Data

Bias Conditions: **Gate Bias**, $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$



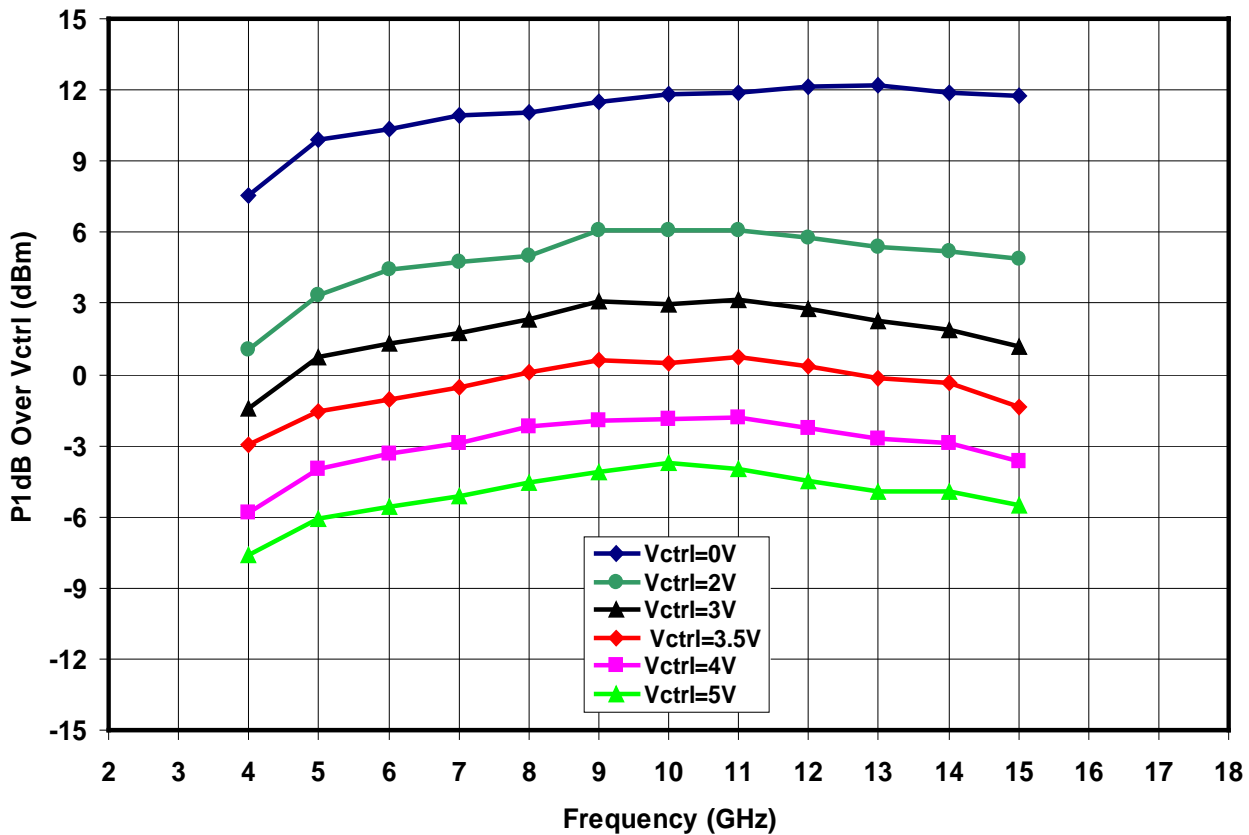
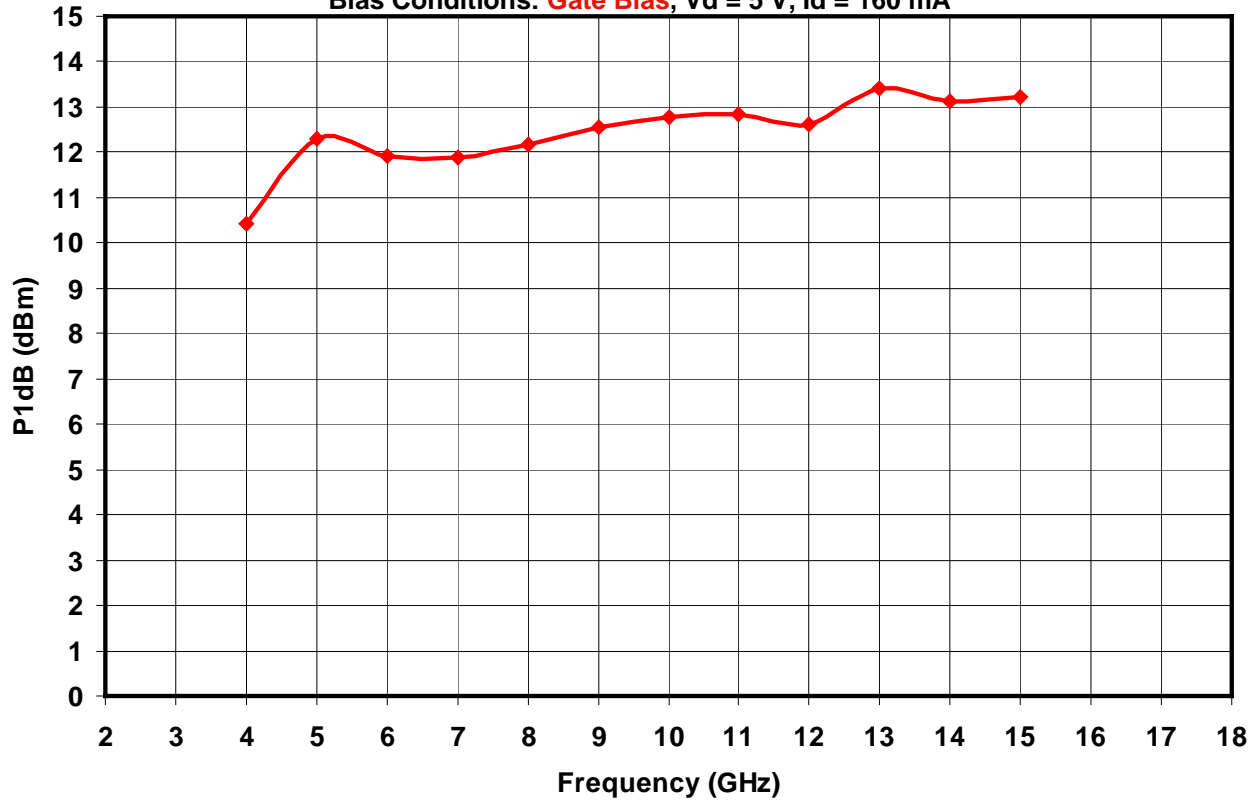
Measured Data

Bias Conditions: Gate Bias, Vd = 5 V, Id = 160 mA



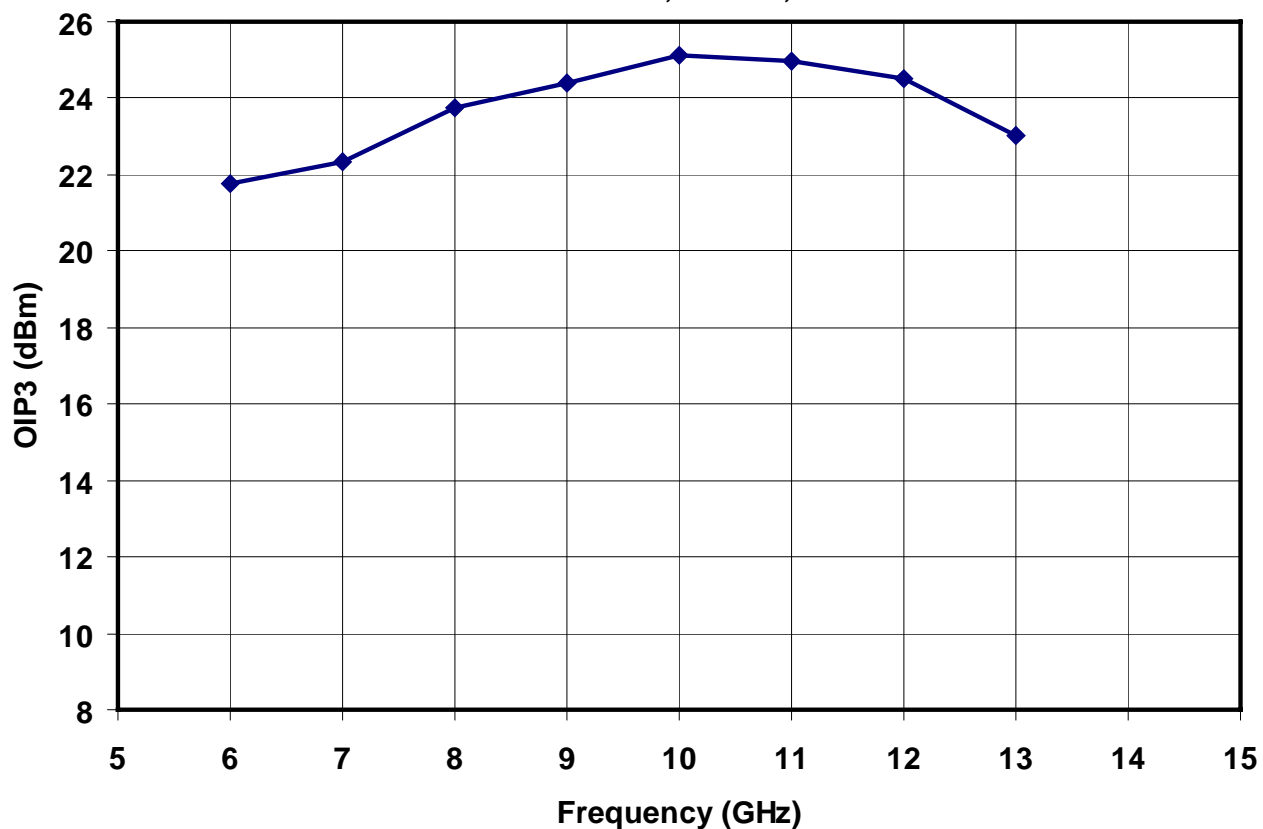
Measured Data

Bias Conditions: Gate Bias, $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$

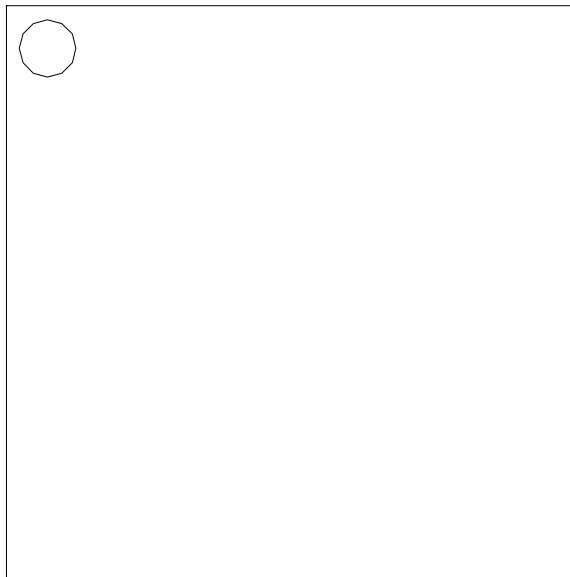


Measured Data

Bias Conditions: **Gate Bias**, $V_d = 5\text{ V}$, $I_d = 160\text{ mA}$

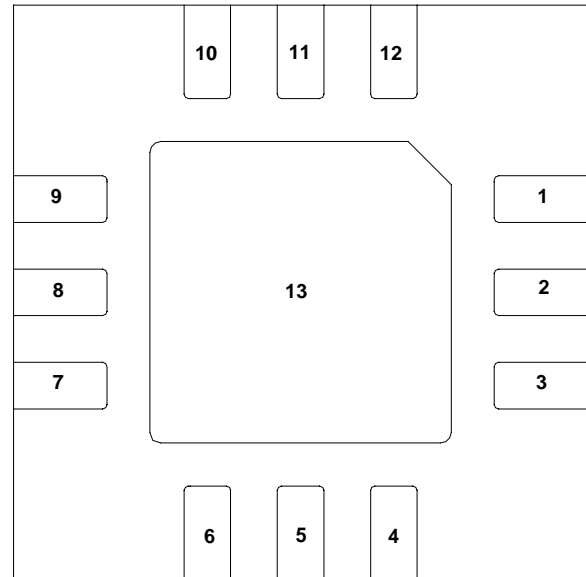


Package Pinout Diagram



Top View

Dot indicates Pin 1



Bottom View

Self Bias

Pin	Description
1,3, 4, 5, 6, 7, 9, 12	NC
2	RF Input
8	RF Output
10	Vd
11	Vctrl
13	Gnd

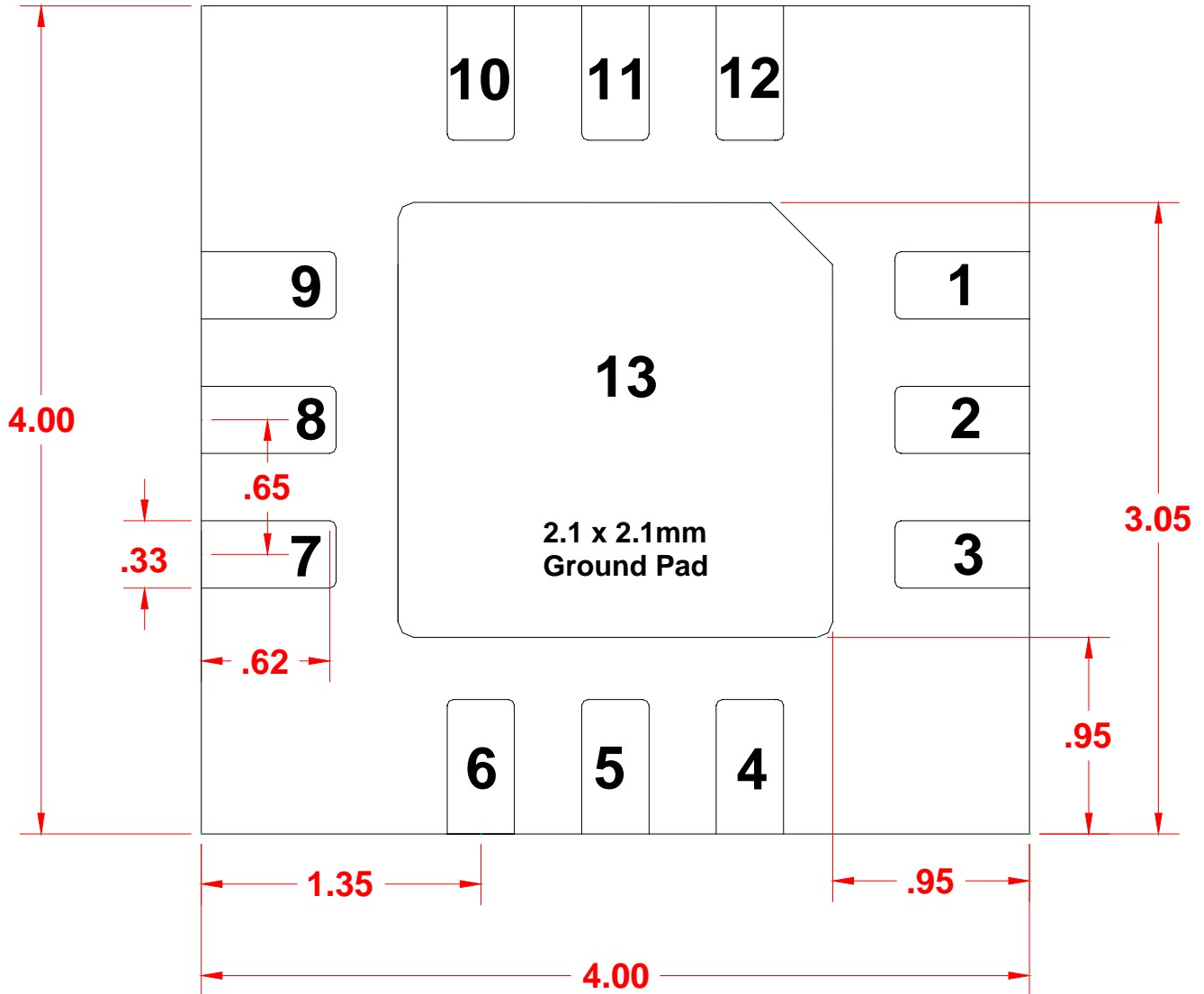
Self Bias: Vd = 5V (Id = ~90mA), Vctrl = 0 to +5V for Gain adjustment

Gate Bias

Pin	Description
1,3, 4, 5, 6, 7, 9	NC
2	RF Input
8	RF Output
10	Vd
11	Vctrl
12	Vg
13	Gnd

Gate Bias: Vd = 5V , Vctrl = 0 to +5V for Gain adjustment
Vg = Range, -0.5 to 0, typically ~ -0.1 will provide ~160mA of Id.

Mechanical Drawing



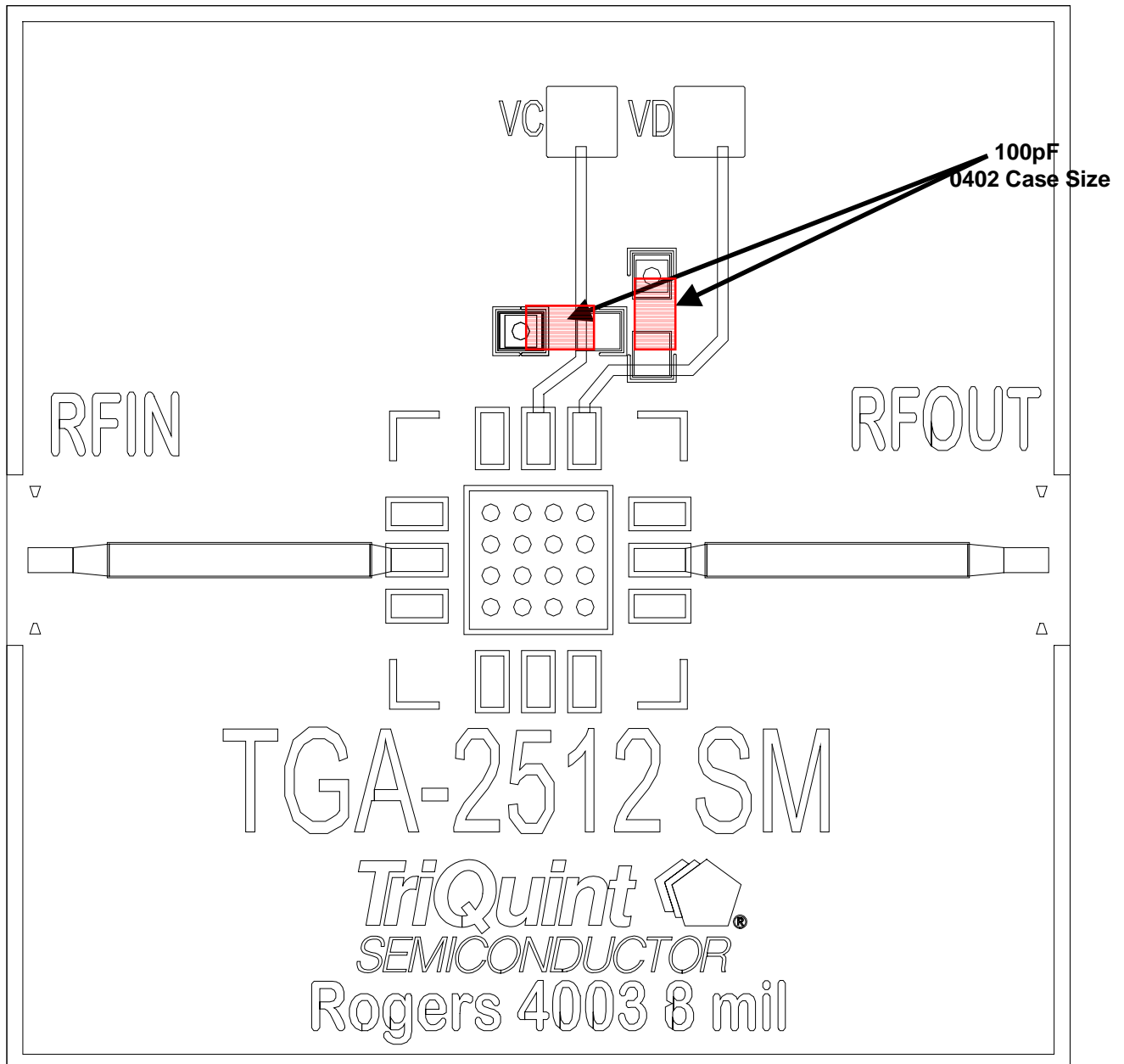
Bottom View

Units: Millimeters. Package tolerance: +/- 0.10

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

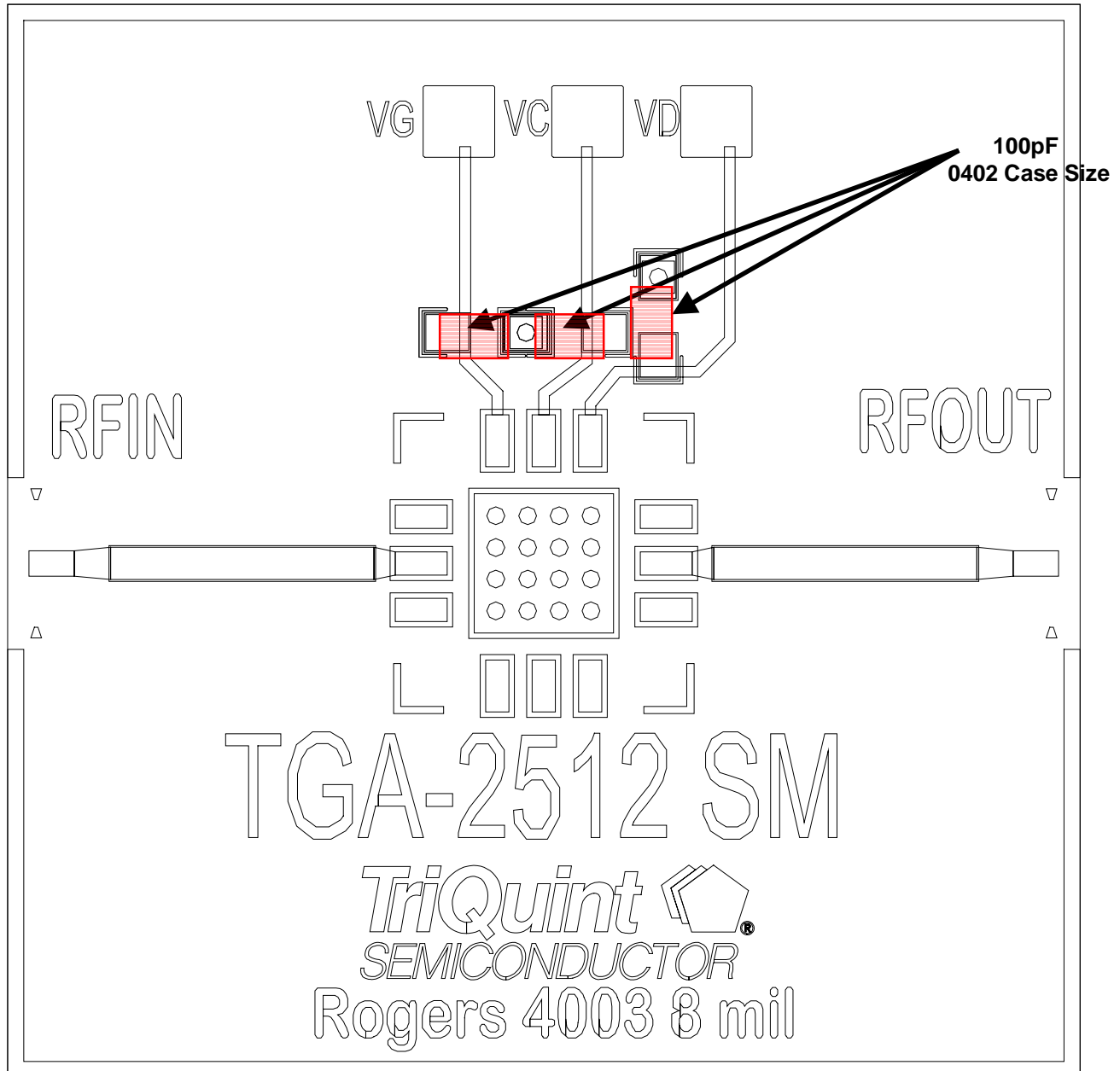
Recommended Board Layout Assembly

Self Bias



Recommended Board Layout Assembly

Gate Bias



Ordering Information

Part	Package Style
TGA2512-1-SM	QFN 4x4 Surface Mount – Self Bias
TGA2512-2-SM	QFN 4x4 Surface Mount – Gate Bias