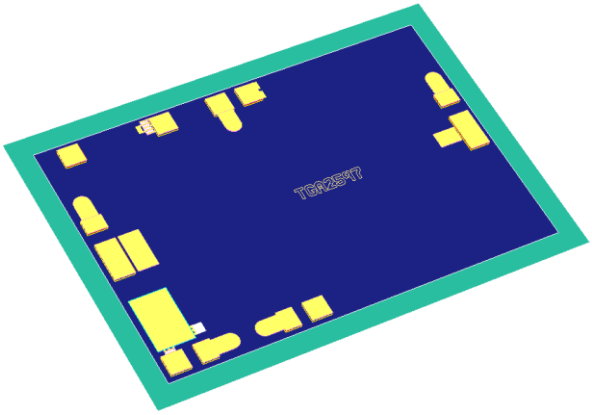
TGA2597

2-6 GHz GaN Driver Amplifier

General Description

Qorvo's TGA2597 is a driver amplifier fabricated on Qorvo's QGAN25 0.25 um GaN on SiC production process. The TGA2597 operates from 2.0 to 6.0 GHz and provides >31.5 dBm of output power with >13.5 dB of large signal gain and >31 % power-added efficiency.

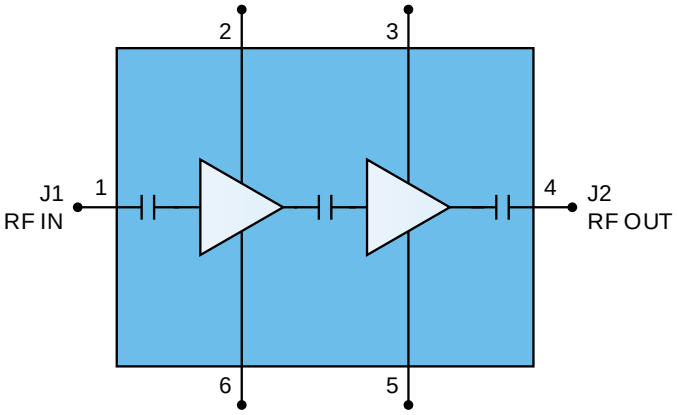
The TGA2597 operates with the same drain bias as corresponding GaN HPA's making it an ideal driver amplifier. It can also function as the output amplifier in lower power applications. The TGA2597 is internally matched to 50 ohms, and includes integrated DC blocks on both RF ports allowing for simple system integration.



Product Features

- Frequency Range: 2-6 GHz
- Output Power: > 31.5 dBm (P_{IN} = 18 dBm)
- PAE: > 31 % (P_{IN} = 18 dBm)
- Large Signal Gain: > 13.5 dB (P_{IN} = 18 dBm)
- Small Signal Gain: > 24 dB
- V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typ.
- Chip Dimensions: 2.140 mm x 1.500 mm x 0.10 mm

Functional Block Diagram



Applications

- Commercial and Military Radar
- Communications
- Electronic Warfare (EW)

Ordering Information

Part	Description
TGA2597	2-6 GHz GaN Driver Amplifier
TGA2597-SMEVB	TGA2597 Evaluation Board, Qty 1

Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
Drain Voltage (V_D)	-	40 V	V
Gate Voltage Range (V_G)	-8	0	V
1st Stage (I_{D1_DRIVE})	-	95	mA
2nd Stage (I_{D2_DRIVE})		305	mA
1st Stage (I_{G1}) (+I_{G1} @ T_{CH}=200 °C)	-0.2	1.4	mA
2nd Stage (I_{G2}) (+I_{G2} @ T_{CH}=200 °C)	-0.64	2.8	mA
Power Dissipation (P_{DISS})	-	5.4	W
Input Power, CW, 50 Ω (P_{IN}), @ 85 °C	-	24	dBm
Input Power, CW, 3:1 VSWR (P_{IN}) @ 85 °C	-	24	dBm
Channel temperature (T_{CH})	-	275	°C
Mounting Temperature (30 Seconds maximum)	-	320	°C
Storage Temperature	-55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter [1]	Min	Typical	Max	Units
Drain Voltage (V_D)		25		V
Drain Current (I_{DQ})		40		mA
Drain Current w/ RF Drive (I_{D_DRIVE}) [2]		200		mA
Gate Voltage (V_G), typ.		-2.5		V
Gate leakage (Test conditions: V_D = 10 V, V_G is at threshold voltage)	-0.84	- 0.042		mA

1 Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions

2 See drain current plot under RF drive

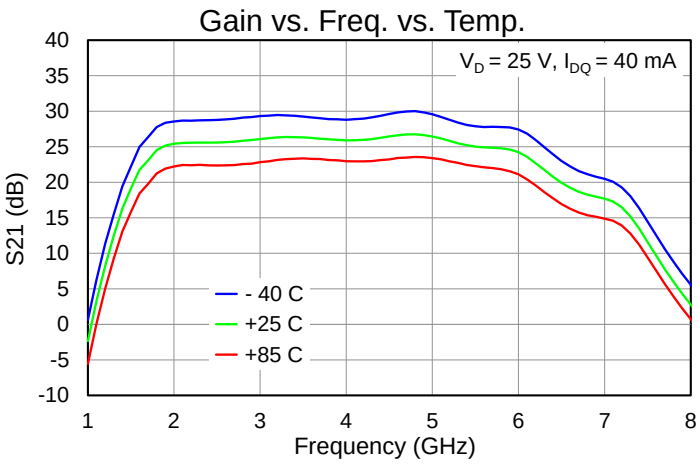
Electrical Specifications

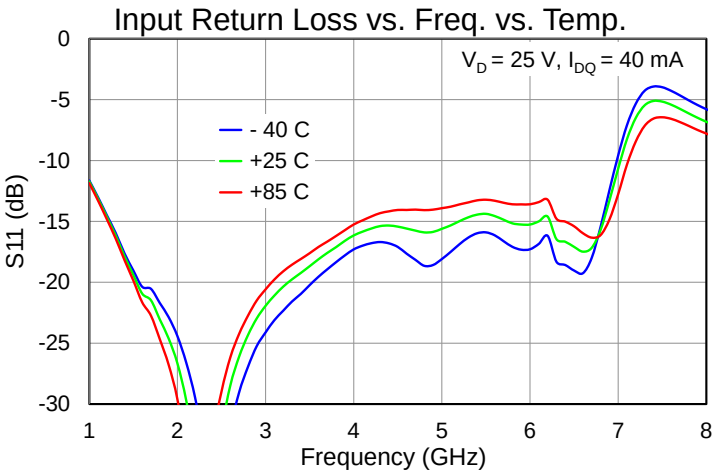
Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typ., data de-embedded to reference plans

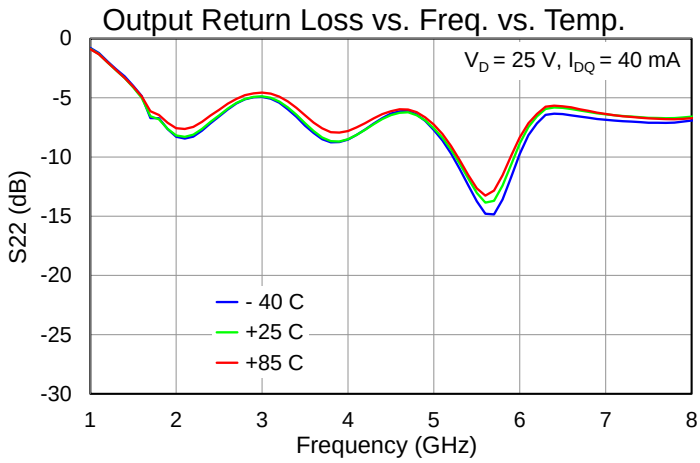
Parameter	Min	Typical	Max	Units
Operating Frequency Range	2.0		6.0	GHz
Output Power (@ Pin = 18 dBm)		> 31.5		dBm
Power Added Efficiency (@ Pin = 18 dBm)		> 31		%
Small Signal Gain		> 24		dB
Input Return Loss		> 15		dB
Output Return Loss		> 5		dB
IM3 (Pout/Tone ≤ 24 dBm, 10 MHz tone spacing)		< -25		dBc
Small Signal Gain Temperature Coefficient		-0.050		dB/°C
Output Power Temperature Coefficient		-0.001		dB/°C

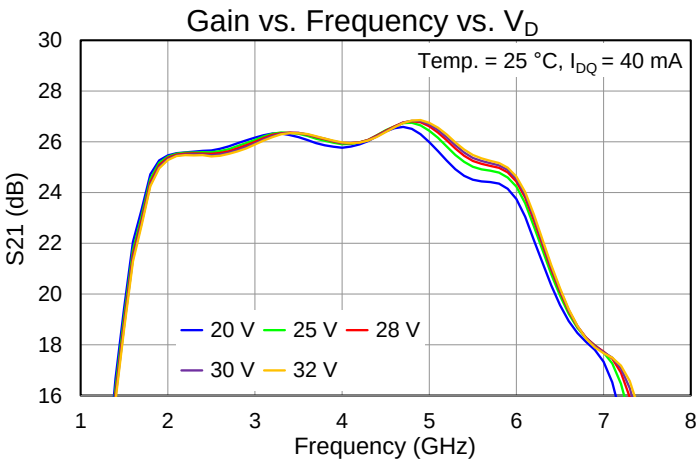
Typical Performance–Small Signal

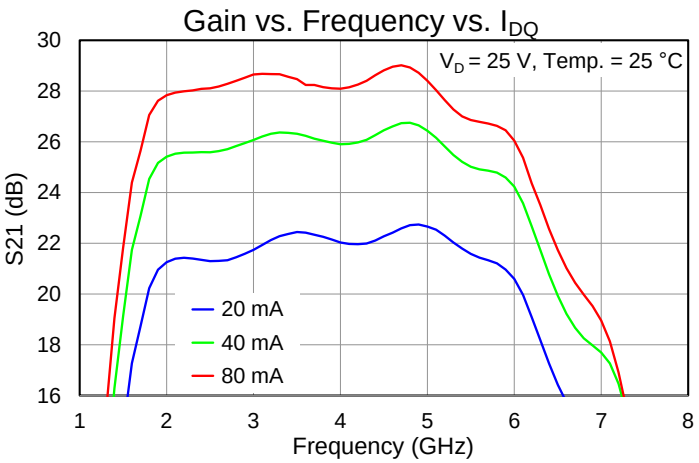
Test conditions unless otherwise noted: 25 °C, VD = 25 V, IDQ = 40 mA, VG = -2.5 V typical





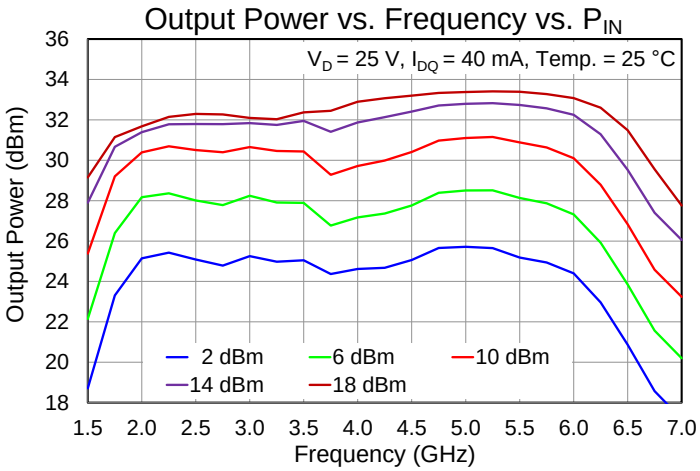


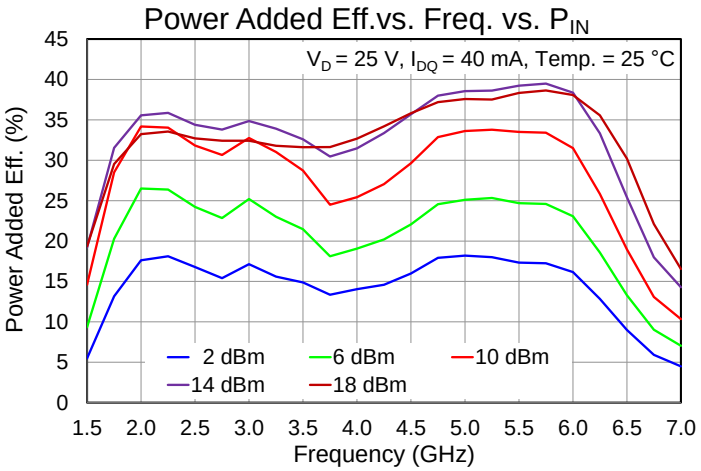


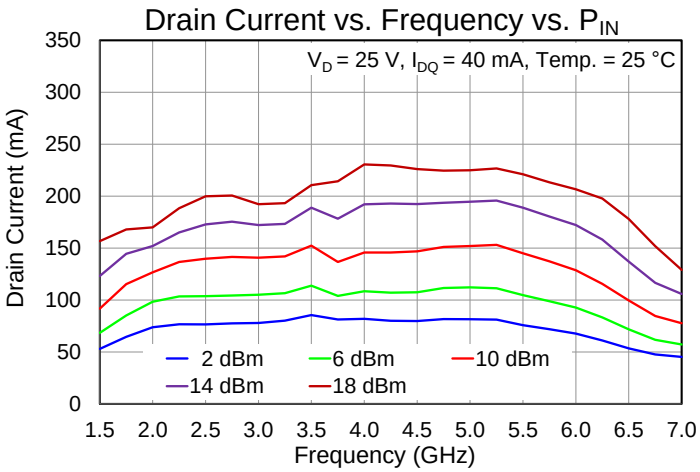


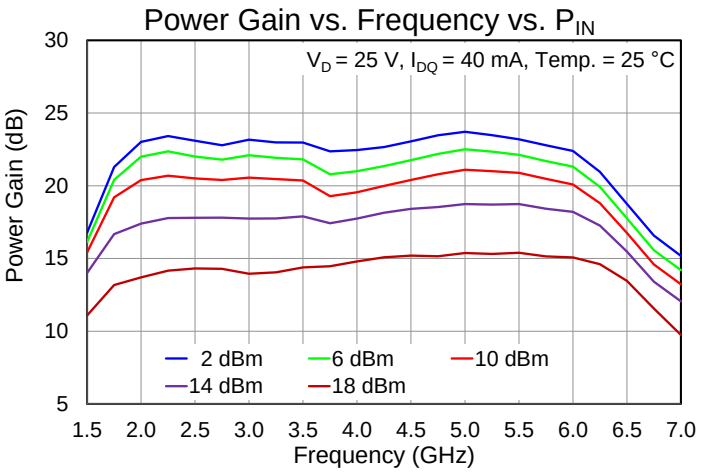
Typical Performance–Large Signal

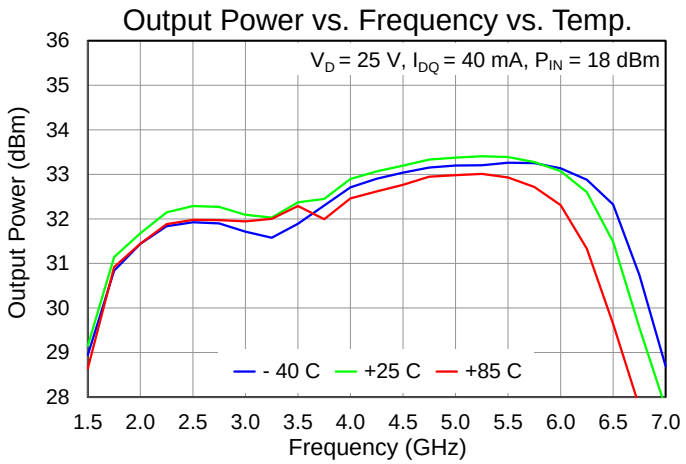
Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typical

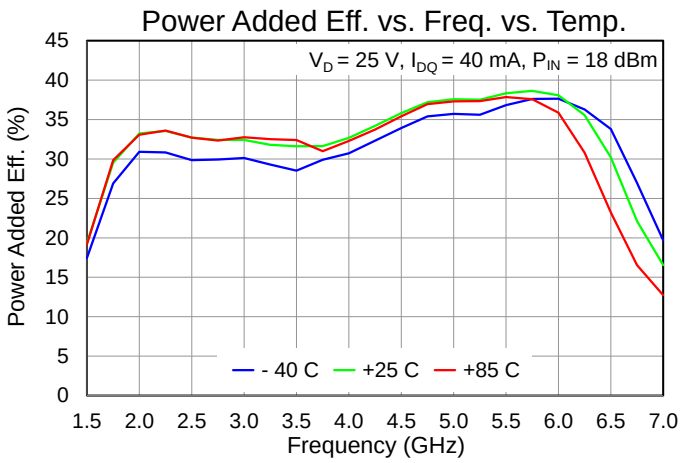






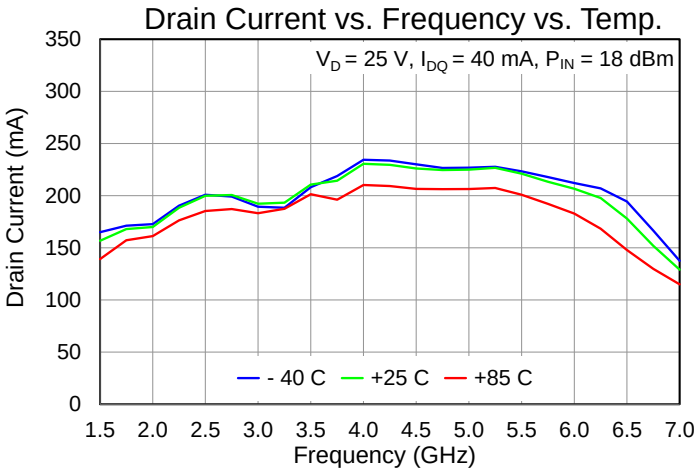


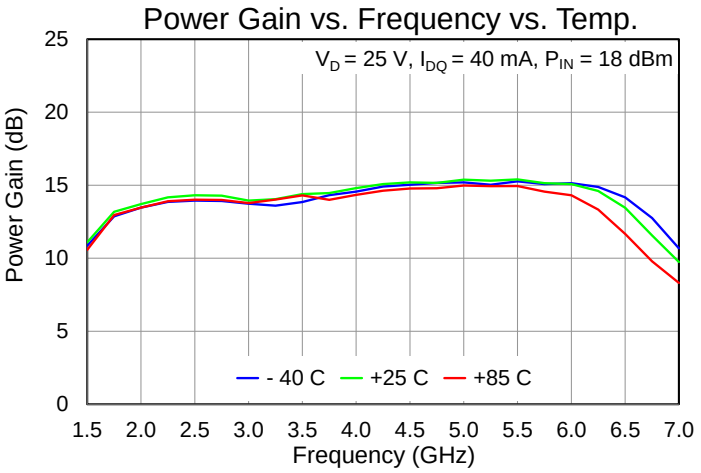


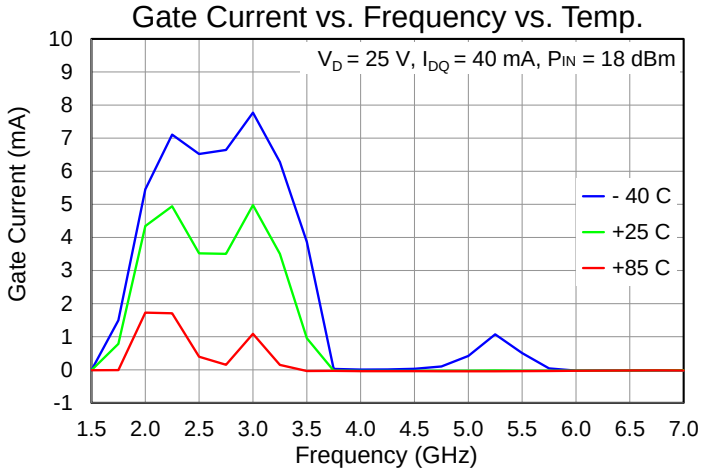


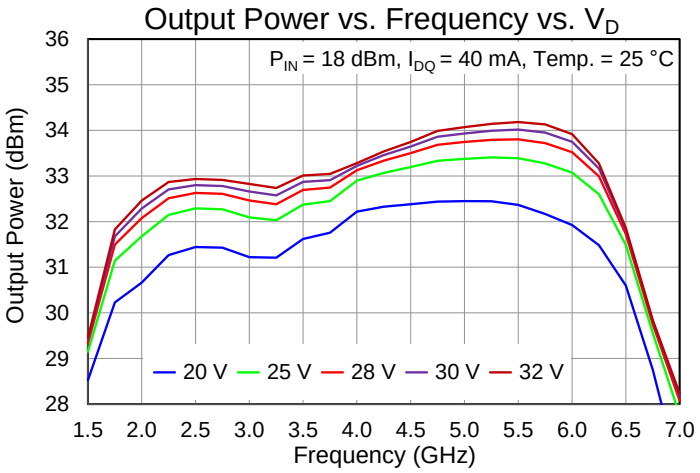
Typical Performance–Large Signal

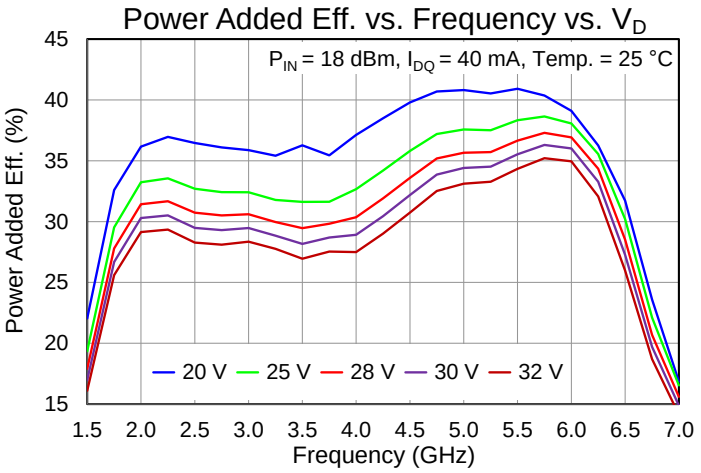
Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typical







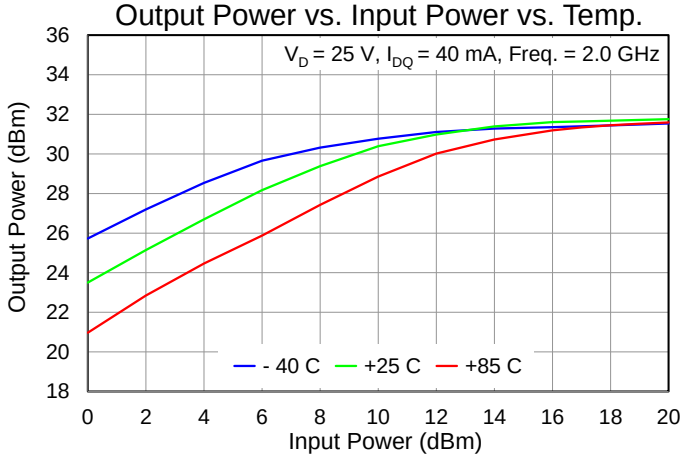




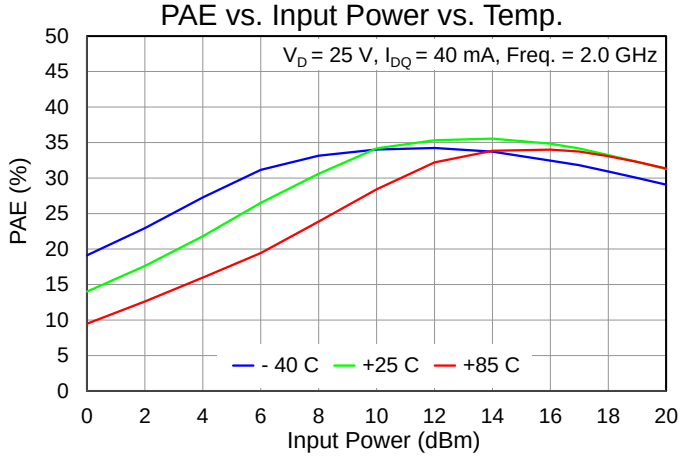
Typical Performance–Large Signal

Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typical

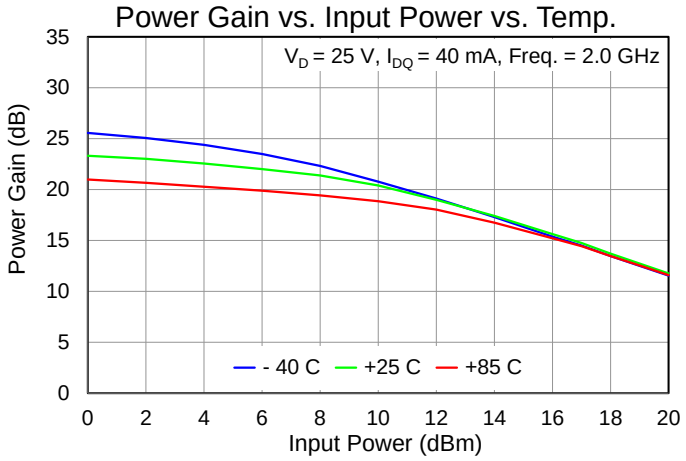
Output Power vs. Input Power vs. Temp.



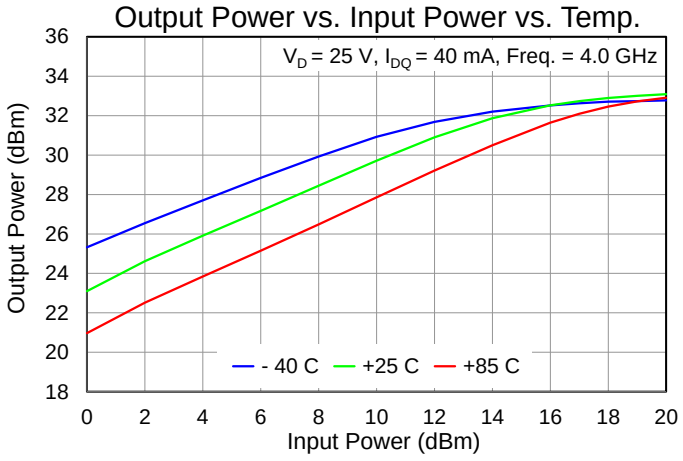
PAE vs. Input Power vs. Temp.



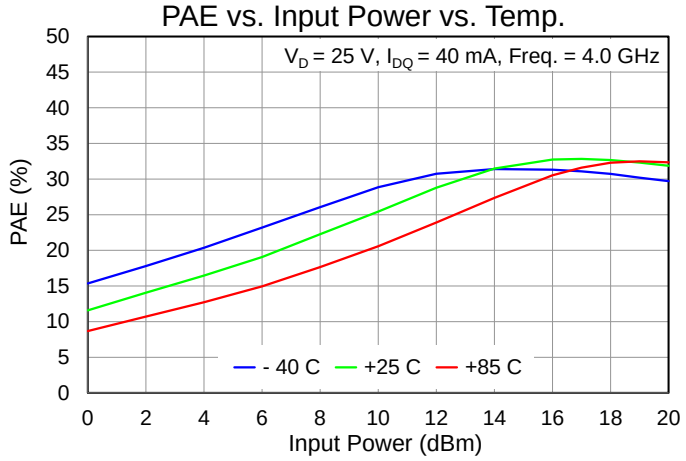
Power Gain vs. Input Power vs. Temp.



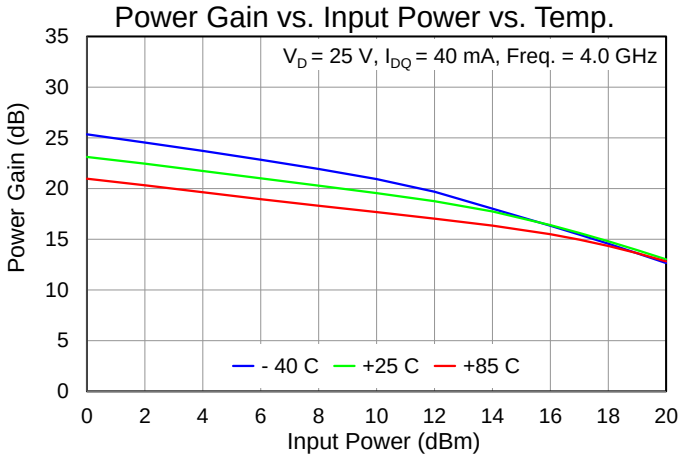
Output Power vs. Input Power vs. Temp.



PAE vs. Input Power vs. Temp.



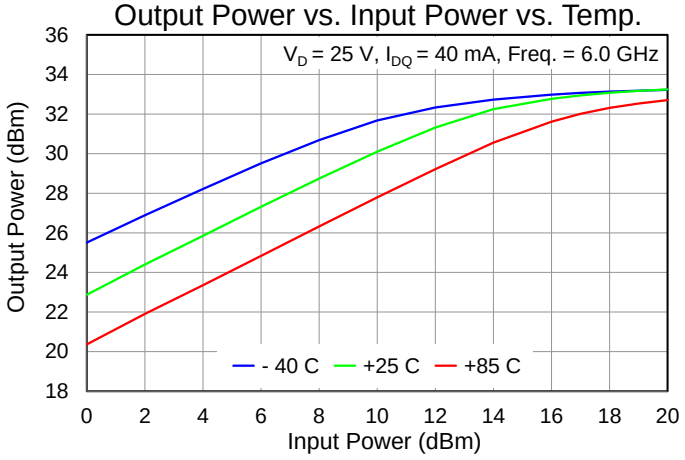
Power Gain vs. Input Power vs. Temp.



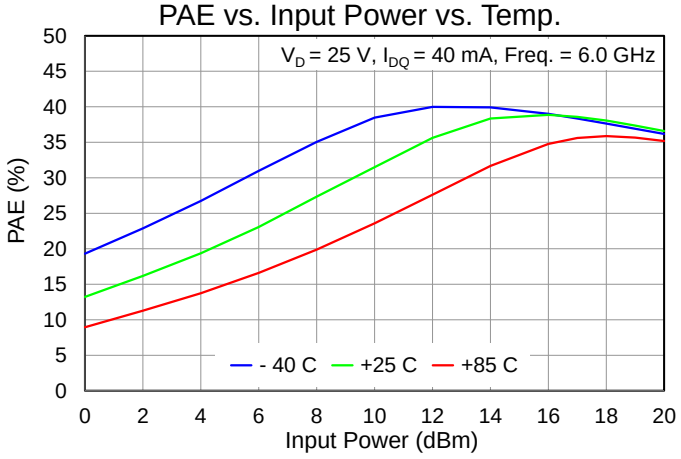
Typical Performance–Large Signal, Harmonics

Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typical

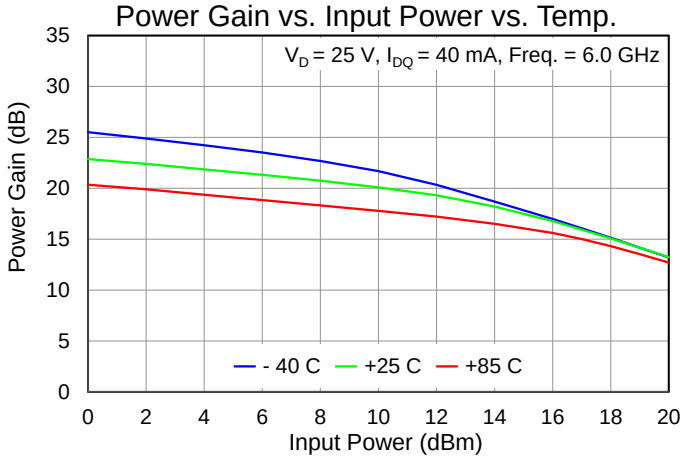
Output Power vs. Input Power vs. Temp.



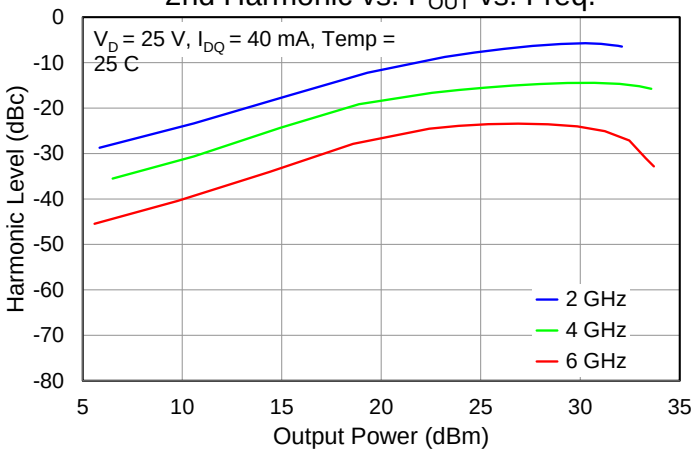
PAE vs. Input Power vs. Temp.



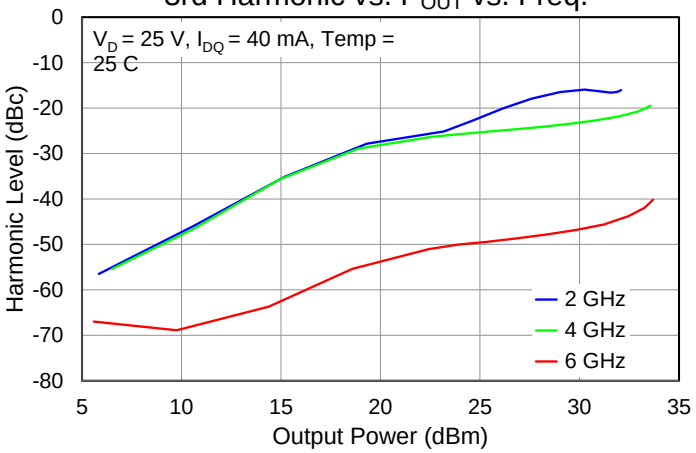
Power Gain vs. Input Power vs. Temp.



2nd Harmonic vs. P_{OUT} vs. Freq.



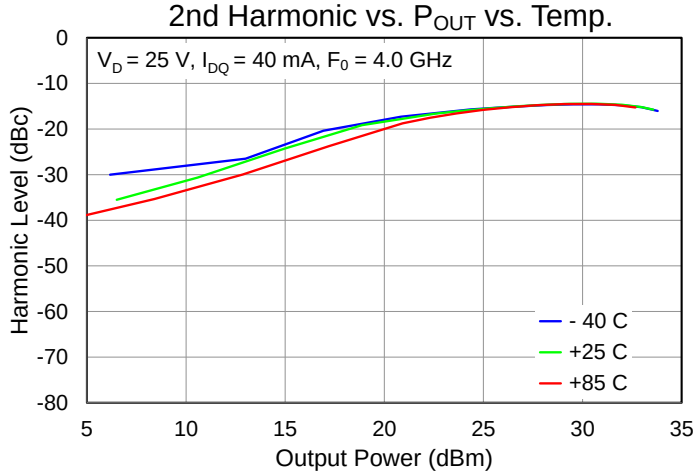
3rd Harmonic vs. P_{OUT} vs. Freq.



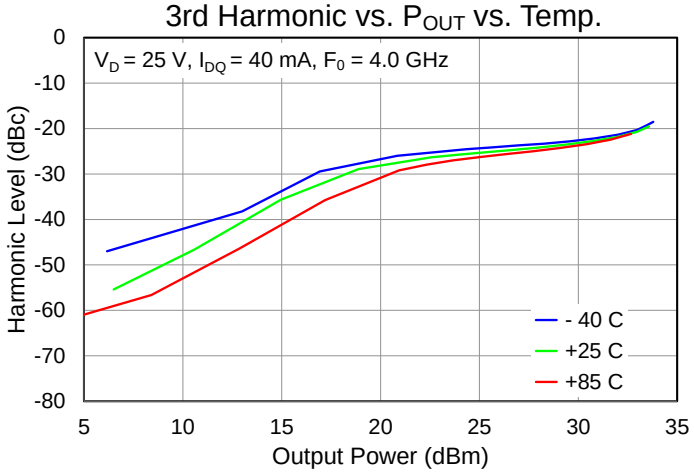
Typical Performance–Harmonics, Linearity

Test conditions unless otherwise noted: 25 °C, V_D = 25 V, I_{DQ} = 40 mA, V_G = -2.5 V typical

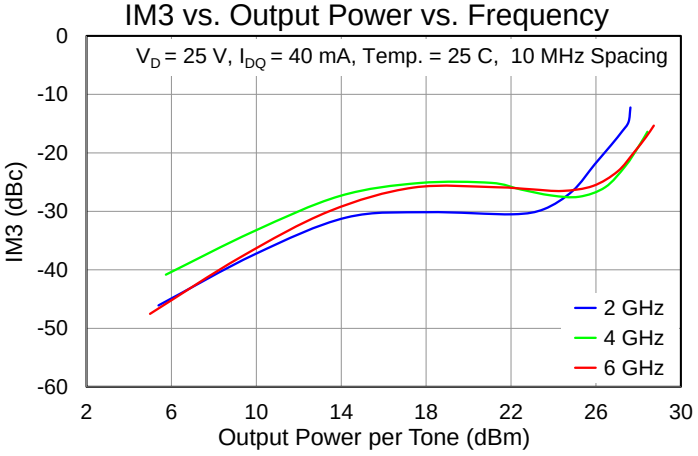
2nd Harmonic vs. P_{OUT} vs. Temp.



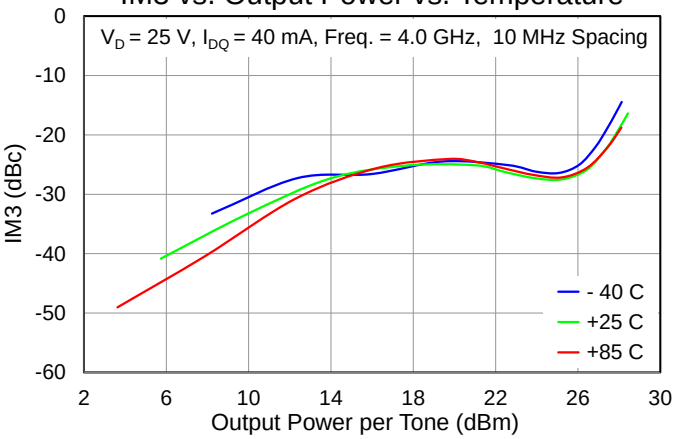
3rd Harmonic vs. P_{OUT} vs. Temp.



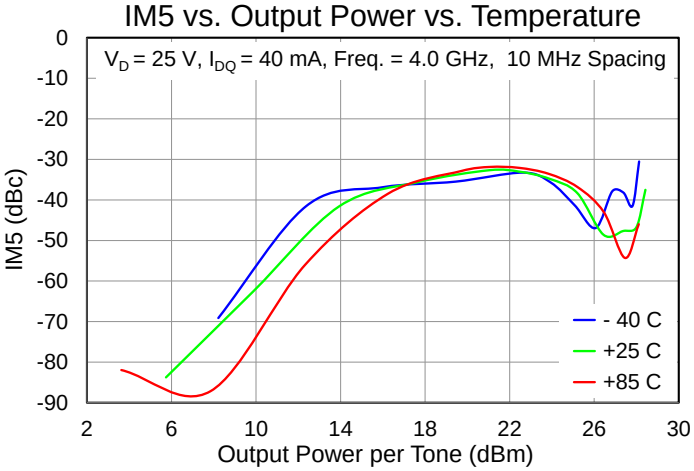
IM3 vs. Output Power vs. Frequency



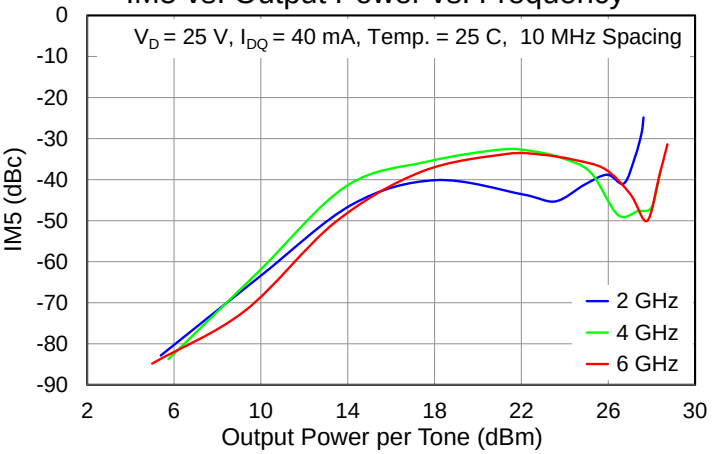
IM3 vs. Output Power vs. Temperature



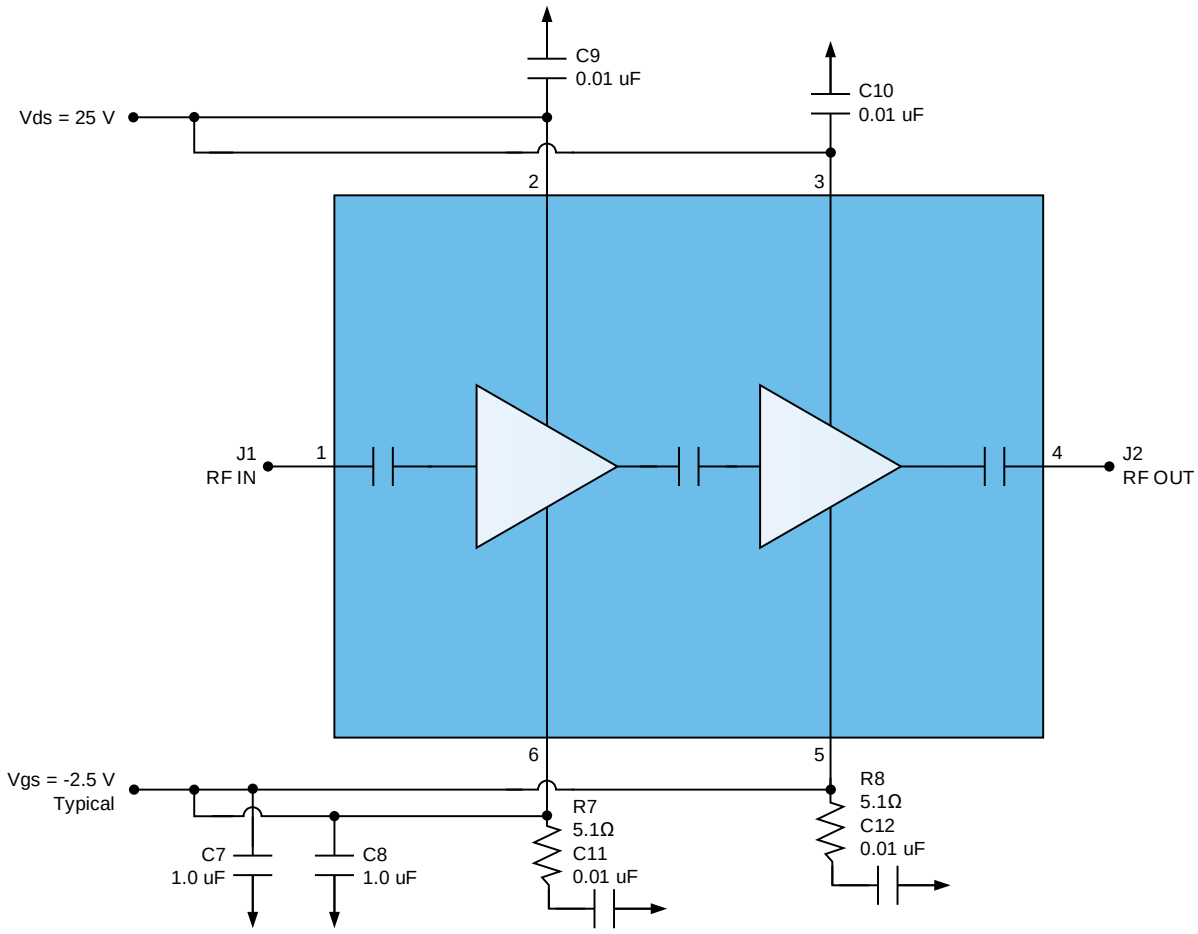
IM5 vs. Output Power vs. Temperature



IM5 vs. Output Power vs. Frequency



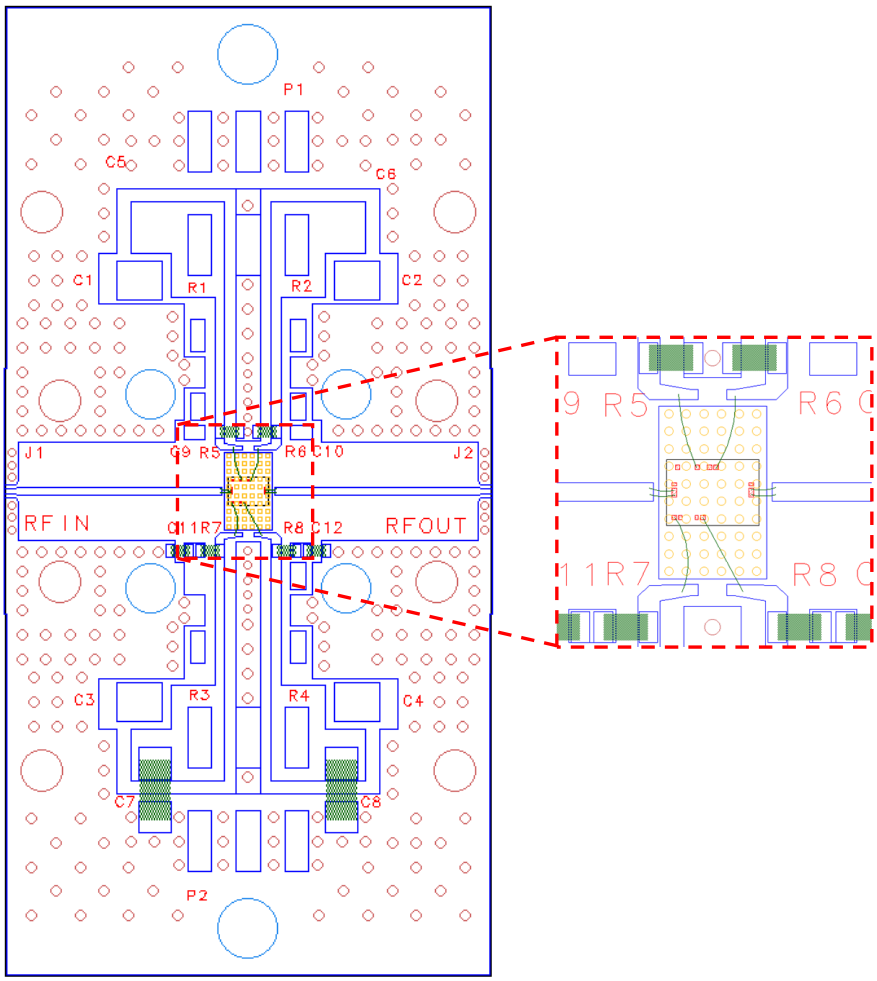
Application Circuit



Bias-up Procedure
Set I_D limit to 400 mA, I_G limit to 4.5 mA
Set V_G to -5.0 V
Set V_D +25 V
Adjust V_G more positive until I_{DQ} = 40 mA.
Apply RF signal

Bias-down Procedure
Turn off RF signal
Set V_G to -5.0 V. Ensure I_{DQ} ~ 0mA
Set V_D to 0 V
Turn off V_D supply
Turn off V_G supply

Evaluation Board

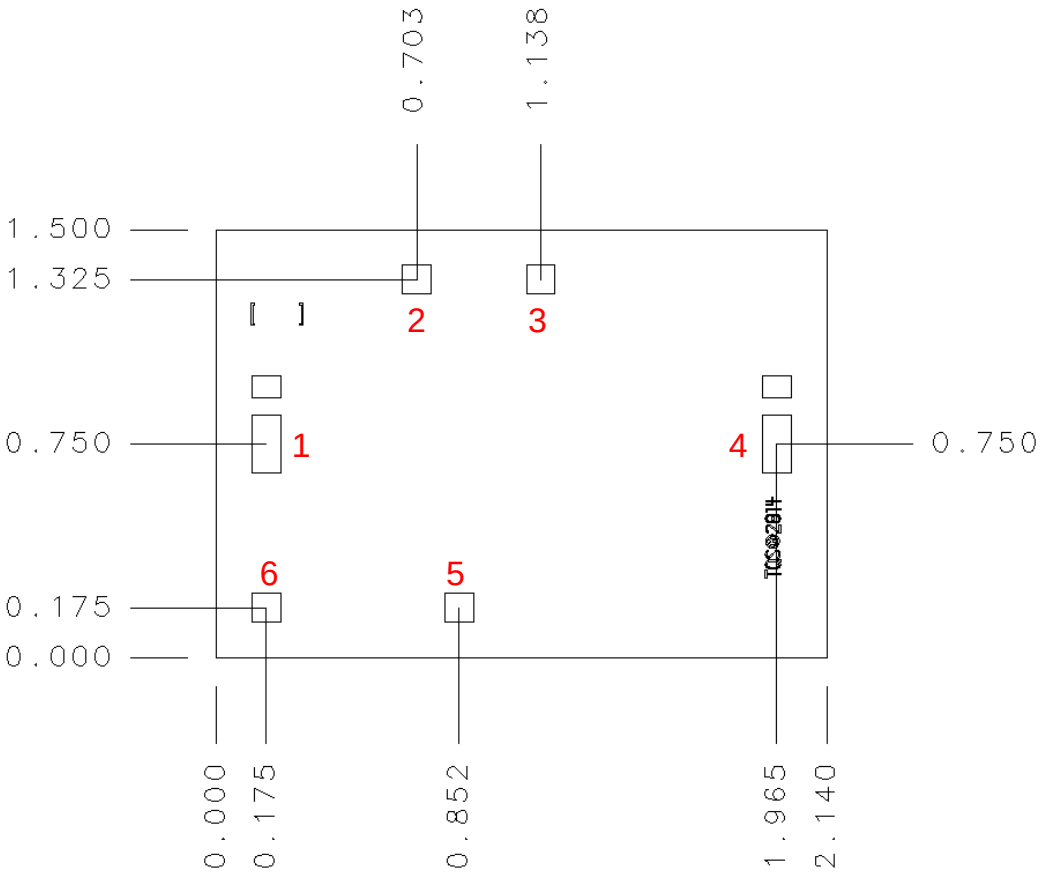


RF Layer is 0.008” thick Rogers Corp. RO4003C, εr = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5. Die attach is accomplished with conductive epoxy. The PCB land pattern has been developed to accommodate bond wire and die tolerances.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
R7–R8	5.1 Ohm	Res, 0402, 5% ROHS	Various	
C7–C8	1.0 uF	Cap, 1206, 16 V, 20%, X5R	Various	
C9–C12	0.01 uF	Cap, 0402, 50 V, 10%, X7R	Various	

Mechanical Drawing & Bond Pad Description



Unit: millimeters, Die thickness: 0.10, Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad, Ground is backside of die

Bond Pad	Symbol	Pad Size	Description
1	RF In	100 x 200	RF Input; matched to 50 ohms; AC coupled.
2	V_{D1}	100 x 100	Drain voltage, first stage.
3	V_{D2}	100 x 100	Drain voltage, second stage.
4	RF Out	100 x 200	RF Output; matched to 50 ohms; AC coupled.
5	V_{G2}	100 x 100	Gate voltage, second stage.
6	V_{G1}	100 x 100	Gate voltage, first stage.

Thermal and Reliability Information

Parameter	Values	Units	Conditions
TX Channel, Thermal Resistance (θ_{JC}) (1,2)	11.77	°C/W	T_{BASE} = 85°C, V_D = 25 V, I_{DQ} = 40 mA, I_{D_DRIVE} = 208 mA, P_{IN} = 18 dBm, P_{OUT} = 32.5 dBm, P_{DISS} = 3.5 W
Channel Temperature (T_{CH})	126.2	°C	

Notes:
1. Thermal resistance is measured to die backside
2. Base or ambient temperature is 85 °C
3. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C	ESDA / JEDEC JS-002-2014

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: **www.qorvo.com**

Email: **customer.support@qorvo.com**

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