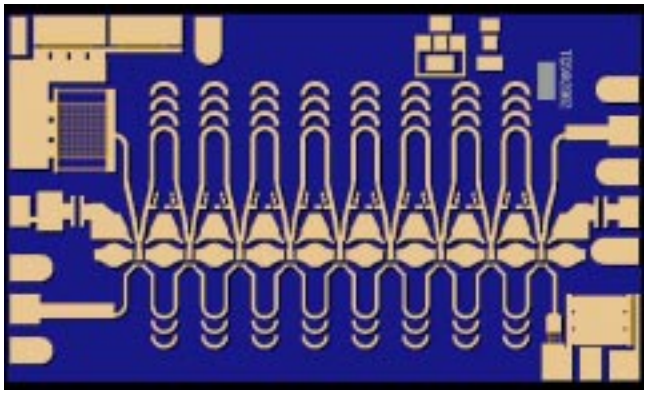
12.5Gb/s Modulator Driver Amplifier TGA4802-EPU

Metro and Long Haul Applications



Key Features and Performance

- Frequency Range: DC - 25 GHz
- Single-ended Input / Output
- 15 dB Small Signal Gain
- 18 GHz Small Signal Bandwidth
- Wide Drive Range (3V to 7V)
- 15ps Edge Rates (20/80)
- Power Dissipation 1.2 Watts
- 0.25um pHEMT 2MI Technology
- Die Size: 3.3 x 2.0 x 0.1 mm
  (0.131 x 0.79 x 0.004 inches)

Description

The TriQuint TGA4802 is part of a series of optical driver amplifiers suitable for a variety of driver applications.

The TGA4802 is a medium power wideband AGC amplifier MMIC die that typically provides 15dB small signal gain with 10dB AGC range. RF ports are DC coupled enabling the user to customize system corner frequencies.

The TGA4802 is an excellent choice for 12.5Gb/s optical modulator driver applications. The TGA4802 has demonstrated capability to amplify a 2V input signal to 7Vpp saturated.

The TGA4802 requires off-chip decoupling, a DC block and a bias tee. The TGA4802 is available in die form.

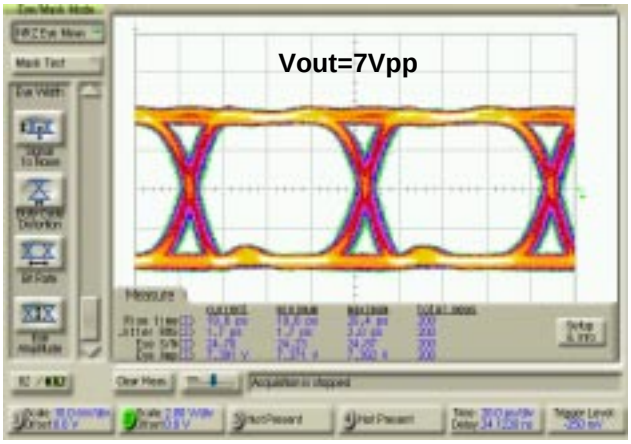
Primary Applications

- Mach-Zehnder Modulator Driver for Metro and Long Haul

Measured Performance

TGA4802 Fixtured Data
Vd(Rfout)=6V, Id=170mA, (Pdc=1.2W)
Vout=7Vpp, Vin = 2Vpp
Scale: 2V/div, 20ps/div

12.5Gb/s **Vin=2V**



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

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TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
	POSITIVE SUPPLY VOLTAGE		
Vd	Drain Voltage at RF output	7 V	2/
	POSITIVE SUPPLY CURRENT		
Id	Drain Current	200 mA	2/
P_d	POWER DISSIPATION	1.4 W	2/, 3/
	NEGATIVE GATE		
Vg	Voltage	0 V to –3 V	
Ig	Gate Current	5 mA	
	CONTROL GATE		
Vctrl	Voltage	Vd/2 to –3 V	4/
Ictrl	Gate Current	5 mA	
	RF INPUT		
P_{IN}	Sinusoidal Continuous Wave Power	23 dBm	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 ^{0}C	5/, 6/
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 ^{0}C	
T_{STG}	STORAGE TEMPERATURE	-65 to 150 ^{0}C	

Notes:

1/ These ratings represent the maximum operable values for the device.

2/ Assure the combination of Vd and Id does not exceed maximum power dissipation rating.

3/ Assure Vctrl never exceeds Vd during bias on and off sequences, and normal operation.

4/ When operated at this bias condition with a base plate temperature of 70^{0}C, the median life is reduced.

5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

TABLE II
DC PROBE TEST
(TA = 25 °C, nominal)

NOTES	SYMBOL	LIMITS		UNITS
		MIN	MAX	
1/	$\|V_{BVGS}\|$	11	30	V
1/	$\|V_{BVGD}\|$	11	30	V

Notes:

1 V_{BVGS} and V_{BVDS} are negative.

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TABLE III
RF SPECIFICATIONS

(T_A = 25°C Nominal)

Bias Conditions: Vd = 7V Id = 170 mA

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			18		GHz
1/	SMALL-SIGNAL GAIN MAGNITUDE	2 - 10 GHz 12 - 18 GHz	14 10			dB
1/	INPUT RETURN LOSS MAGNITUDE	2 - 14 GHz		10		dB
1/	OUTPUT RETURN LOSS MAGNITUDE	2 - 14 GHz		12		dB
2/ 3/	SATURATED OUTPUT POWER	2 - 12 GHz	22			dBm
2/, 3/	EYE AMPLITUDE	Vd(RFout) = 6V Vd(RFout) = 5V Vd(RFout) = 4V	7.0 6.0 5.0			Vpp
2/, 4/	ADDITIVE JITTER			5		ps
2/, 4/	RISE TIME (20/80)			15		ps

Notes:

1/ RF Probe Bias: V^+ = 8 V, adjust Vg1 to achieve Id = 80 mA, Vctrl = +1.5 V

2/ Verified by design, TGA4802 assembled onto an evaluation platform as shown on page 9 then tested using the application circuit and bias procedure detailed on pages 7 and 8.

3/ Vin = 2 V, Data Rate = 12.5 Gb/s, Vctrl and Vg are adjusted for maximum output.

4/ Computed using RSS Method where Jpp_additive = SQRT(Jpp_out^2 - Jpp_in^2)

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TABLE IV
THERMAL INFORMATION*

PARAMETER	TEST CONDITIONS	T_{CH} (^oC)	$R_{\theta JC}$ (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd (RF out) = 7 V I_D = 170 mA Pdiss = 1.2 W	110	32.7	4.2 E+7

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated. Thermal transfer is conducted thru the bottom of the TGA4802 into the mounting carrier. Design the mounting interface to assure adequate thermal transfer to the base plate.

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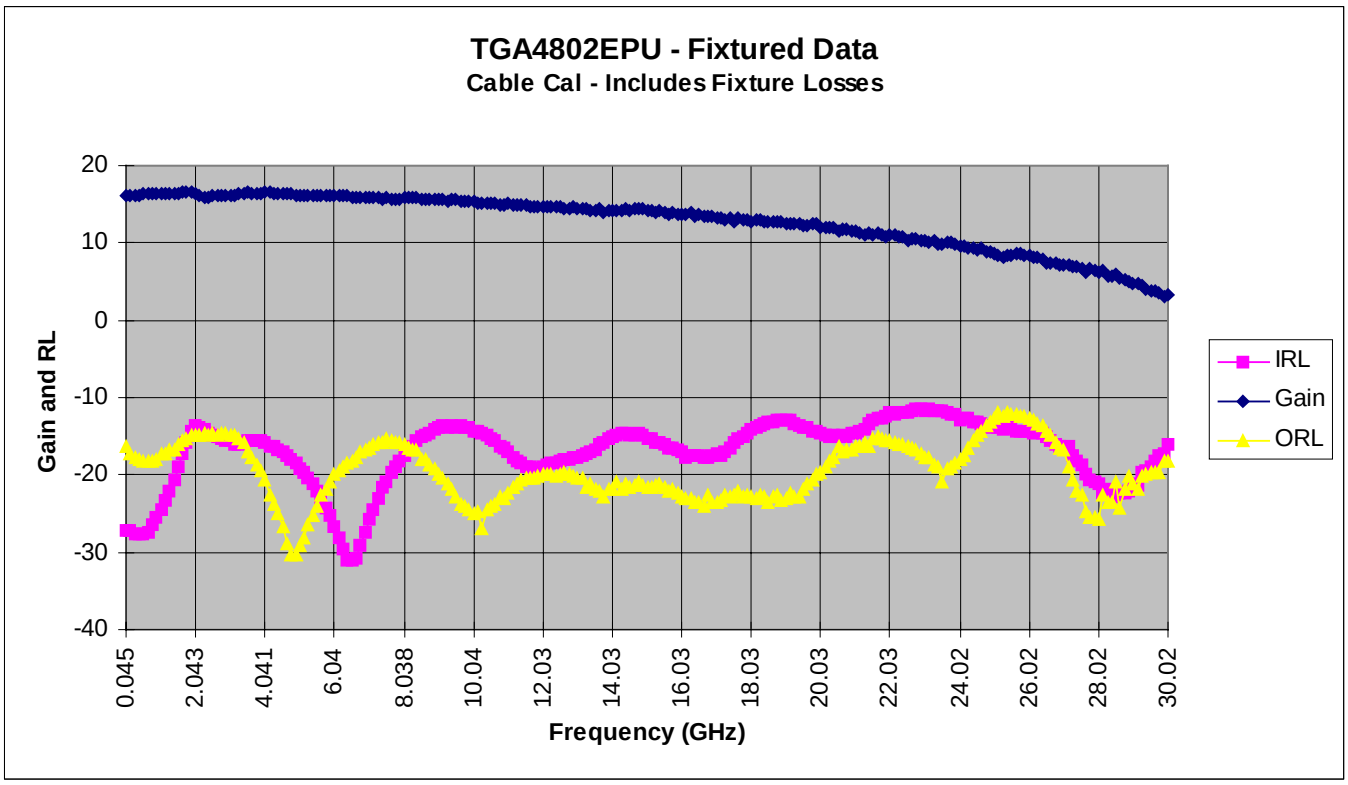
Measured Fixtured Data

Bias Conditions: Vd = 7V, Id= 170mA



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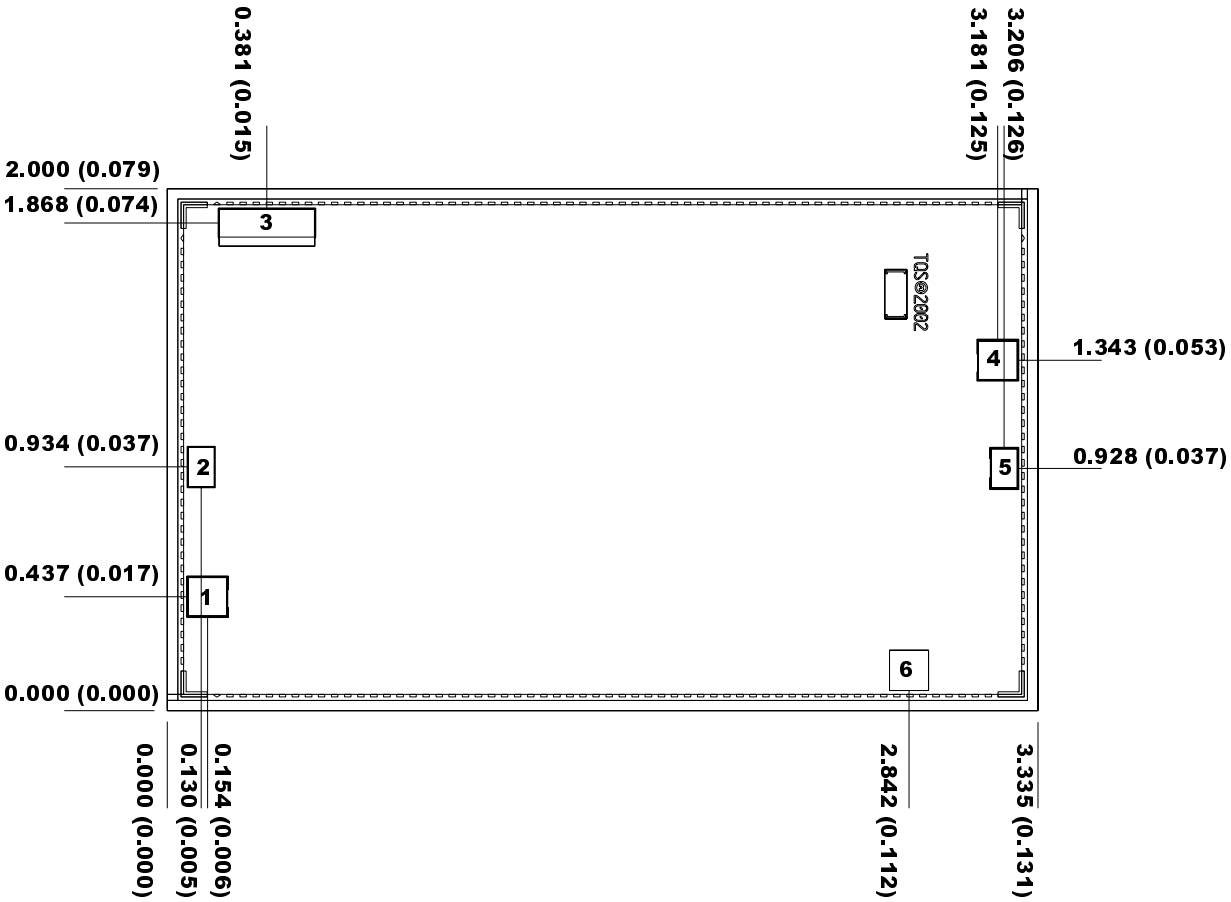
Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

Bond pad #1	**(RF In)**	**0.150 x 0.150 (0.006 x 0.006)**
Bond pad #2	**(Vctrl)**	**0.100 x 0.150 (0.004 x 0.006)**
Bond pad #3	**(V+)**	**0.366 x 0.108 (0.014 x 0.004)**
Bond pad #4	**(RF Out)**	**0.155 x 0.155 (0.006 x 0.006)**
Bond pad #5	**(Vctrl aux)**	**0.100 x 0.150 (0.004 x 0.006)**
Bond pad #6	**(Vg)**	**0.150 x 0.150 (0.006 x 0.006)**

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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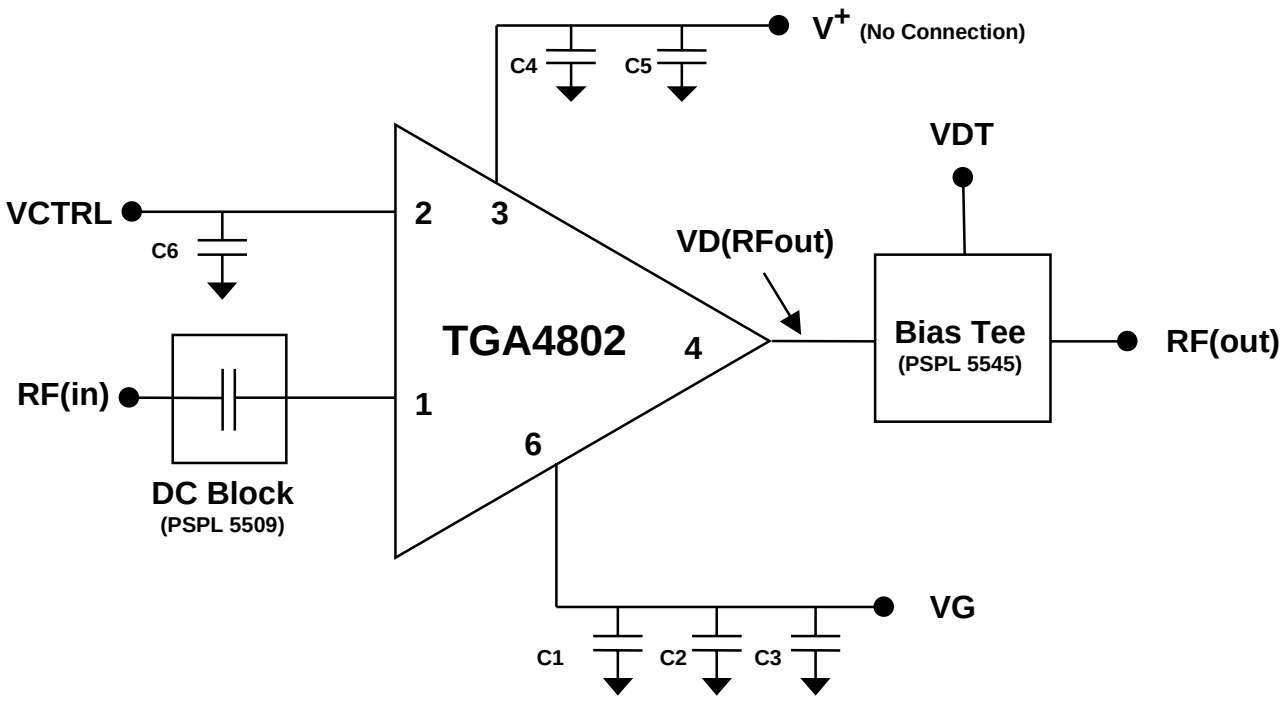
TGA4802 Application Circuit



Notes:

Recommended Components are detailed on page 9.

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Bias Procedure for 7V Output

Bias ON

1. Disable the RF source (PPG)
2. Set VdT=0V Vctrl=0V and Vg=0V
3. Set Vg=-1.5V
4. Increase VdT to 7V observing Id.
   - Assure Id=0mA
5. Set Vctrl=+1.0V
   - Id should still be 0mA
6. Make Vg more positive until **Idd=170mA**.
   - Typical value for **Vg is -0.2V**
7. Measure V^+, adjust VdT such that V^+ is 6V.
   - This will set Vd(RFout) to approximately 6V.
   - Idd will increase slightly
8. Adjust Vg such that Idd=170mA.
9. Enable the RF source (PPG)
   - Set Vin=2V
10. Output Swing Adjust: Adjust Vctrl slightly positive to increase output swing or adjust Vctrl slightly negative to decrease the output swing.
    - Typical value for Vctrl is +1.0V for Vo=7V.
11. Crossover Adjust: Adjust: Vg slightly positive to push the crossover down or adjust Vg slightly negative to push the crossover up.
    - Typical value for Vg is -0.2V to center crossover with Vo=7V.

Bias OFF

1. Disable the output of the PPG
2. Set Vctrl=0V
3. Set VdT=0V
4. Set Vg=0V

Notes:

1. Assure Vctrl never exceeds Vd during Bias ON and Bias OFF sequences and during normal operation.

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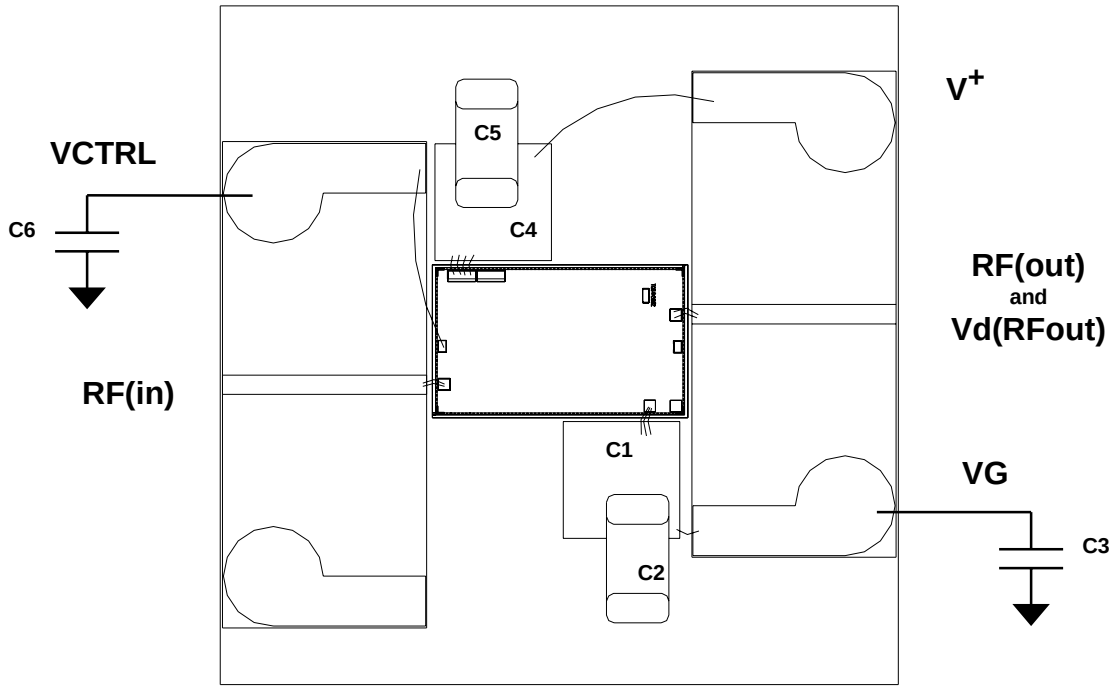
Evaluation Platform Assembly Diagram



Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C4	1500pF Capacitor SLC	Presidio	SL5050X7R1522H5
C2, C5	0.1uF Capacitor MLC Ceramic	AVX	0603YC104KAT
C3	10uF Capacitor MLC Ceramic	AVX	0603YC102KAT
C6	0.01 uF Capacitor MLC	AVX	0603YC103KAT

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Evaluation Platform Assembly Notes

Assembly Notes:

Reflow Attachment:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300▪C
- Use alloy station or conveyor furnace with reducing atmosphere
- No fluxes should be utilized
- Coefficient of thermal expansion matching is critical for long-term reliability
- Storage in dry nitrogen atmosphere

Adhesive Attachment:

- Organic attachment can be used in low-power applications
- Curing should be done in a convection oven; proper exhaust is a safety concern
- Microwave or radiant curing should not be used because of differential heating
- Coefficient of thermal expansion matching is critical

Component Pickup and Placement:

- Vacuum pencil and/or vacuum collet preferred method of pick up
- Avoidance of air bridges during placement
- Force impact critical during auto placement

Interconnect:

- Thermosonic ball bonding is the preferred interconnect technique
- Force, time, and ultrasonics are critical parameters
- Aluminum wire should not be used
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- Maximum stage temperature: 200▪C

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