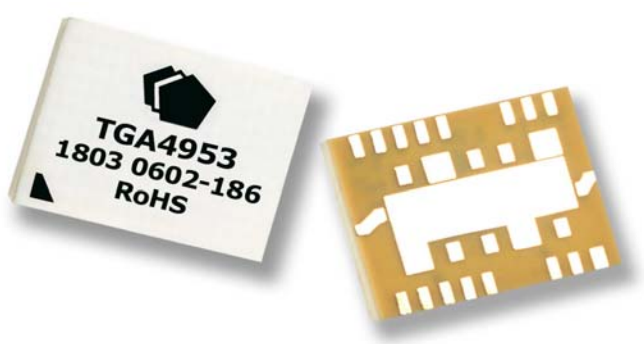
9.9-12.5Gb/s Optical Modulator Driver TGA4953-SCC-SL

OC-192 Metro and Long Haul Applications
Surface Mount Package



Key Features and Performance

- Metro MSA Compatible
- Wide Drive Range (3V to 10V)
- Single-ended Input / Output
- Low Power Dissipation
  (1.2W at Vo = 6V)
- Very Low Rail Ripple
- 25ps Edge Rates (20/80)
- Small Form Factor
  - 11.4 x 8.9 x 2 mm
  - 0.450 x 0.350 x 0.080 inches
- Evaluation Board Available.

Primary Applications

- Mach-Zehnder Modulator Driver for Metro and Long Haul
- IRZ & Duobinary Applications

Description

The TriQuint TGA4953-SCC-SL is part of a series of surface mount modulator drivers suitable for a variety of driver applications and is compatible with Metro MSA standards.

The 4953 consists of two high performance wideband amplifiers combined with off chip circuitry assembled in a surface mount package. A single 4953 placed between the MUX and Optical Modulator provides OEMs with a board level modulator driver surface mount solution.

The 4953 provides Metro and Long Haul designers with system critical features such as: low power dissipation (1.1W at Vo = 6V), very low rail ripple, high voltage drive capability at 5V bias (6 V amplitude adjustable to 3 V), low output jitter (1ps rms typical), and low input drive sensitivity (250mV at Vo = 6V).

The 4953 requires external DC blocks, a low frequency choke, and control circuitry.

The TGA4953-SCC-SL is available on an evaluation board.

RoHS compliant version available.

Measured Performance

TGA4953 Evaluation Board (Metro MSA Conditions)
10.7 Gb/s, V_D = 5 V, I_D = 210 mA, (Pdc = 1.1W)
V_{OUT} = 6 V_{PP}, CPC = 50%, V_{IN} = 500 mV_{PP}
Scale: 2 V/div, 15 ps/div

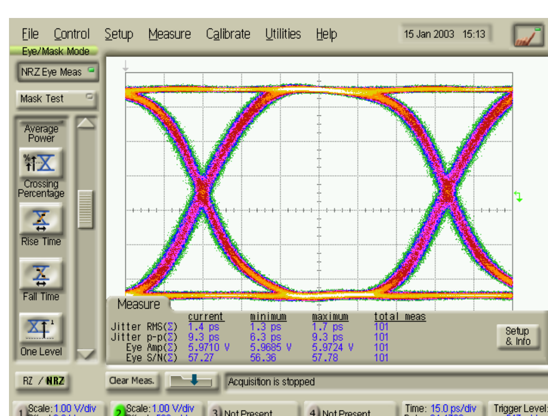


TABLE I
MAXIMUM RATINGS

Symbol	Parameter	Value	Notes
V_{D1} V_{D2T}	Drain Voltage	8 V	1/ 2/
V_{G1} V_{G2}	Gate Voltage Range	-3V to 0V	1/
V_{CTRL1} V_{CTRL2}	Control Voltage Range	-3V to V_D	1/
I_{D1} I_{D2T}	Drain Supply Current (Quiescent)	200 mA 350 mA	1/ 2/
$\lvert I_{G1} \rvert$ $\lvert I_{G2} \rvert$	Gate Supply Current	15 mA	1/
$\lvert I_{CTRL1} \rvert$ $\lvert I_{CTRL2} \rvert$	Control Supply Current	15 mA	1/ 5/
P_{IN}	Input Continuous Wave Power	23 dBm	1/ 2/
V_{IN}	12.5Gb/s PRBS Input Voltage	4 V_{PP}	1/ 2/
P_D	Power Dissipation	4 W	1/ 2/ 3/
T_{CH}	Operating Channel Temperature	150 ^{0}C	4/
T_M	Mounting Temperature (10 Seconds)	230 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings represent the maximum operable values for this device

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D at a package base temperature of 80°C

3/ When operated at this bias condition with a baseplate temperature of 80°C, the MTTF is reduced

4/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

5/ Assure V_{CTRL1} never exceeds V_{D1}, and V_{CTRL2} never exceeds V_{D2} during bias up and down sequences.

TABLE II
THERMAL INFORMATION

Parameter	Test Conditions	T_{CH} (°C)	$R_{\Theta JC}$ (°C/W)	MTTF (hrs)
$R_{\Theta JC}$ Thermal Resistance (Channel to Backside of Package)	V_{D2T} = 4.7V I_{D2T} = 150mA P_{DISS} = 0.71W T_{BASE} = 80°C	98	26	>1E6

Note: Thermal transfer is conducted through the bottom of the TGA4953-SCC-SL package into the motherboard. The motherboard must be designed to assure adequate thermal transfer to the base plate.

TABLE III
RF CHARACTERIZATION TABLE
(T_A = 25°C, Nominal)

Parameter	Test Conditions	Min	Typ	Max	Units	Notes
Small Signal Bandwidth			8		GHz	
Saturated Power Bandwidth			12		GHz	
Small Signal Gain	0.1, 2, 4 GHz 6 GHz 10 GHz 14 GHz 16 GHz	30 28 26 19 14			dB	1/ 2/
Input Return Loss	0.1, 2, 4, 6, 10, 14, 16 GHz	10	15		dB	1/ 2/
Output Return Loss	0.1, 2, 4, 6, 10, 14, 16 GHz	10	15		dB	1/ 2/
Noise Figure	3 GHz		2.5		dB	
Small Signal AGC Range	Midband		30		dB	
Saturated Output Power	2, 4, 6, 8 & 10 GHz	25			dBm	6/ 7/

TABLE III
RF CHARACTERIZATION TABLE
(T_A = 25°C, Nominal)

Parameter	Test Conditions	Min	Typ	Max	Units	Notes
Eye Amplitude	V_{D2T} = 8.0V V_{D2T} = 6.5V V_{D2T} = 5.5V V_{D2T} = 4.5V V_{D2T} = 4.0V	10 8.0 7.0 6.0 5.5			V_{PP}	3/ 4/
Additive Jitter (RMS)	V_{IN} = 500mV_{PP} V_{IN} = 800mV_{PP}		0.9 1.0	2.0 2.0	Ps	5/
Q-Factor	V_{IN} = 250mV_{PP} V_{IN} = 500mV_{PP} V_{IN} = 800mV_{PP}	26.5 28.5 28.5	32 35 35		V/V	
Delta Crossing Percentage	250mV_{PP} 800mV_{PP}			6.0 6.0	%	
Delta Eye Amplitude	250mV_{PP} 800mV_{PP}			0.45 0.10	V_{PP}	

Table III Notes:

1/ Verified at package level RF test

2/ Package RF Test Bias: V_D = 5V, adjust V_{G1} to achieve I_D = 65mA then adjust V_{G2} to achieve I_D = 200mA, V_{CTRL1} = -0.2V & V_{CTRL2} = +0.2 V

3/ Verified by design, SMT assembled onto a demonstration board detailed on sheet 6.

4/ V_{IN} = 250mV, Data Rate = 10.7Gb/s, V_{D1} = V_{D2T} or greater, V_{CTRL2} and V_{G2} are adjusted for maximum output

5/ Computed using RSS Method where $J_{RMS\_DUT} = \sqrt{(J_{RMS\_TOTAL}^2 - J_{RMS\_SOURCE}^2)}$

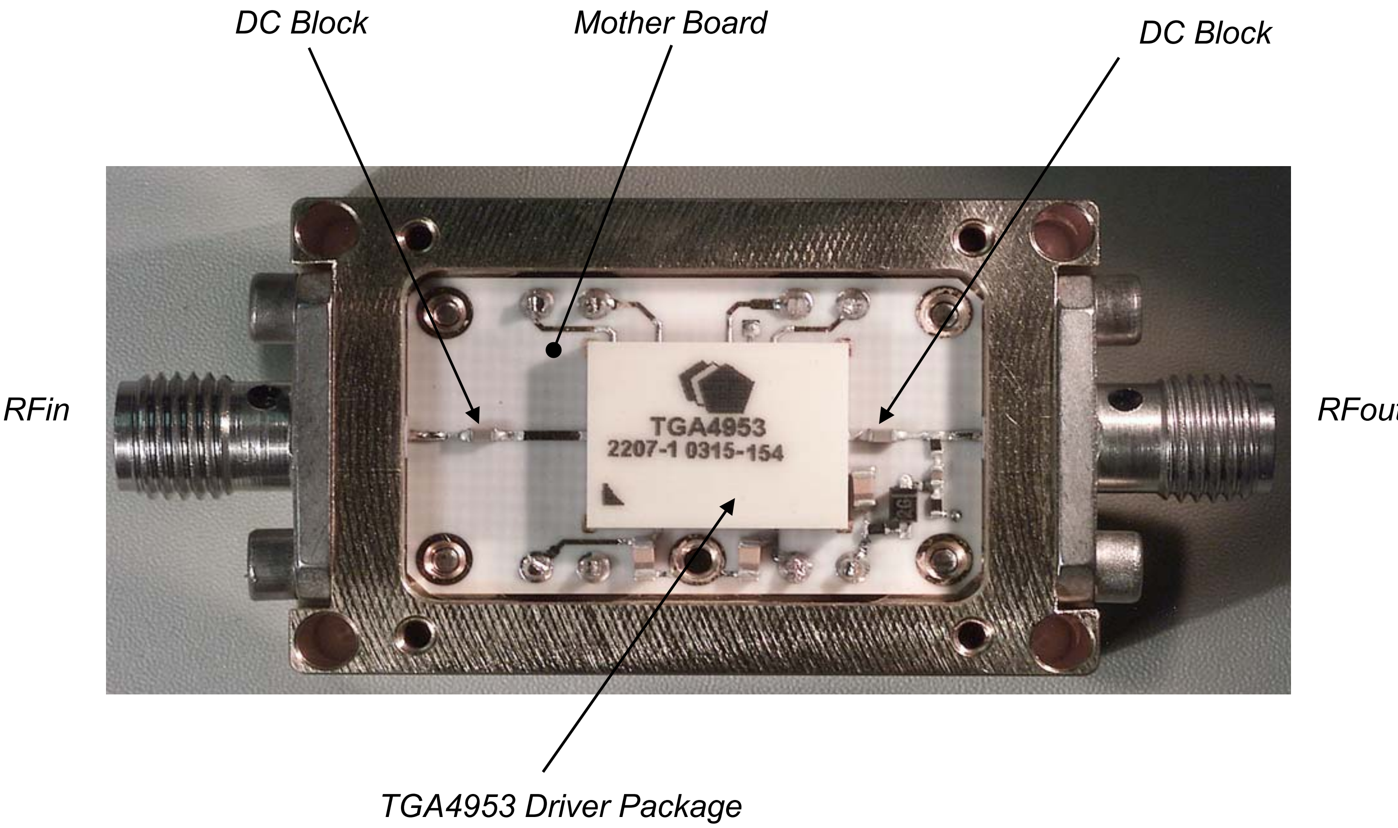
6/ Verified at die level on-wafer probe

7/ Power Bias Die Probe: V_{TEE} = 8V, adjust V_G to achieve I_D = 175mA ±5%, V_{CTRL} = +1.5V

8/ Value is the difference with the 500mV input measurement. Result is the absolute value.

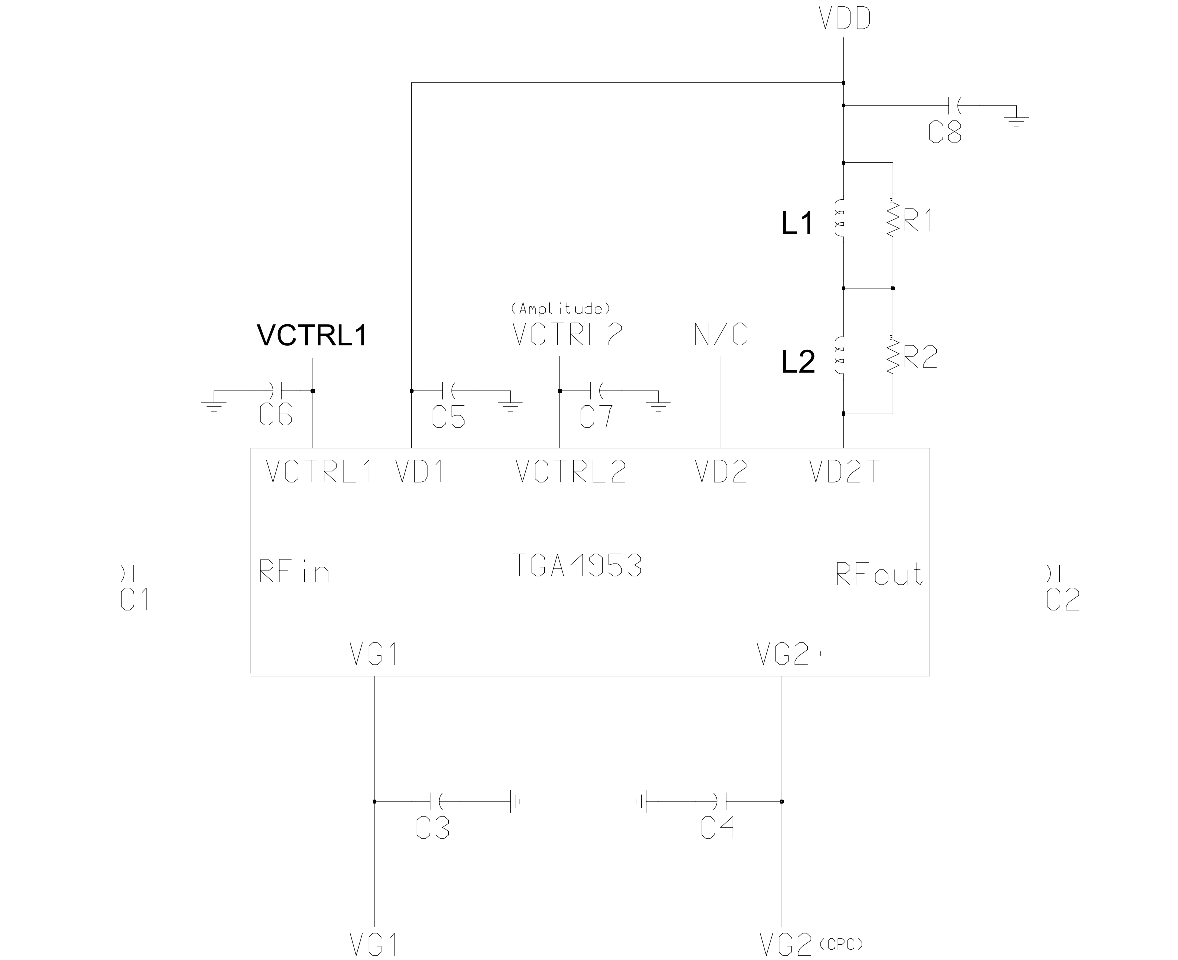
Note: At the die level, drain bias is applied through the RF output port using a bias tee, voltage is at the DC input to the bias tee

Demonstration Board



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

Demonstration Board Application Circuit



Notes:

1. C3 and C4 extend low frequency performance thru 30 KHz. For applications requiring low frequency performance thru 100 KHz, C3 and C4 may be omitted

2. C5 is a power supply decoupling capacitor and may be omitted

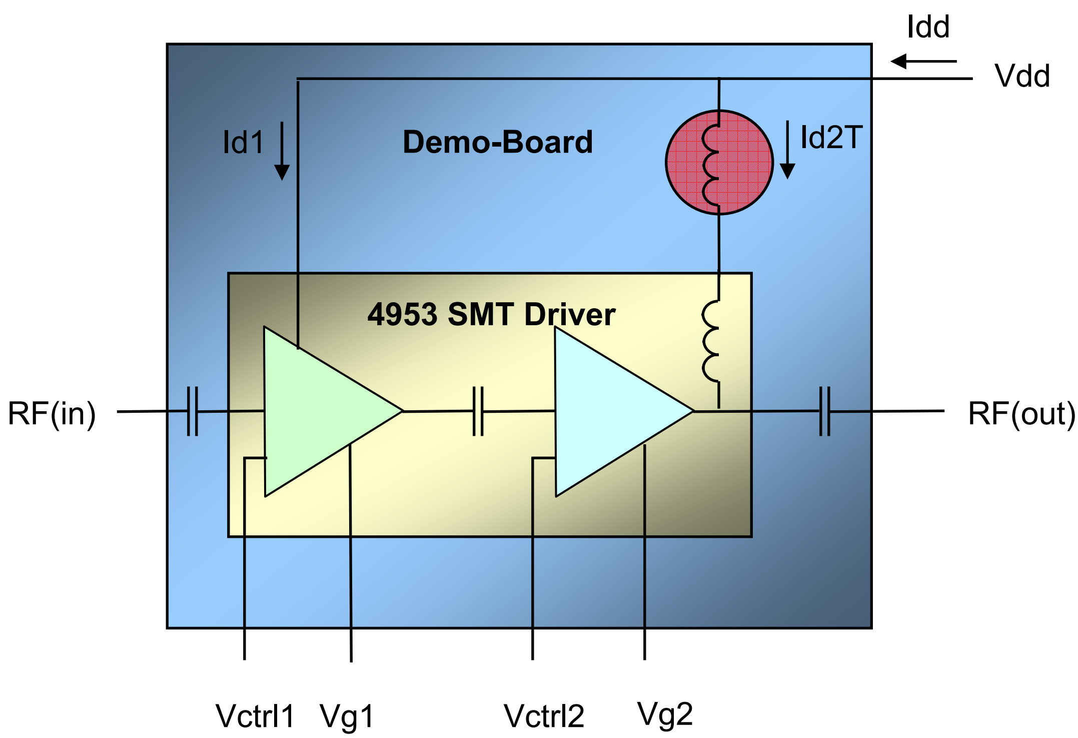
3. C6 and C7 are power supply decoupling capacitors and may be omitted when driven directly with an op-amp. Impedance looking into VCTRL1 and VCTRL2 is 10kΩ real

Demonstration Board Application Circuit
(Continued)

Recommended Components:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2	DC Block, Broadband	Presidio	BB0502X7R104M16VNT9820
C3, C4, C5	10uF Capacitor MLC Ceramic	AVX	0805YC106KA
C6, C7	0.01 uFCapacitor MLC Ceramic	AVX	0603YC103KA
C8	10 uF Capacitor Tantalum	AVX	TAJT106K016
L1	220 uH Inductor	Belfuse	S581-4000-14
L2	330 nH Inductor	Panasonic	ELJFA331M
R1, R2	274 Ω Resistor	Panasonic	ERJ2RKD274

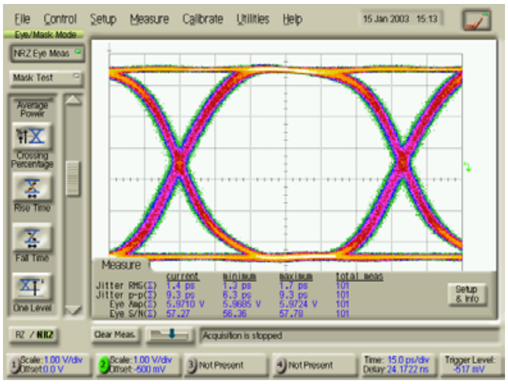
TGA4953 Typical Performance Data Measured on a Demonstration Board



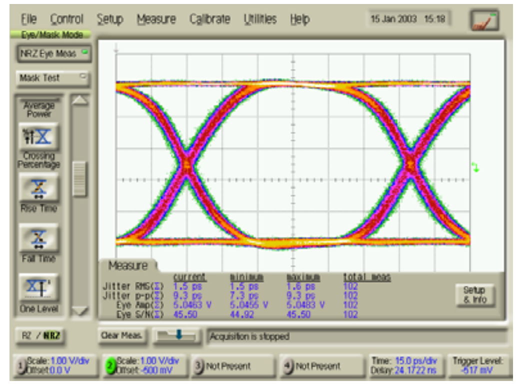
Demonstration Board Block Diagram

Typical Measured Performance on Demonstration Board
10.7Gb/s 2^31-1, Vdd=5V
CPC=50%

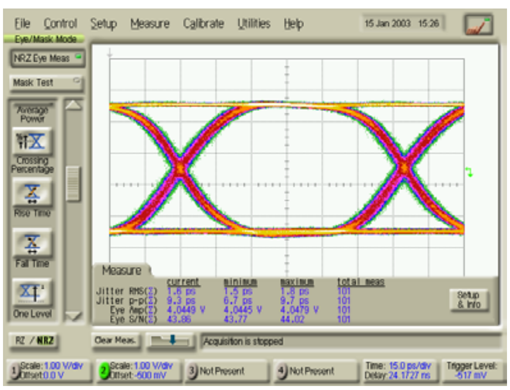
Vo=6V



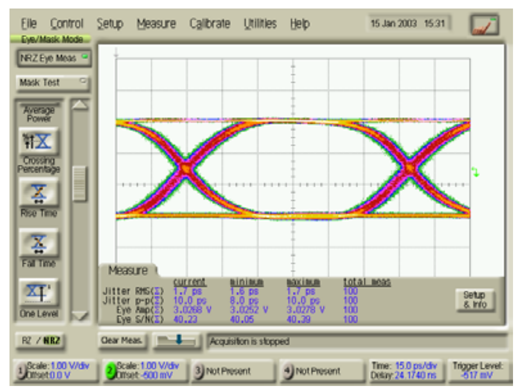
Vo=5V



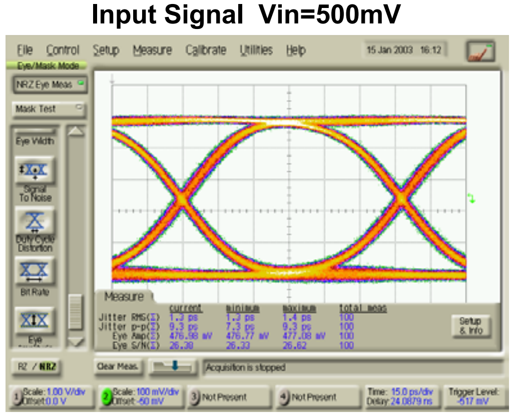
Vo=4V



Vo=3V

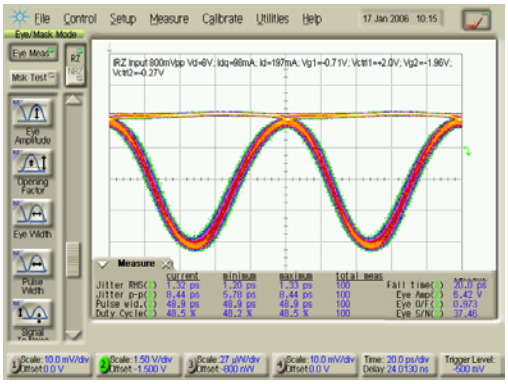


Input Signal Vin=500mV

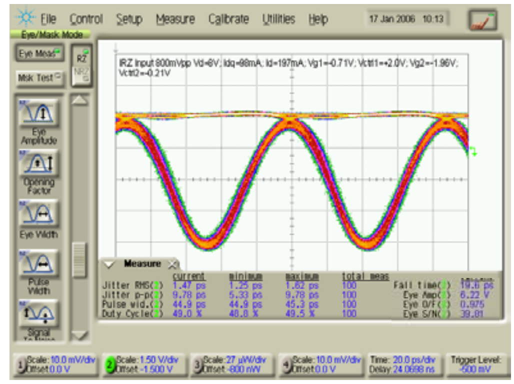


Typical Measured Performance on Demonstration Board
IRZ 2^31-1, Vdd=8V
Vin=800mVpp

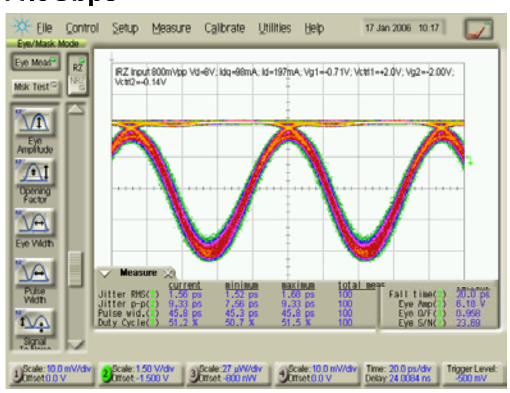
9.953Gbps



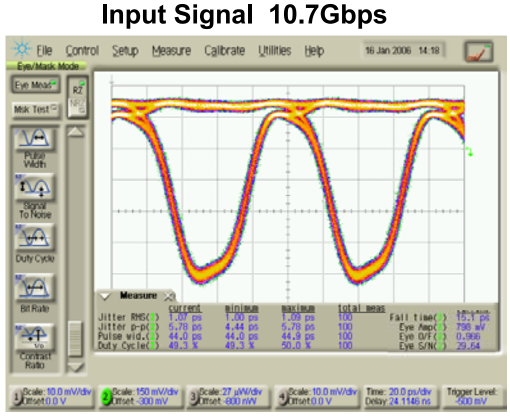
10.7Gbps



11.3Gbps

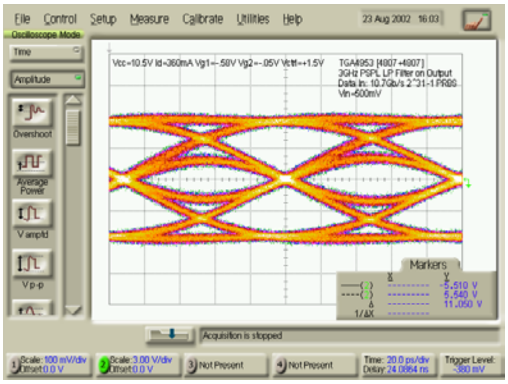


Input Signal 10.7Gbps

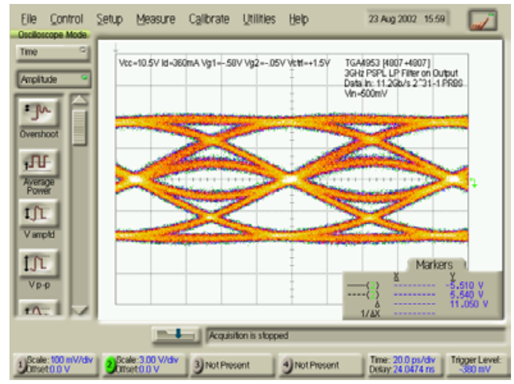


Typical Measured Performance on Demonstration Board
Duobinary 2^31-1, Vdd=10.5V
Vin=800mVpp

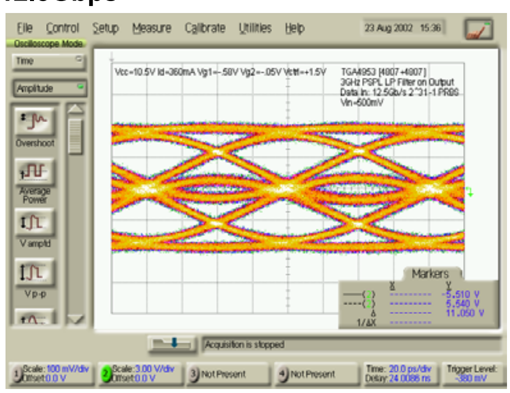
10.7Gbps



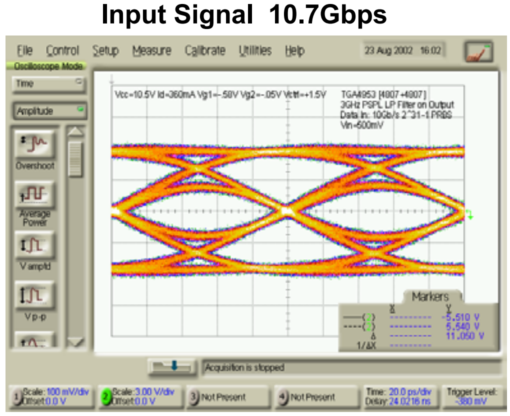
11.2Gbps



12.5Gbps



Input Signal 10.7Gbps



Typical Bias Conditions
Vdd=5V

Vo(V)	Vg1(V)	Vg2(V)	Id	Vctrl2
6	-0.66	-0.57	221	+0.22
5	-0.66	-0.59	198	+0.04
4	-0.66	-0.67	172	-0.14
3	-0.66	-0.74	147	-0.34

Notes:
1. Vdd=5V, Id1=65mA, and Vctrl1=-0.2V
2. Vin=500mVpp
3. 50%CPC
4. Actual bias points may be different.

Demonstration Board - Bias ON/OFF Procedure
Vdd=5V, Vo=6Vamp, CPC=50%
(Hot Pluggable)

Bias ON

1. Disable the output of the PPG
2. Set Vd=0V Vctrl1=0V Vctrl2=0 Vg1=0V and Vg2=0V
3. Set Vg1=-1.5V Vg2=-1.5V **Vctrl1=-0.2V**
4. Increase Vd to 5V observing Id.
   - Assure Id=0mA
5. Set Vctrl2=+0.2V
   - Id should still be 0mA
6. Make Vg1 more positive until **Idd=65mA**.
   - This is Id1 (current into the first stage)
   - Typical value for **Vg1 is -0.65V**
7. Make Vg2 more positive until Idd=220mA.
   - This sets Id2T to 155mA.
   - Typical value for Vg2 is -0.55V
8. Enable the output of the PPG.
   - Set Vin=500mV
9. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl slightly negative to decrease the output swing.
   - Typical value for **Vctrl2 is +0.22V** for Vo=6V.
10. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.
   - Typical value for **Vg2 is -0.57V** to center crossover with Vo=6V.

Bias OFF

1. Disable the output of the PPG
2. Set Vctrl2=0V
3. Set Vd=0V
4. Set Vctrl1=0V
5. Set Vg2=0V
6. Set Vg1=0V

Production - Initial Alignment - Bias Procedure

Vdd=5V, Vo=6Vamp, CPC=50%

(Hot Pluggable)

Bias Network Initial Conditions -

Vg1=-1.5V
Vg2=-1.5V
Vctrl1=-0.2V
Vctrl2=+.1V
Vd=5V

Bias ON

1. Disable the output of MUX
2. Apply Vg1, Vg2, Vctrl1, Vctrl2, and Vd in any sequence.
   Note: If Vd is applied first Id could reach near 400mA.
3. Make Vg1 more positive until **Idd=65mA**.
   - This is Id1 (current into the first stage)
   - Typical value for **Vg1 is -0.65V**
4. Make Vg2 more positive until Idd=220mA.
   - This sets Id2T to 155mA.
   - Typical value for Vg2 is -0.55V
5. Enable the output of the MUX.
   - Set Vin=500mV
6. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl2 slightly negative to decrease the output swing.
   - Typical value for **Vctrl2 is +0.22V** for Vo=6V.
7. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.
   - Typical value for **Vg2 is -0.57V** to center crossover with Vo=6V.

Bias OFF

Remove Vg1, Vg2, Vctrl1, Vctrl2, and Vd in any sequence.

Production - Post Alignment - Bias Procedure
Vdd=5V, Vo=6Vamp, CPC=50%
(Hot Pluggable)

Bias Network Initial Conditions -
Vg1= As found during initial alignment
Vg2=-As found during initial alignment
Vctrl1=-0.2V
Vctrl2=As found during initial alignment
Vd=5V

Bias ON
1. Mux output can be either Enabled or Disabled
2. Apply Vg1, Vg2, Vctrl1, Vctrl2, and Vd in any sequence.
   Note: If Vd is applied first Id could reach near 400mA.
3. Enable the output of the MUX
4. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl slightly negative to decrease the output swing.
5. Crossover Adjust: Adjust Vg2 slightly positive to push the crossover down or adjust Vg2 slightly negative to push the crossover up.

Bias OFF
Remove Vg1, Vg2, Vctrl1, Vctrl2, and Vd in any sequence.

Production - Initial Alignment – IRZ Bias Procedure

Vdd=8V, Vo=6Vamp

(Hot Pluggable)

Bias Network Initial Conditions -

Vg1=-1.5V
Vg2=-2.0V
Vctrl1=+1.0V
Vctrl2=+2.0V
Vd=8V

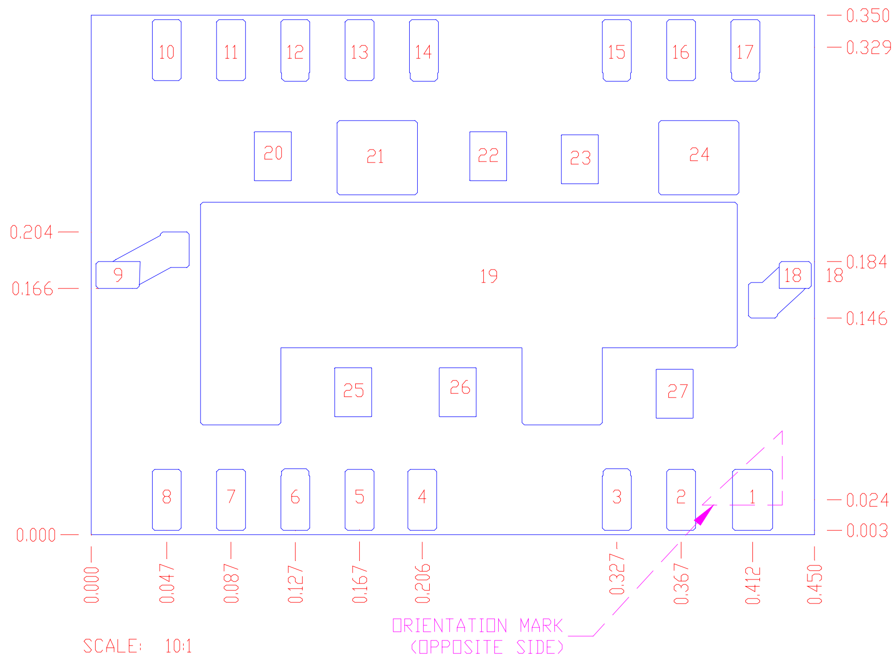
Bias ON

1. Disable the output of MUX
2. Apply Vg1, Vg2, Vctrl1, Vctrl2, and Vd in any sequence.
   Note: If Vd is applied first Id could reach near 400mA.
3. Make Vg1 more positive until **Idd=80mA**.
   - This is Id1 (current into the first stage)
   - Typical value for **Vg1 is -0.55V**
4. Enable the output of the MUX.
   - Set Vin=800mV
5. Crossover Adjust: Adjust Vg2 slightly negative to push the crossover towards zero level.
6. Output Swing Adjust: Adjust Vctrl2 slightly positive to increase output swing or adjust Vctrl2 slightly negative to decrease the output swing.
7. Duty Cycle Fine Tune: Adjust Vctrl1 slightly negative to reduce duty cycle percentage.
8. Readjust Vctrl2 for proper output amplitude.

Bias OFF

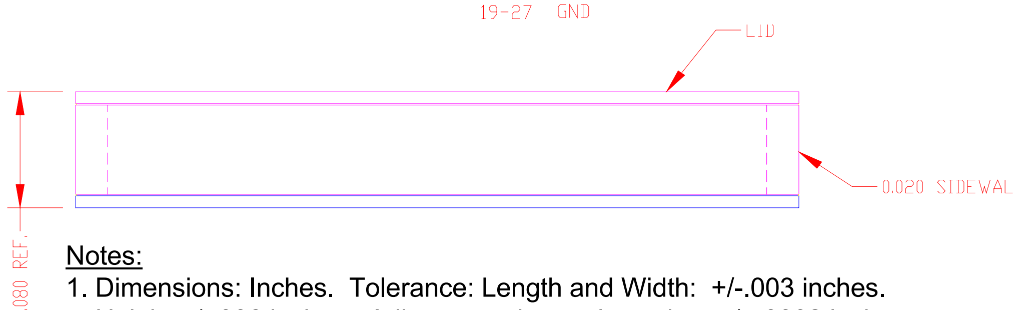
Remove Vg1, Vg2, Vctrl1, Vctrl2, and Vd in any sequence.

TGA4953 Mechanical Drawing



PIN	FUNCTION	PAD DIM (X, Y)
1	N/C	(0.025, 0.041)
2	N/C	(0.018, 0.041)
3	Vg1	(0.018, 0.041)
4	N/C	(0.018, 0.041)
5	N/C	(0.018, 0.041)
6	Vg2	(0.018, 0.041)
7	N/C	(0.018, 0.041)
8	N/C	(0.018, 0.041)
9	RF OUT	(0.027, 0.018)

PIN	FUNCTION	PAD DIM (X, Y)
10	N/C	(0.018, 0.041)
11	N/C	(0.018, 0.041)
12	Vd2T	(0.018, 0.041)
13	Vd2	(0.018, 0.041)
14	Vctrl2	(0.018, 0.041)
15	Vd1	(0.018, 0.041)
16	N/C	(0.018, 0.041)
17	Vctrl1	(0.018, 0.041)
18	RF IN	(0.020, 0.018)
19-27	GND	



Notes:

1. Dimensions: Inches. Tolerance: Length and Width: +/-.003 inches. Height +/-.006 inches. Adjacent pad to pad spacing: +/- .0002 inches. Pad Size: +/- .001 inches.
2. Surface Mount Interface:
   Material: RO4003 (thickness=.008 inches), 1/2oz copper (thickness=.0007 inches)
   Plating Finish: 100-350 microinches nickel underplate, with 5-10 microinches flash gold overplate.

Recommended Surface Mount Package Assembly

Proper ESD precautions must be followed while handling packages.

Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.

TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.

Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance. *This package has little tendency to self-align during reflow*.

Clean the assembly with alcohol.

Typical Solder Reflow Profiles

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

Ordering Information

Part	Package Style
TGA4953-SCC-SL	Land Grid Array Surface Mount
TGA4953-SL,RoHS	Land Grid Array Surface Mount (RoHS Compliant)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.