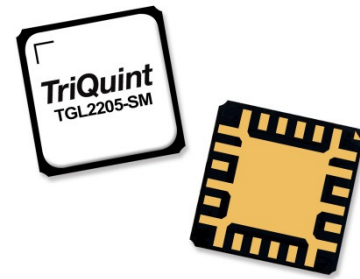


Applications

- Receive Chain Protection
- Commercial and Military Radar

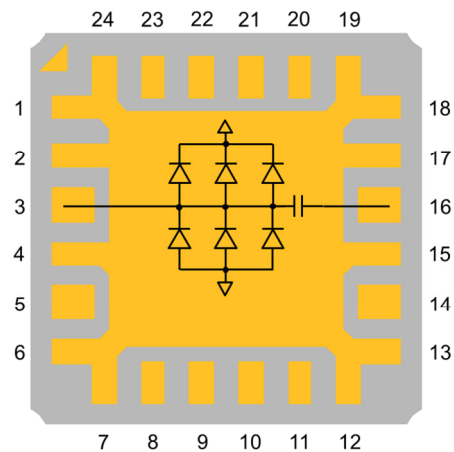


4 mm x 4 mm QFN Package

Product Features

- Frequency Range: 2 to 6 GHz
- Insertion Loss: < 0.6 dB
- Peak Power Handling: 100 W (pulsed)
- Flat Leakage: < 16.5 dBm
- Passive (no DC bias required)
- Integrated DC Block on output
- Spike Leakage < 0.5 dB
- Recovery time < 115 ns
- Package Dimensions: 4.0 mm x 4.0 mm x 1.47 mm

Functional Block Diagram



General Description

The TriQuint TGL2205-SM is a high power, wideband GaAs VPIN limiter capable of protecting sensitive receive channel components against high power incident signals. The TGL2205-SM does not require DC bias and achieves a low insertion loss all in a small form factor. These features allow for simple integration with minimal impact to system performance.

The TGL2205-SM operates from 2 to 6 GHz with low insertion loss of less than 0.6 dB. It can limit up to 100 W incident pulsed-power with a low flat leakage of less than 16.5 dBm.

The TGL2205-SM die has a protective surface passivation layer that provides enhanced environmental robustness. It is well suited for both commercial and defense related applications.

Lead-free and RoHS compliant.

Pad Configuration

Pad Number	Symbol
3	RF Input
16	RF Output
1,2,4,6,7,12,13,15,17-19,24,25	GND
5,8-11,14,20-23	No connection

NOTE: the RF Input and Output ports are not interchangeable.

Ordering Information

Part	ECCN	Description
TGL2205-SM	EAR99	S and C-Band 100W VPIN Limiter

Absolute Maximum Ratings

Parameter	Value
Incident Power, CW or Pulsed, 50Ω, 25 °C	100W
Incident Power, CW or Pulsed, 50Ω, 85 °C	50W
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Passive – No bias	

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, Tuned EVB Results

Parameter	Min	Typical	Max	Units
Operational Frequency Range	2		6	GHz
Insertion Loss		< 0.6		dB
Input Return Loss		12		dB
Output Return Loss		12		dB
Flat Leakage Power at P _{IN} > 30 dBm		< 16.5		dBm
Pulse Recovery Time		< 115		ns
Spike Leakage		< 0.5		dB
Insertion Loss Temperature Coefficient		0.003		dB/°C

Thermal and Reliability Information

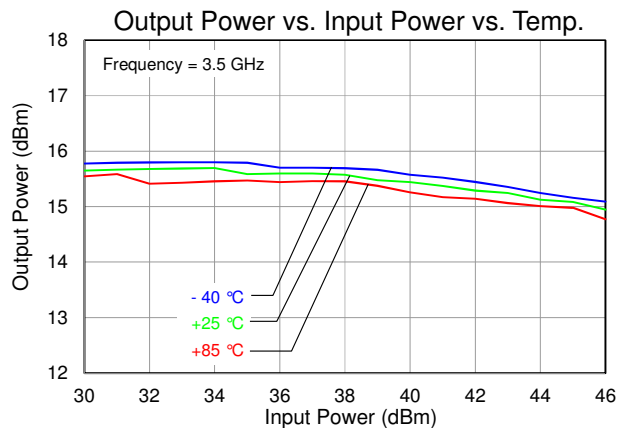
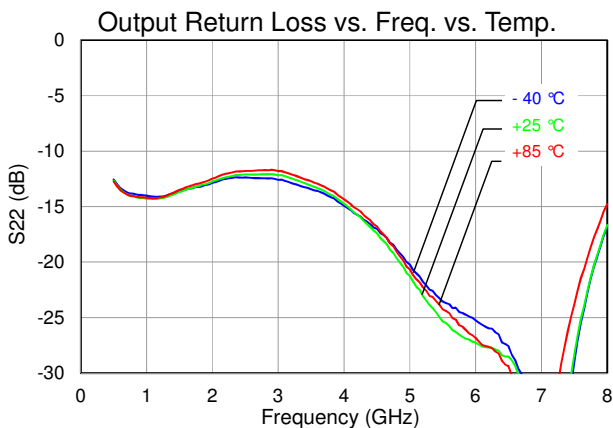
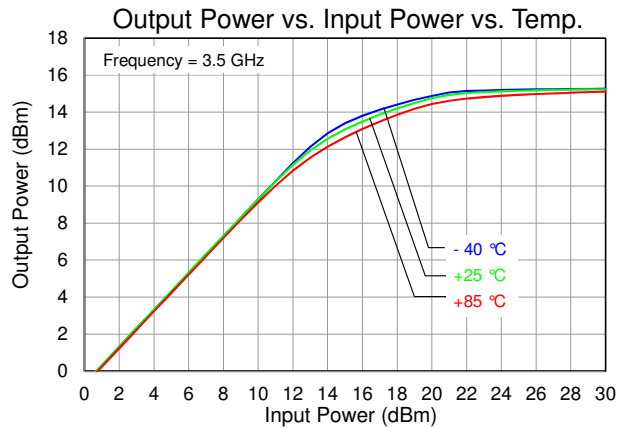
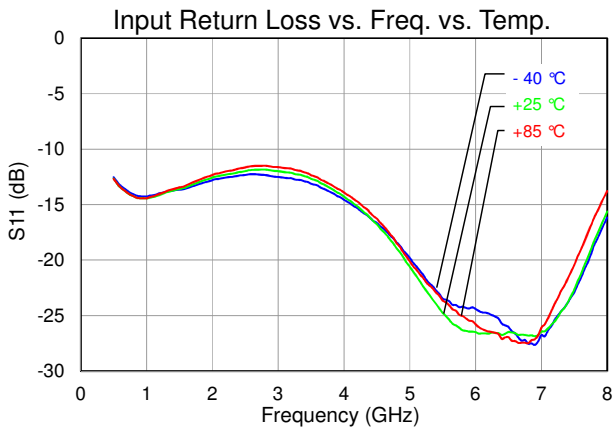
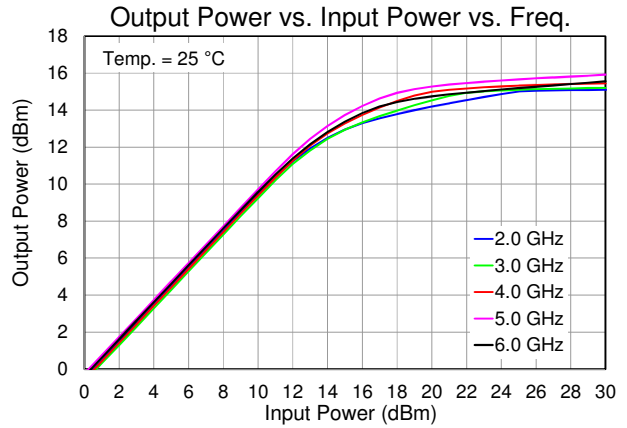
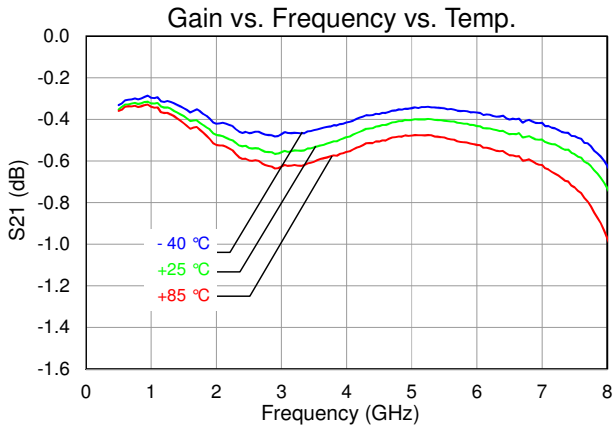
Parameter	Test Conditions	Value	Units
Incident Power (RF Operational Life Test 168 Hours ⁽¹⁾)	Frequency = 4.5 GHz, CW, 50Ω, 25 °C	31	W
	Frequency = 4.5 GHz, Pulsed, PW=10us, DC=10%, 50Ω, 25 °C	100	W

Notes:

1. Test was terminated at 168 hours. Insertion Loss remained ≤ 1 dB for device under test.

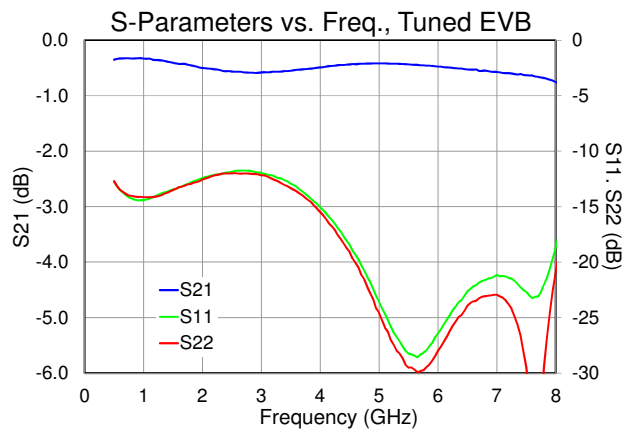
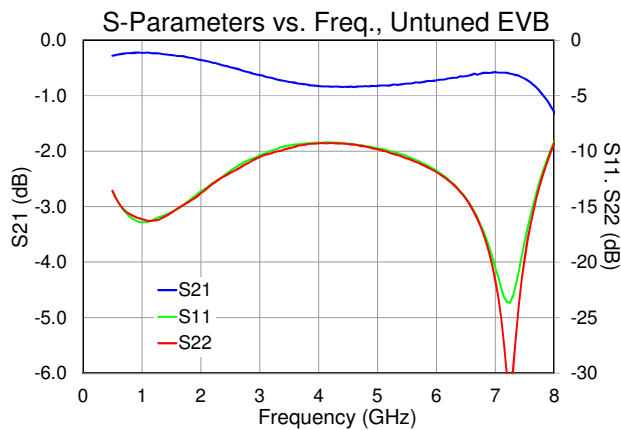
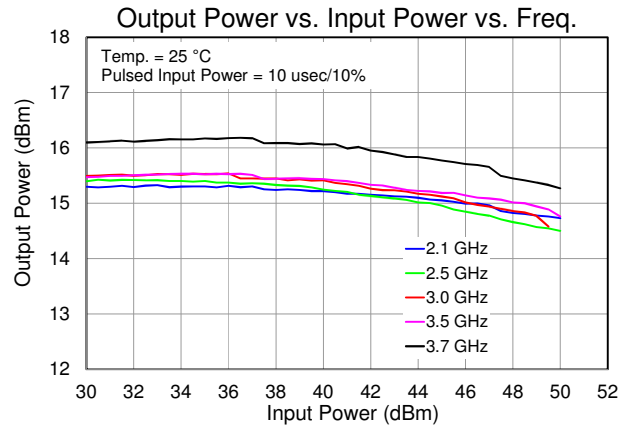
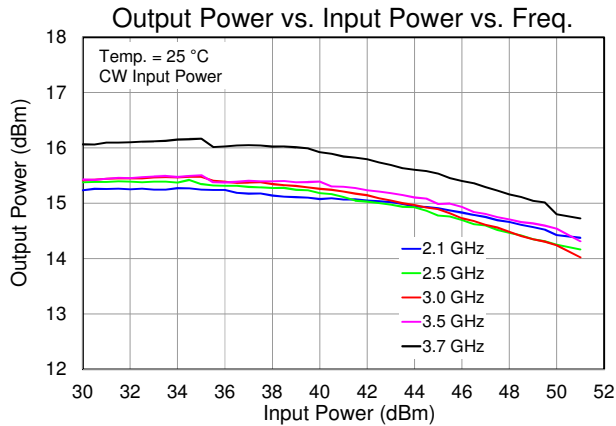
Typical Performance – Tuned EVB Performance

Test conditions unless otherwise noted: 25 °C

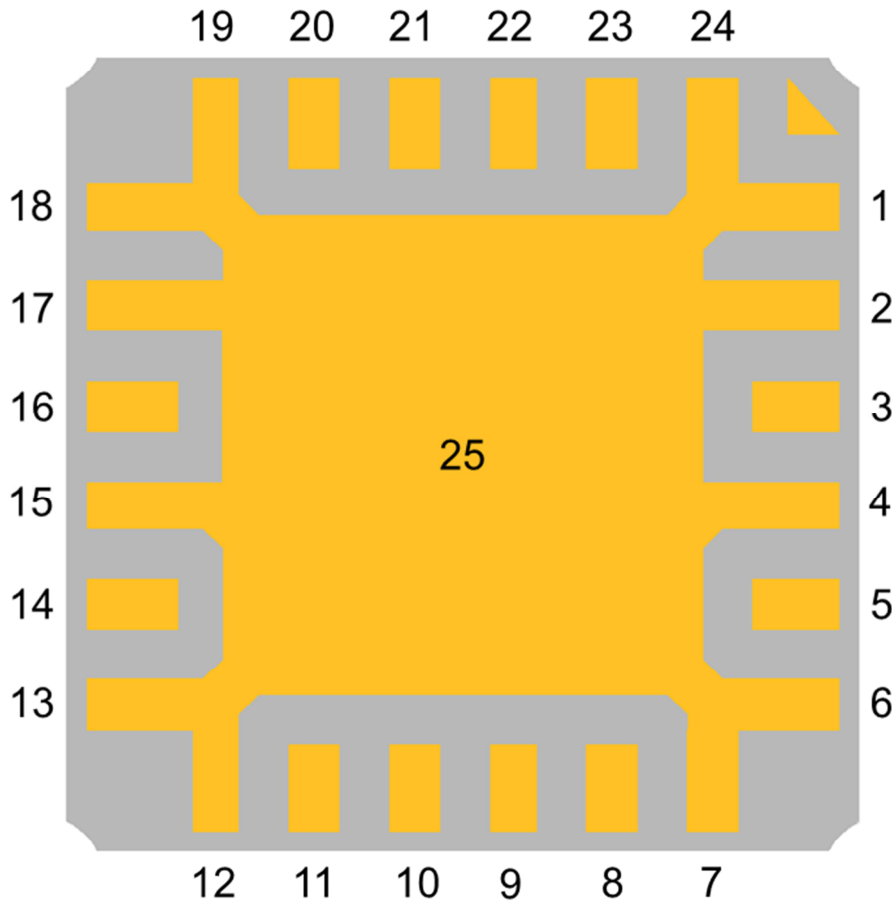


Typical Performance – Tuned EVB Performance

Test conditions unless otherwise noted: 25 °C



Pad Description



Bottom View

Package Pad	Symbol	Description
1,2,4,6,7,12,13,15,17-19,24,25	GND	On PCB, multiple vias should be employed under 25 (center pad) to minimize inductance and thermal resistance; see page 9 for suggested mounting configuration.
3	RF Input	Input, matched to 50 Ohms, not DC blocked
16	RF Output	Output, matched to 50 Ohms, DC blocked
5,8-11,14,20-23	NC	No connection

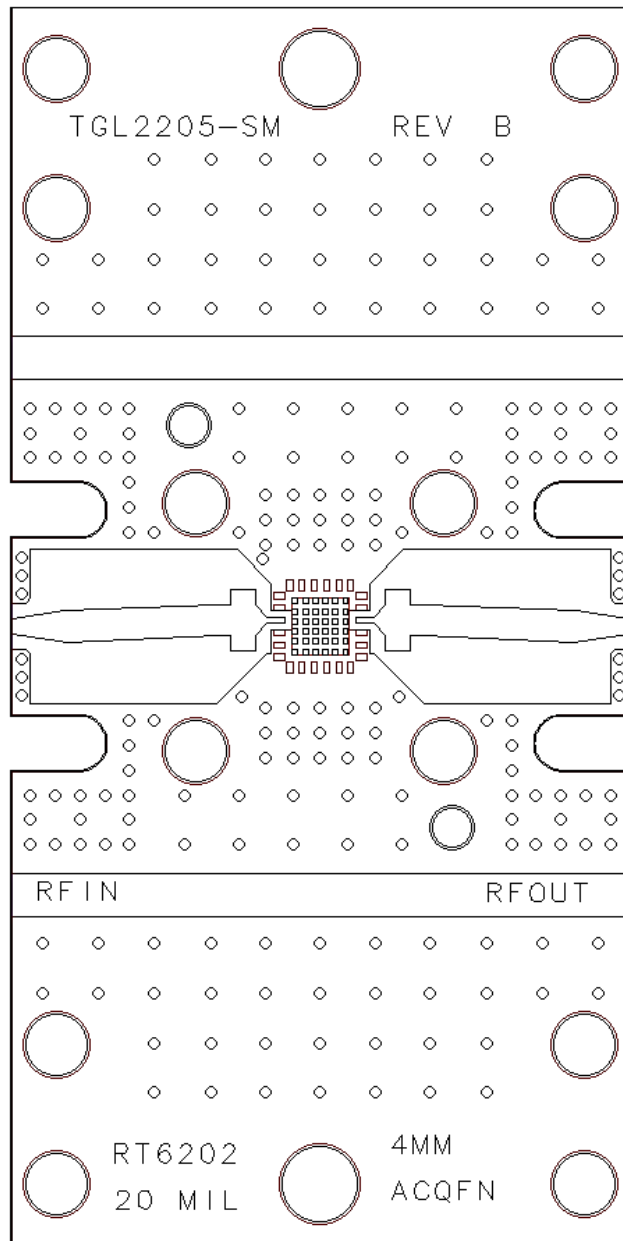
NOTE: The RF Input and Output ports are not interchangeable.

Applications Information

PC Board Layout

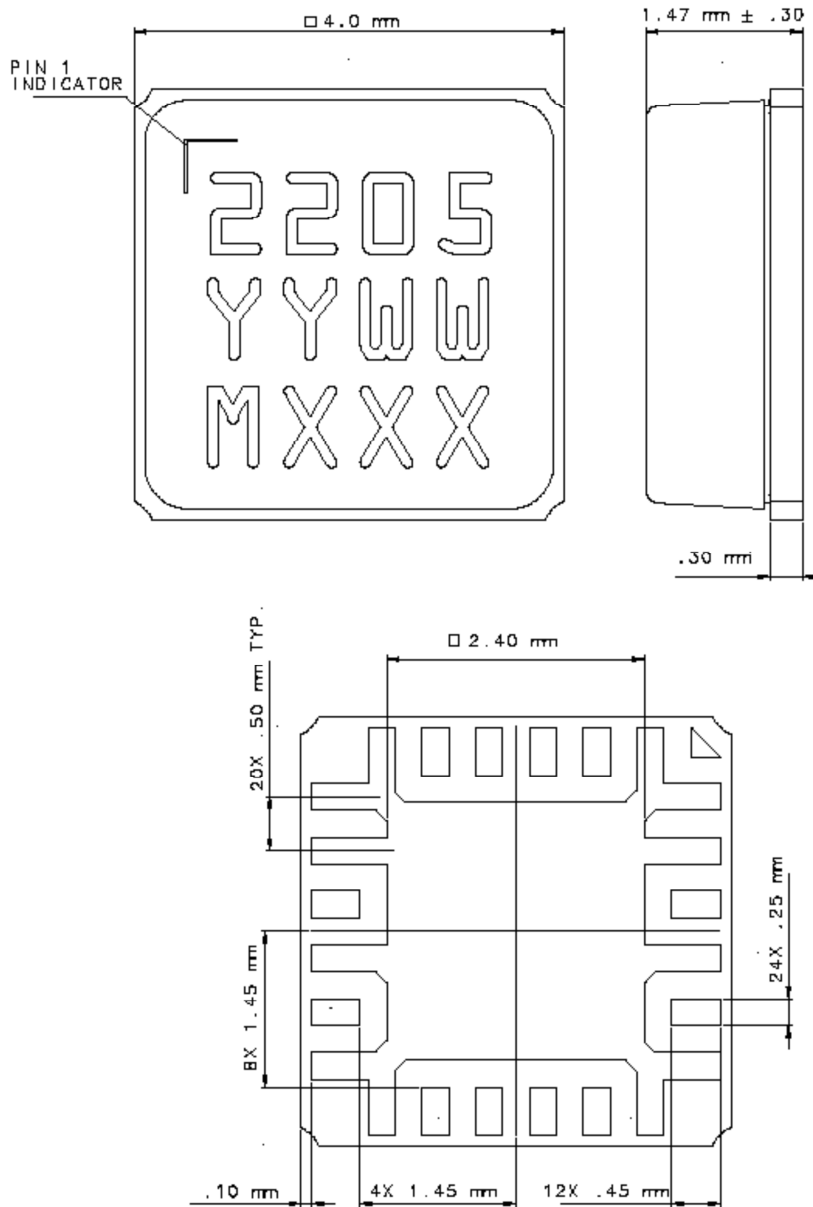
RF layer is 0.020" thick Rogers RO6020, $\epsilon_r=2.94$. Metal layers are 1-oz copper. Microstrip 50 Ω line width is 0.050". The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-02A-5.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



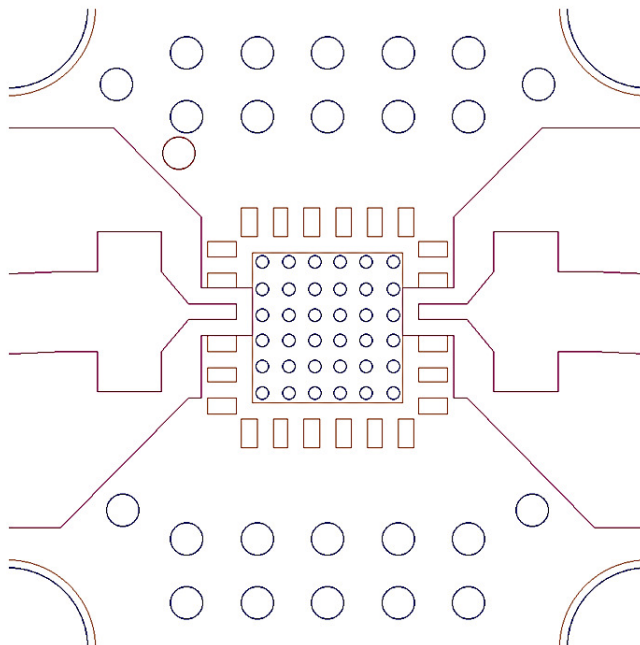
Mechanical Information

Package Information and Dimensions (Units: millimeters)



The TGL2205-SM will be marked with the “yyyy” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the year the part was manufactured, the “WW” is the work week, and the “XXXX” is an auto-generated number.

This package is lead-free/RoHS-compliant. The package base is Aluminum Nitride and the plating material on the leads is gold over nickel (Au-Ni). This package is compatible with both lead free and tin-lead soldering processes. The lid is plastic.

Mechanical Information (continued)**Mounting Configuration****Notes:**

1. Ground / thermal vias under the DUT are critical for the proper performance of this device.
2. The EVB shown herein utilizes copper filled vias (8 mil diameter) under the DUT to maximize heat transfer away from the DUT under large signal conditions.
3. Thermal dissipation is low for normal non-limiting operation.

Product Compliance Information**ESD Sensitivity Ratings**

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

TBD at 260 °C convection reflow
The part is rated Moisture Sensitivity Level TBD
JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260 °C.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

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