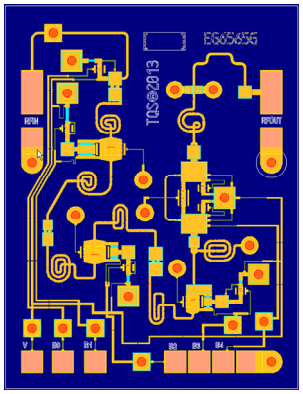
TGL2616

10-20 GHz 5-Bit Attenuator

Applications

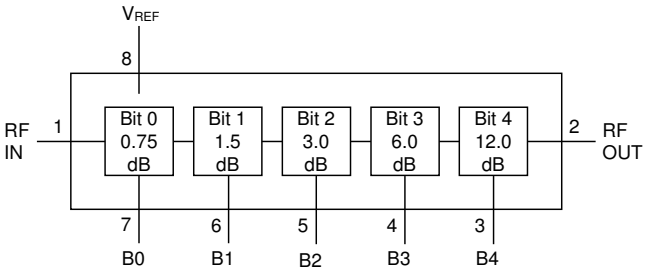
- Phased Array Antenna Systems
- Satellite Communication Systems
- Electronic Warfare



Product Features

- Frequency Range: 10-20 GHz
- 5-Bit Digital Attenuator
- Attenuation Range: 23.25 dB
- Attenuation Step Size (LSB): 0.75 dB
- Insertion Loss (Ref. State): 4.2 dB
- RMS Amplitude Error: < 0.6 dB
- RMS Step Error: < 0.2 dB
- Control Voltage: 3.3-5.0 V
- Positive logic
- Die Size: 1.340 x 1.760 x 0.10 mm

Functional Block Diagram



General Description

The TriQuint TGL2616 is a 5-bit digital attenuator MMIC design using TriQuint's TQPHT15 0.15 um GaAs pHEMT process. The TGL2616 is ideally suited for a variety of wideband phased array applications, including commercial and military radars, satellite-based communication systems and electronic warfare.

The TGL2616 provides a 5-bit digital attenuator function with a nominal 4.2 dB insertion loss and RMS attenuation error of better than 0.6 dB over a bandwidth of 10-20 GHz.

The TGL2616 operates with a control and reference voltage of 3.3 to 5 V. Each device is RF tested on-wafer to ensure performance compliance. The device is available in die form.

Lead-free and RoHS compliant.

Evaluation Boards available on request.

Pad Configuration

Pad Number	Symbol
1	RF Input
2	RF Output
3	B4 (12 dB bit)
4	B3 (6 dB bit)
5	B2 (3 dB bit)
6	B1 (1.5 dB bit)
7	B0 (0.75 dB bit)
8	V_{REF}

Ordering Information

Part	ECCN	Description
TGL2616	EAR99	10-20 GHz 5-Bit Digital Attenuator

Absolute Maximum Ratings

Parameter	Value
Control Voltage (V_C)	6 V
Control Current (I_C)	1 mA
Input Power (P_{IN})	35 dBm
Power Dissipation (P_{DISS})	0.9 W
Operating Channel Temperature	150 °C
Mounting Temperature (30 sec.)	320 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Reference Voltage[1]	3.3-5 V
Control Voltage (logic L / H)[1]	0 / 3.3-5 V

Note:

1. $V_{REF} \geq V_C$

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions, unless otherwise noted: 25 °C, V_{REF} = 3.3 V, V_C = 0 / 3.3 V, tested using assembly drawing on page 8

Parameter	Min	Typical	Max	Units
Frequency Range	10		20	GHz
LSB Attenuation		0.75		dB
Attenuation range		23.25		dB
Reference State Insertion Loss		4.2		dB
Input Return Loss		> 12		dB
Output Return Loss		> 17		dB
IIP3 (10 MHz spacing, P_{IN}/Tone=10 dBm, 15 GHz)		> 36		dBm
Switching Speed (90% to 10%)		< 10		ns
RMS Attenuation Error		< 0.6		dB
RMS Step Error		< 0.2		dB
Max. Attenuation Error		< 1.3		dB

Specifications

Thermal and Reliability Information

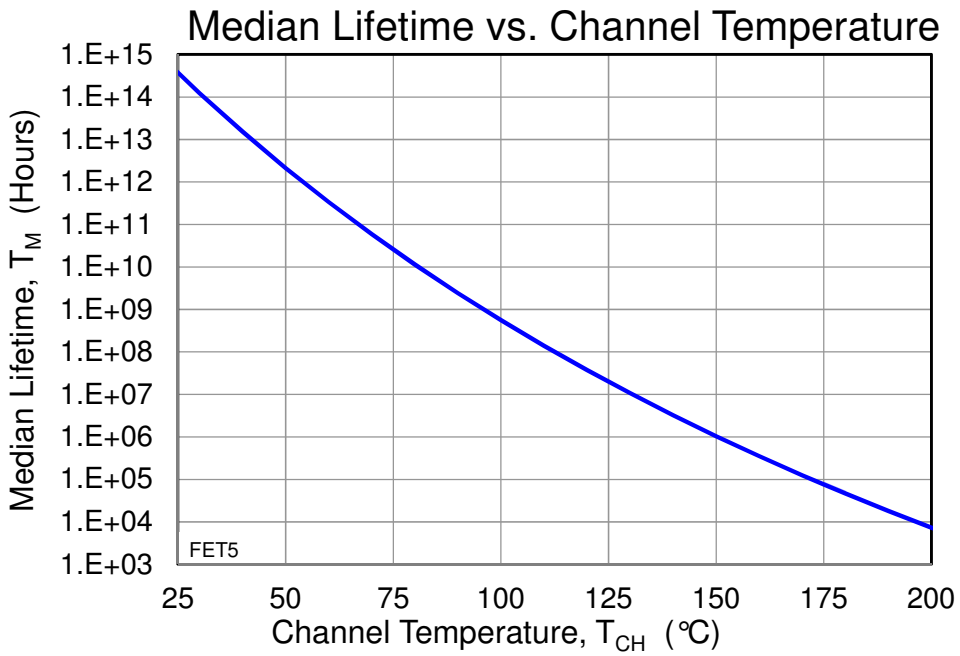
Parameter	Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_{REF} = 3.3 V, V_C = 3.3 V, P_{DISS} = 0.09 W	22	°C/W
Channel Temperature (T_{CH}) (1)		87	°C
Median Lifetime (T_M)		3.8E+09	Hrs

Note:

1. Die mounted to 40 mil Cu-Mo carrier plate using 1.5 mil Au-Sn solder, carrier plate backside temperature fixed at 85 °C.

Median Lifetime

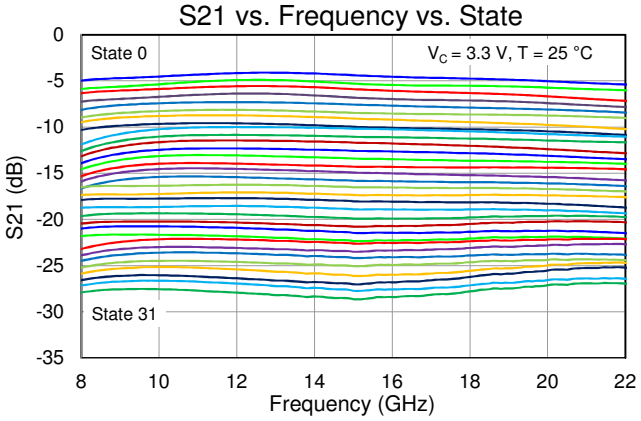
Test Conditions: 6.0 V; Failure Criterion = 10% reduction in $I_{D\ MAX}$



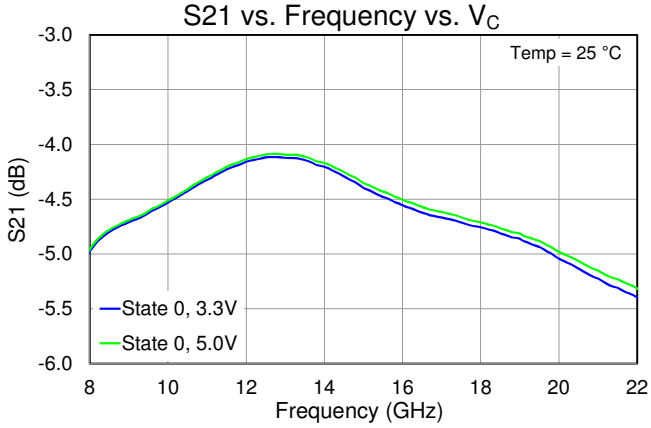
Typical Performance

Test conditions unless otherwise noted: Tested using assembly drawing on page 8.

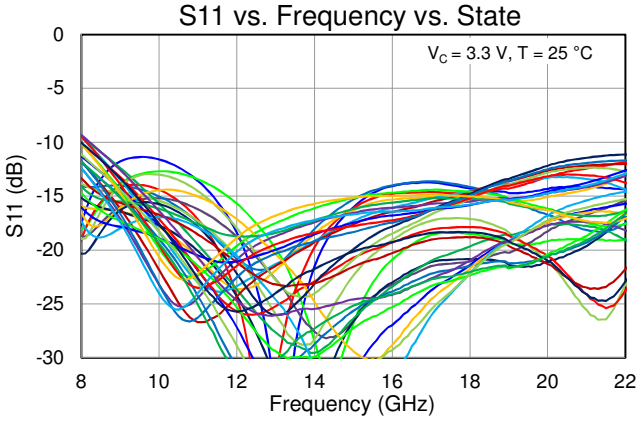
S21 vs. Frequency vs. State



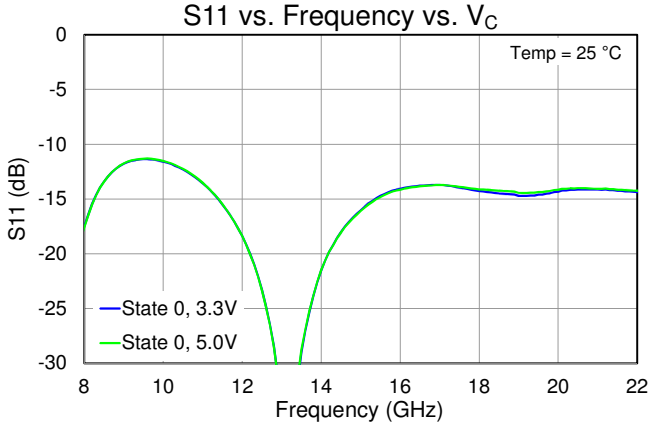
S21 vs. Frequency vs. V_C



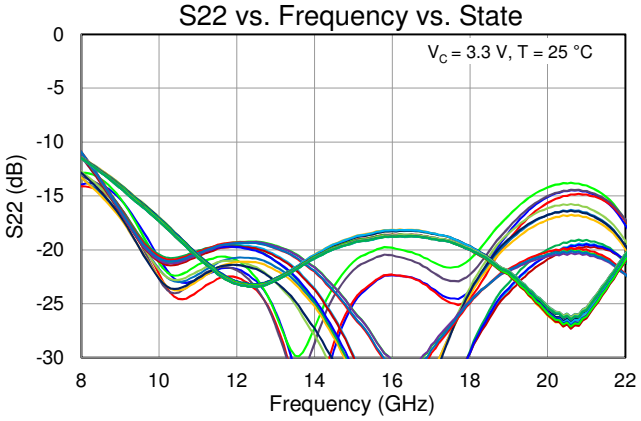
S11 vs. Frequency vs. State



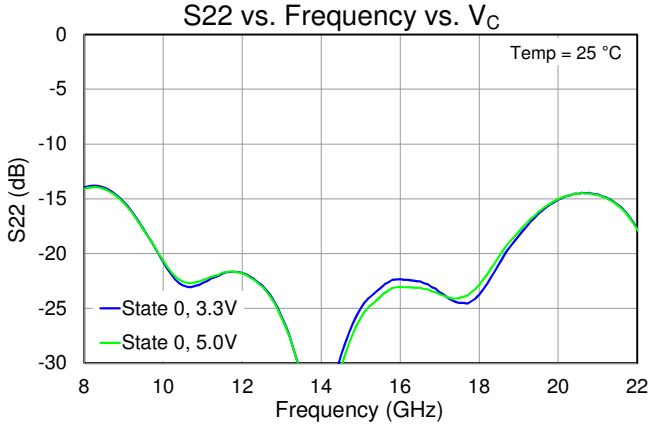
S11 vs. Frequency vs. V_C



S22 vs. Frequency vs. State



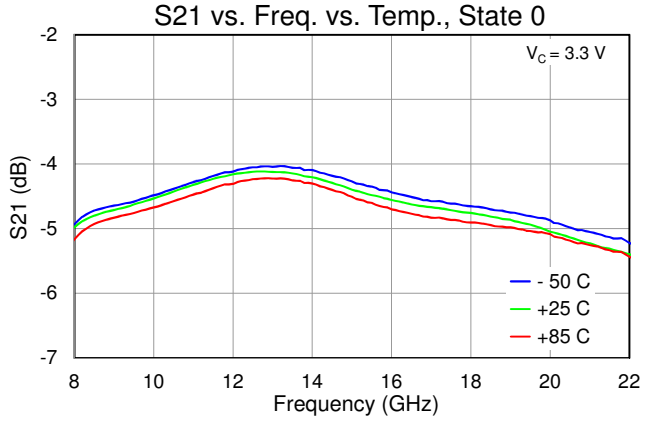
S22 vs. Frequency vs. V_C



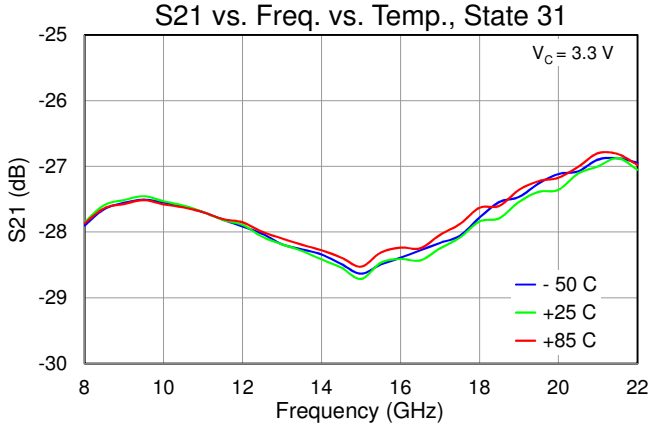
Typical Performance

Test conditions unless otherwise noted: Tested using assembly drawing on page 8.

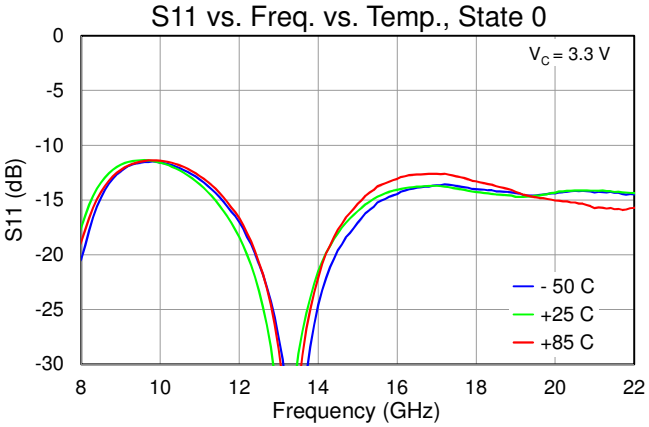
S21 vs. Freq. vs. Temp., State 0



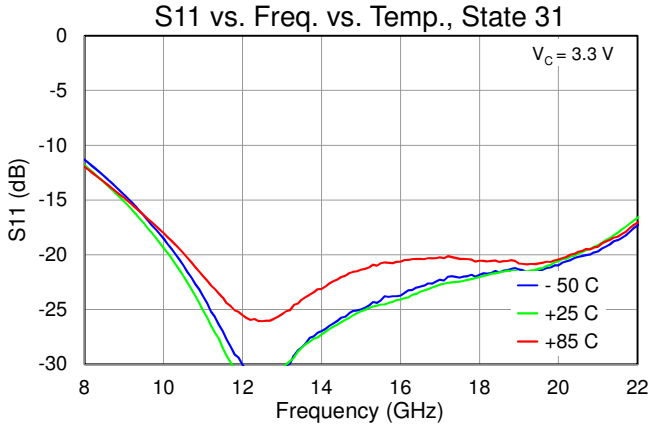
S21 vs. Freq. vs. Temp., State 31



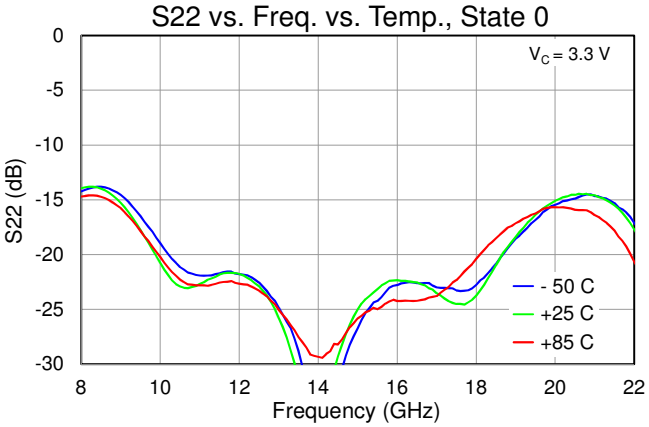
S11 vs. Freq. vs. Temp., State 0



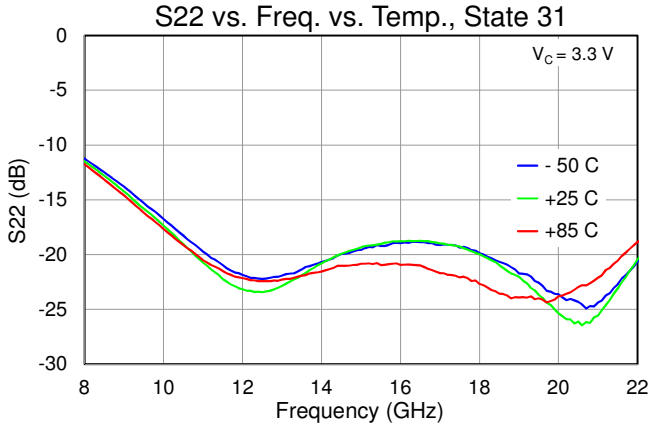
S11 vs. Freq. vs. Temp., State 31



S22 vs. Freq. vs. Temp., State 0



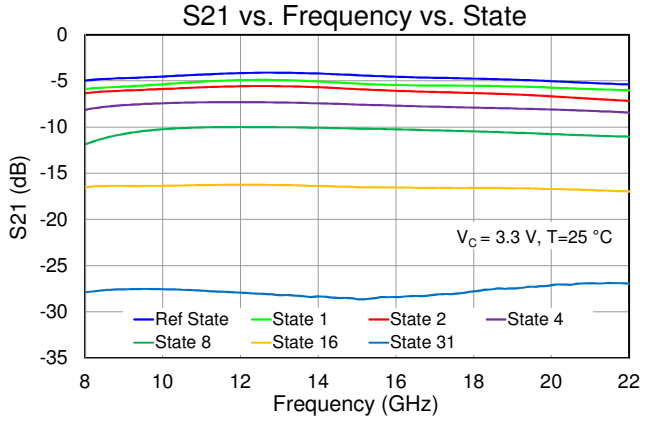
S22 vs. Freq. vs. Temp., State 31



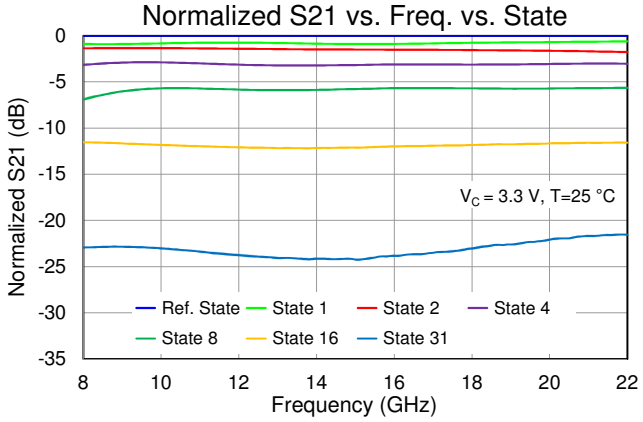
Typical Performance

Test conditions unless otherwise noted: Tested using assembly drawing on page 8.

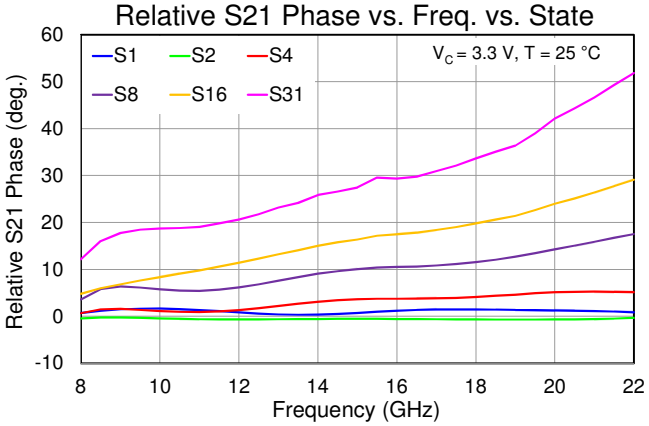
S21 vs. Frequency vs. State



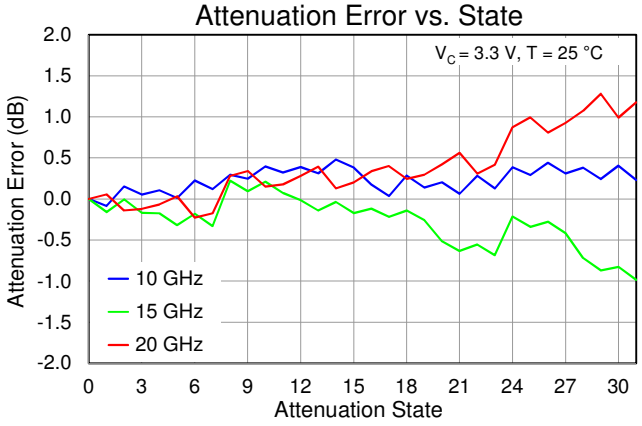
Normalized S21 vs. Freq. vs. State



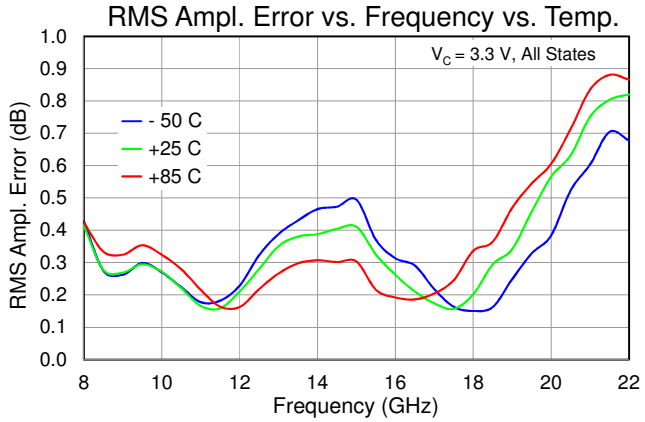
Relative S21 Phase vs. Freq. vs. State



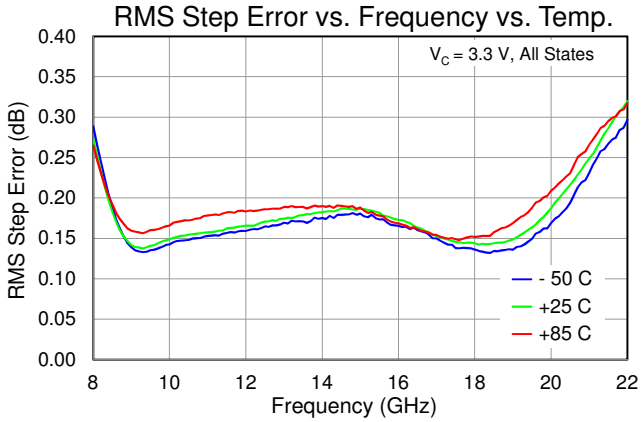
Attenuation Error vs. State



RMS Ampl. Error vs. Frequency vs. Temp.



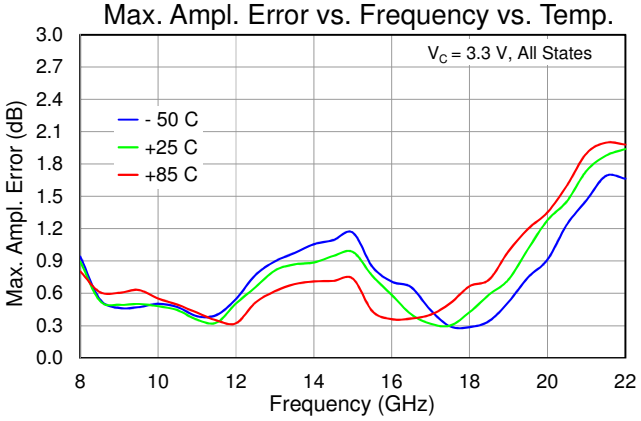
RMS Step Error vs. Frequency vs. Temp.



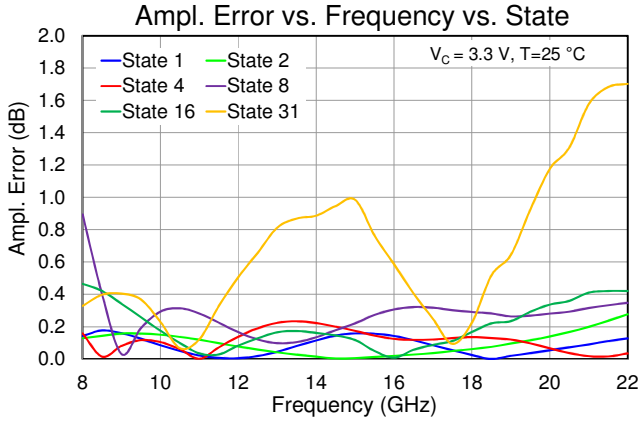
Typical Performance

Test conditions unless otherwise noted: Tested using assembly drawing on page 8.

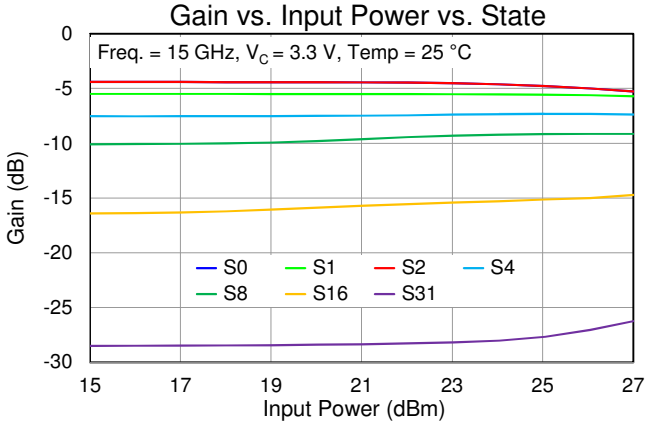
Max. Ampl. Error vs. Frequency vs. Temp.



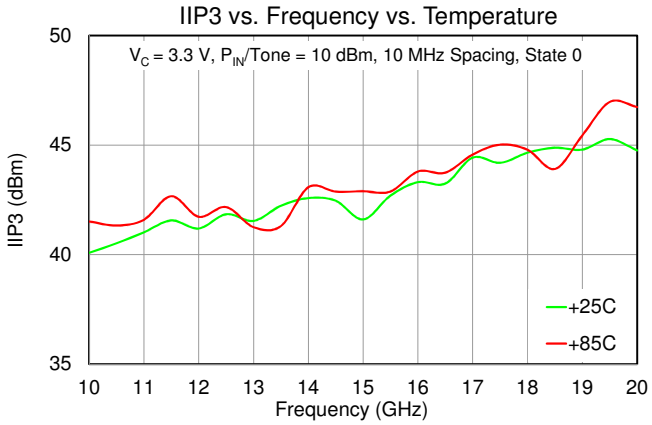
Ampl. Error vs. Frequency vs. State



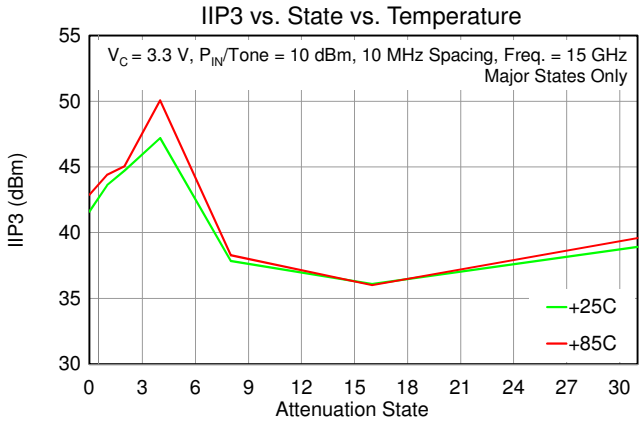
Gain vs. Input Power vs. State



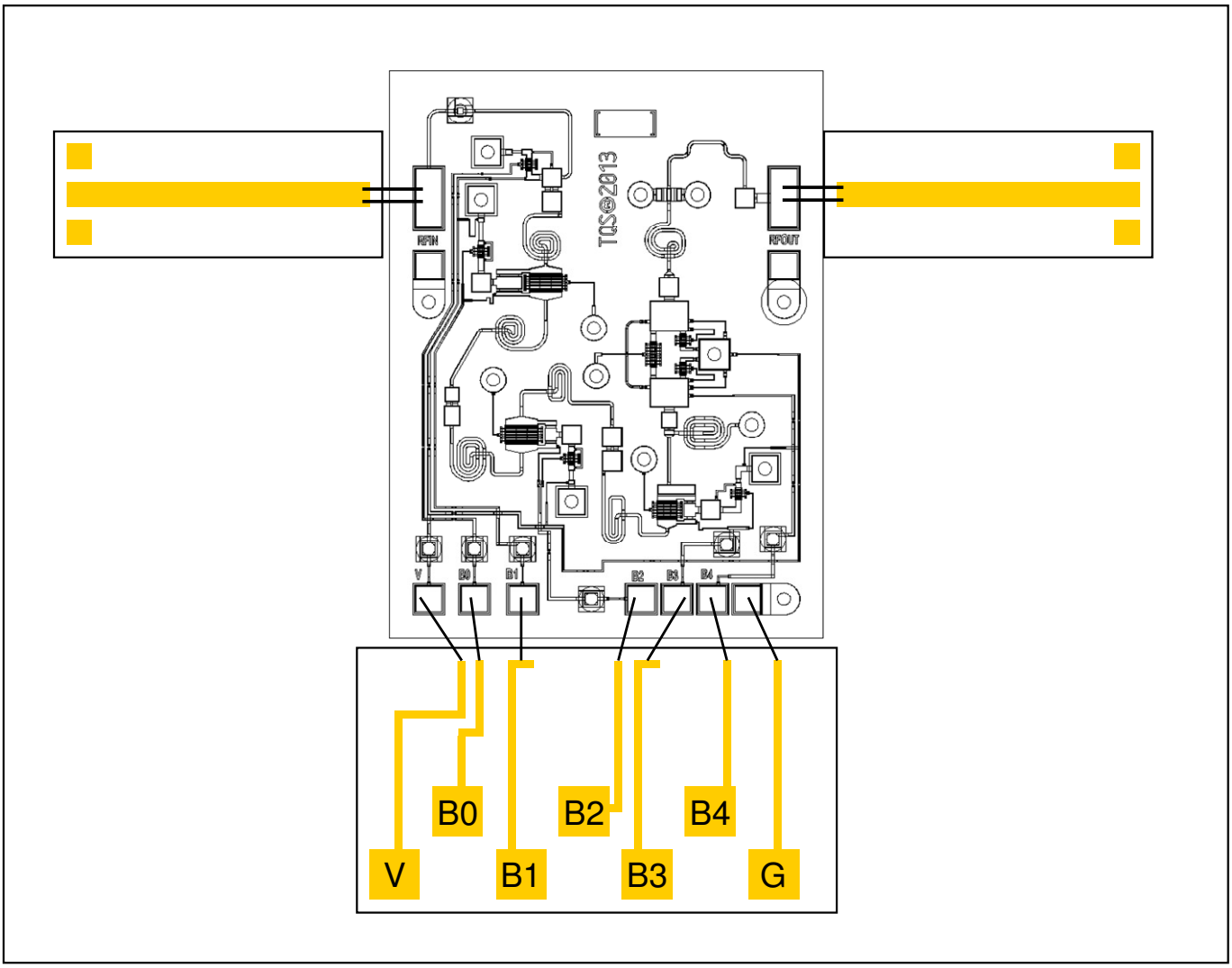
IIP3 vs. Frequency vs. Temperature



IIP3 vs. State vs. Temperature



Application Circuit

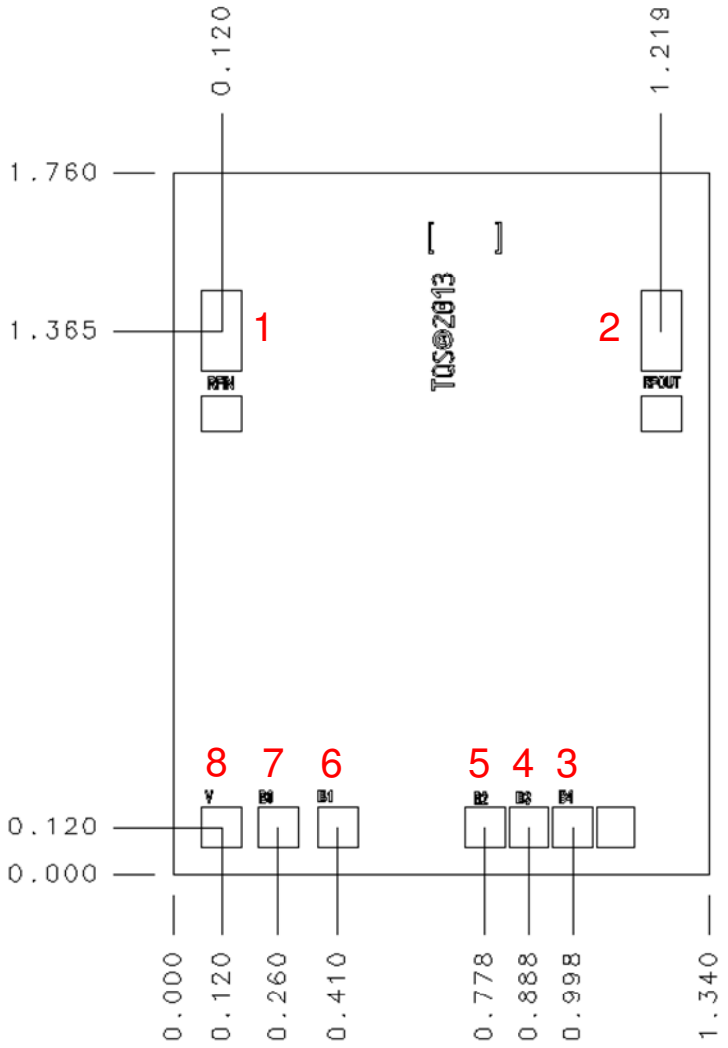


Function Table – Major States

Parameter	State	B0	B1	B2	B3	B4
0 dB Attenuation (Ref. State)	State 0	L	L	L	L	L
0.75 dB Attenuation	State 1	H	L	L	L	L
1.5 dB Attenuation	State 2	L	H	L	L	L
3.0 dB Attenuation	State 4	L	L	H	L	L
6.0 dB Attenuation	State 8	L	L	L	H	L
12.0 dB Attenuation	State 16	L	L	L	L	H
23.25 dB Attenuation	State 31	H	H	H	H	H

Intermediate attenuation states are combinations of the above major states.
Logic L = 0V. Logic H = 3.3-5.0 V

Mechanical Drawing and Bond Pad Description



Dimensions are in mm.

Pin Number	Label	Description	Pad Size (um)
1	RF Input	RF input, AC coupled	100 x 200
2	RF Output	RF output, AC coupled	100 x 200
3	B4	12.0 bit (MSB)	100 x 100
4	B3	6.0 bit	100 x 100
5	B2	3.0 bit	100 x 100
6	B1	1.5 dB bit	100 x 100
7	B0	0.75 dB bit (LSB)	100 x 100
8	V_{REF}	Reference voltage	100 x 100

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e., conductive epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ECCN

US Department of Commerce: EAR99

Solderability

Use only AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.

RoHS-Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@tqs.com **Fax:** +1.972.994.8504

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