TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

128 Mbit (16 M × 8 bit) CMOS NAND E^{2}PROM

DESCRIPTION

The TH58V128 device is a single 3.3 volt 128 M (138,412,032) bit NAND Electrically Erasable and Programmable Read Only Memory (NAND EEPROM) organized as 528 bytes × 32 pages × 1024 blocks. The device has a 528 byte static register which allows the program and read data to be transferred between the register and the memory cell array in 528 byte increments. The erase operation is implemented in a single block unit (16K bytes + 512 bytes : 528 bytes × 32 pages).

The TH58V128 is a serial type of memory device which utilizes the I/O pins for both address and data input / output as well as command inputs. The erase and program operations are automatically executed making the device most suitable for applications such as Solid State File Storage, Voice Recording, Image File Memory for digital still cameras and other systems which require a high-density non-volatile memory data storage.

FEATURES

- Organization
  - Memory cell array 528 × 16 K × 8× 2
  - Register 528 × 8
  - Page size 528 bytes
  - Block size (16 K + 512) bytes
- Mod
  - Read
  - Reset, Auto page program
  - Auto block erase, Status read
- Mode control
  - Serial input/output
  - Command control
- Power supply
  - V_{CC} = 3.3 V ± 0.3 V
- Access time
  - Cell array - Register 7 μs max
  - Serial Read Cycle 50 ns min
- Operating current
  - Read (80ns cycle) 10 mA typ
  - Program (ave.) 10 mA typ
  - Erase (ave.) 10 mA typ
  - Standby (CMOS) 100 μA max
- Package
  - TH58V128FT : TSOP II 44/40-P-400-0.80J (Weight : 0.51g typ)

PIN ASSIGNMENT (TOP VIEW)

TH58V128FT

V_{SS}	1	44	V_{CC}
CLE	2	43	$\overline{CE}$
ALE	3	42	$\overline{RE}$
$\overline{WE}$	4	41	R/$\overline{B}$
$\overline{WP}$	5	40	OP
NC	6	39	NC
NC	7	38	NC
NC	8	37	NC
NC	9	36	NC
NC	10	35	NC
	11	34	
	12	33	
NC	13	32	NC
NC	14	31	NC
NC	15	30	NC
NC	16	29	NC
NC	17	28	NC
I/O 1	18	27	I/O 8
I/O 2	19	26	I/O 7
I/O 3	20	25	I/O 6
I/O 4	21	24	I/O 5
V_{SS}	22	23	V_{CCQ}

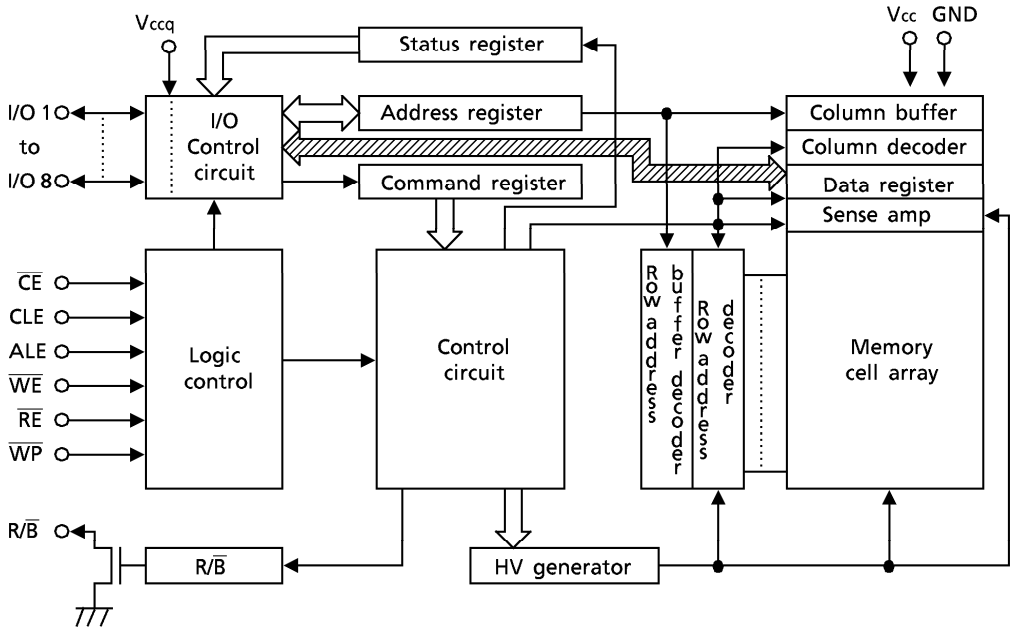
PIN NAMES

$I/O_{1\ to\ 8}$	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
R / $\overline{B}$	Ready / Busy
OP	Option Pin
Vcc	Power supply
Vccq	Output Buffer Power supply
V_{SS}	Ground

OP : GND Input : 528Byte/page Operation
VCC Input : 512Byte/Page Operation

980910EBA1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power supply Voltage	– 0.6 to 4.6	V
Vccq	output Buffer Power Supply	– 0.6 to 6.0	V
V_{IN}	Input Voltage	– 0.6 to 6.0	V
$V_{I/O}$	Input / Output Voltage	– 0.6V ~ Vccq + 0.3V(≦6.0V)	V
P_D	Power Dissipation	0.3	W
T_{STG}	Storage Temperature	– 55 to 150	°C
T_{SOLDER}	Sold ering Temperature (10s)	260	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	–	20	pF
C_{OUT}	Output	V_{OUT} = 0 V	–	20	pF

* This parameter is periodically sampled and is not tested for every component.

VALID BLOCKS *

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
N_{VB}	Valid Block Number	1004	1016	1024	Blocks

* The TH58V128 occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
Vccq	Output Buffer Power Supply	3.0	–	5.5	V
V_{IH}	High Level Input Voltage	2.0	–	Vccq + 0.3 *1	V
V_{IL}	Low Level Input Voltage	– 0.3 *2	–	0.8	V

*1 : OP : Vcc + 0.3V

*2 : – 2 V (pulse width ≦ 20 ns)

DC CHARACTERISTICS

(Ta = 0° to 70 °C, V_{CC} = 3.3 V ± 0.3 V , Vccq = 3.0V to 5.5V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}q	–	–	± 10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4 V to Vccq	–	–	± 10	μA
I_{CCO1}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, Iout = 0 mA, t_{cycle} = 50 ns	–	10	30	mA
I_{CCO3}	Operating Current (Command Input)	t_{cycle} = 50 ns	–	10	30	mA
I_{CCO4}	Operating Current (Data Input)	t_{cycle} = 50 ns	–	10	30	mA
I_{CCO5}	Operating Current (Address Input)	t_{cycle} = 50 ns	–	10	30	mA
I_{CCO7}	Programming Current	–	–	10	30	mA
I_{CCO8}	Erasing Current	–	–	10	30	mA
I_{CCS1}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}	–	–	1	mA
I_{CCS2}	Standby Current (CMOS)	$\overline{CE}$ = V_{CC}q – 0.2 V	–	–	100	μA
V_{OH}	High Level Output Voltage	I_{OH} = – 400 μA	2.4	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA	–	–	0.4	V
I_{OL} (R/$\overline{B}$)	Output Current of (R/$\overline{B}$) Pin	V_{OL} = 0.4 V	–	8	–	mA

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = 0° to 70 °C, V_{CC} = 3.3V ± 0.3V , Vccq = 3.0 V to 5.5 V)

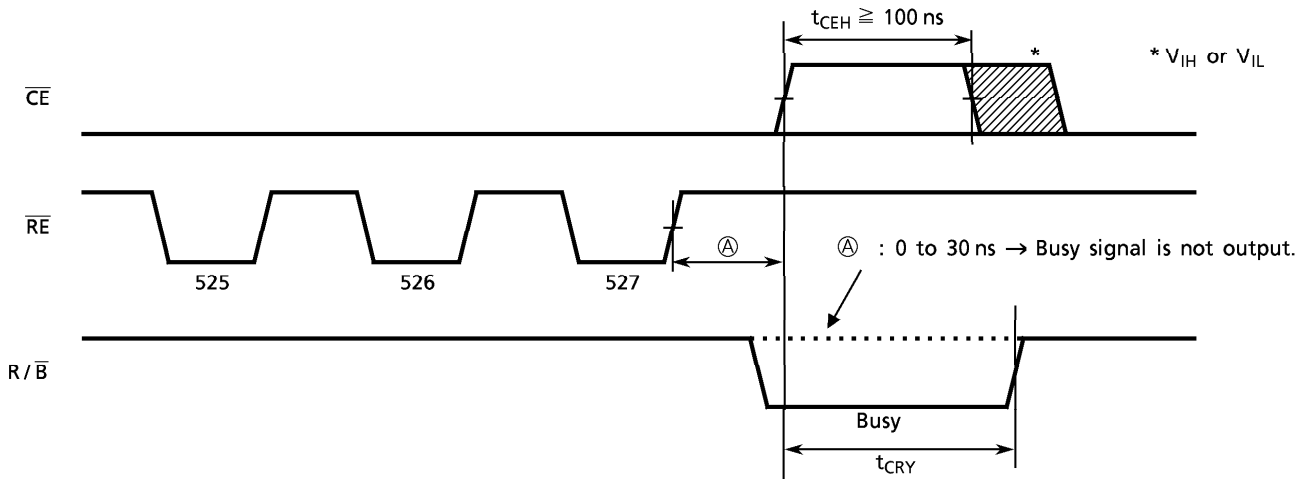
SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
t_{CLS}	CLE Set-Up Time	0	–	ns	
t_{CLH}	CLE Hold Time	10	–	ns	
t_{CS}	$\overline{CE}$ Set-Up Time	0	–	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	–	ns	
t_{WP}	Write Pulse Width	25	–	ns	
t_{ALS}	ALE Set-Up Time	0	–	ns	
t_{ALH}	ALE Hold Time	10	–	ns	
t_{DS}	Data Set-Up Time	20	–	ns	
t_{DH}	Data Hold Time	10	–	ns	
t_{WC}	Write Cycle Time	50	–	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	–	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	–	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	–	ns	
t_{RP}	Read Pulse Width	35	–	ns	
t_{RC}	Read Cycle Time	50	–	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)	–	35	ns	
t_{CEH}	$\overline{CE}$ High Time for interruption of data transfer from cell to register	100	–	ns	(2)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)	–	35	ns	
t_{OH}	Data Output Hold Time	10	–	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	–	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	–	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	–	ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0	–	ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	–	35	ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	–	45	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0	–	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	–	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	–	ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (ID Read)	100	–	ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (ID Read)	100	–	ns	
t_R	Data transfer from memory cell array to data register	–	7	μs	
t_{WB}	$\overline{WE}$ High to Busy	–	100	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	–	ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (in Sequential Read)	–	100	ns	
t_{CRY}	$\overline{CE}$ High to Ready (at interruption of data transfer from cell to register)	–	50 + tr (R/$\overline{B}$)	ns	(1)(2)
t_{RST}	Device Resetting Time (Read/Program/Erase)	–	6/10/500	μs	

AC TEST CONDITIONS

Input level	:	2.4 V / 0.4 V
Input pulse rise and fall time	:	3ns
Input comparison level	:	1.5 V / 1.5 V
Output data comparison level	:	1.5 V / 1.5 V
Output load	:	1TTL & C_L (100 pF)

Note : (1) $\overline{CE}$ High to Ready time depends on the pull-up resistor tied to the R/$\overline{B}$ pin.
(Refer to Application Note (7) toward the end of this document.)

(2) Sequential Read is terminated when t_{CEH} is greater than or equal to 100 ns.
If the $\overline{RE}$ to $\overline{CE}$ delay is less than 30ns, R/$\overline{B}$ signal stays Ready.



PROGRAMMING AND ERASING CHARACTERISTICS

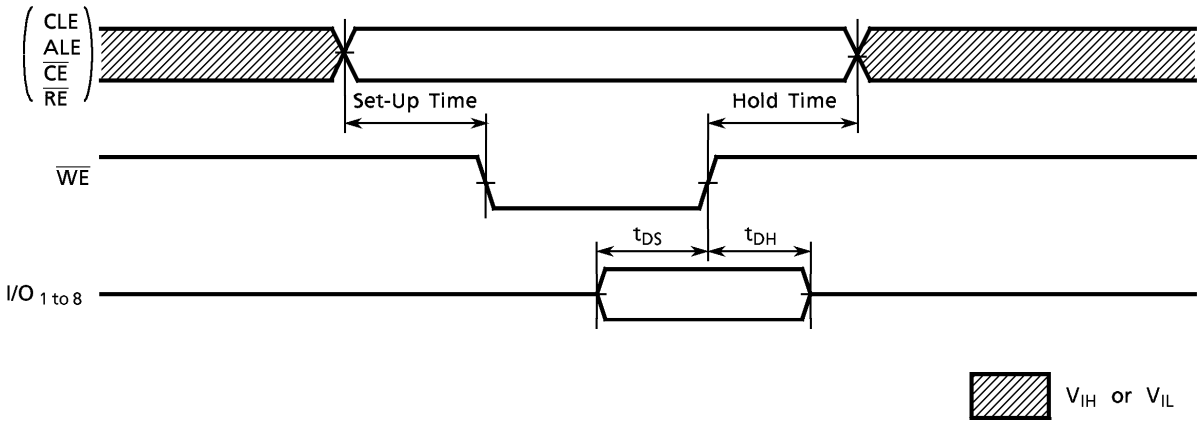
(Ta = 0° to 70 °C, V_{CC} = 3.3V ± 0.3V , Vccq = 3.0 V to 5.5 V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
t_{PROG}	Average Programming Time		200	1000	μs	
N	Number of Programming Cycles on Same Page			10		(1)
t_{BERASE}	Block Erasing Time		2	20	ms	
P/E	Number of Program/Erase Cycles			1×10^6		(2)

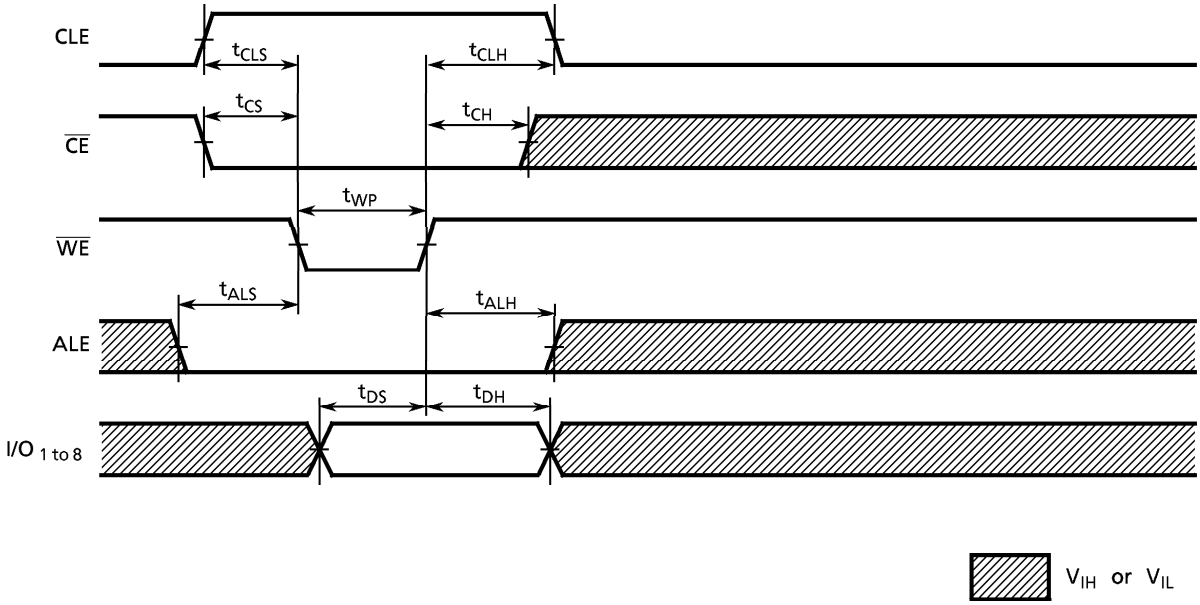
(1) Refer to Application Note (12) toward the end of this document.
(2) Refer to Application Note (15) toward the end of this document.

TIMING DIAGRAMS

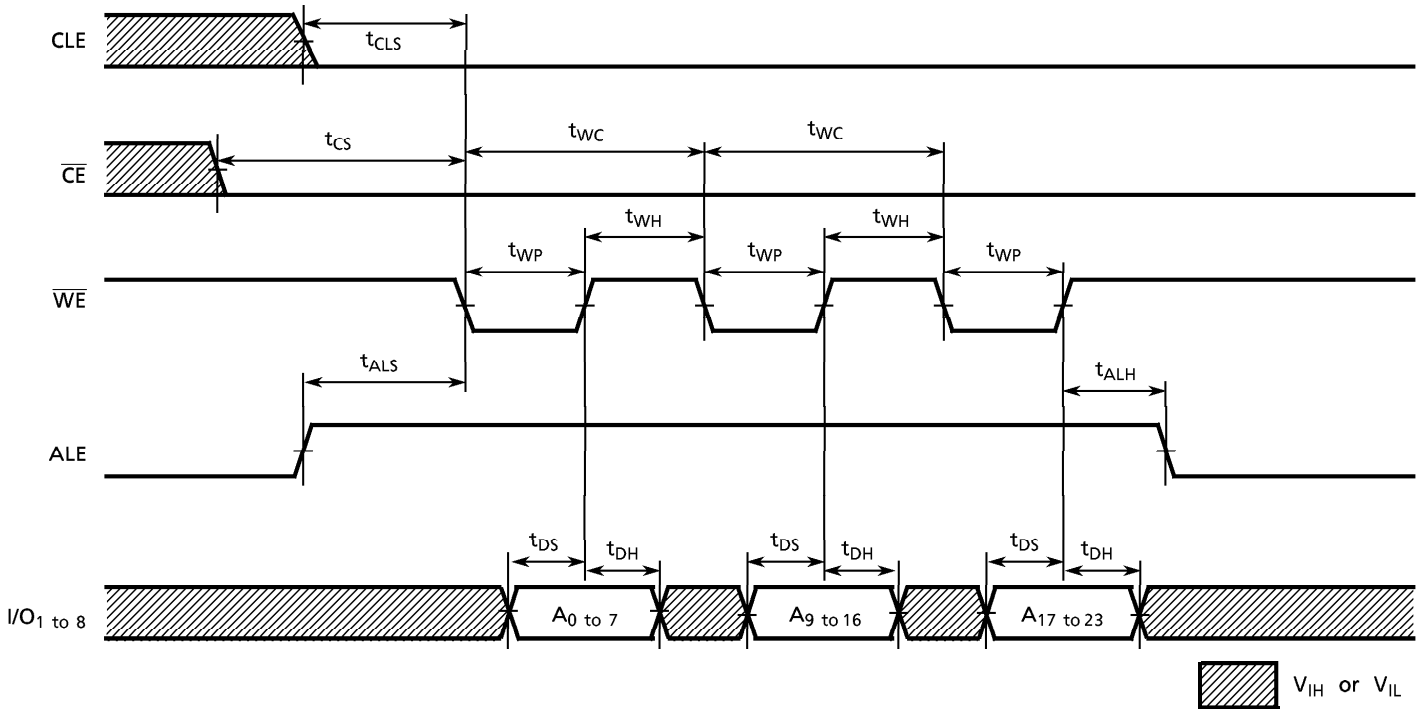
Latch Timing Diagram for Command/Address /Data



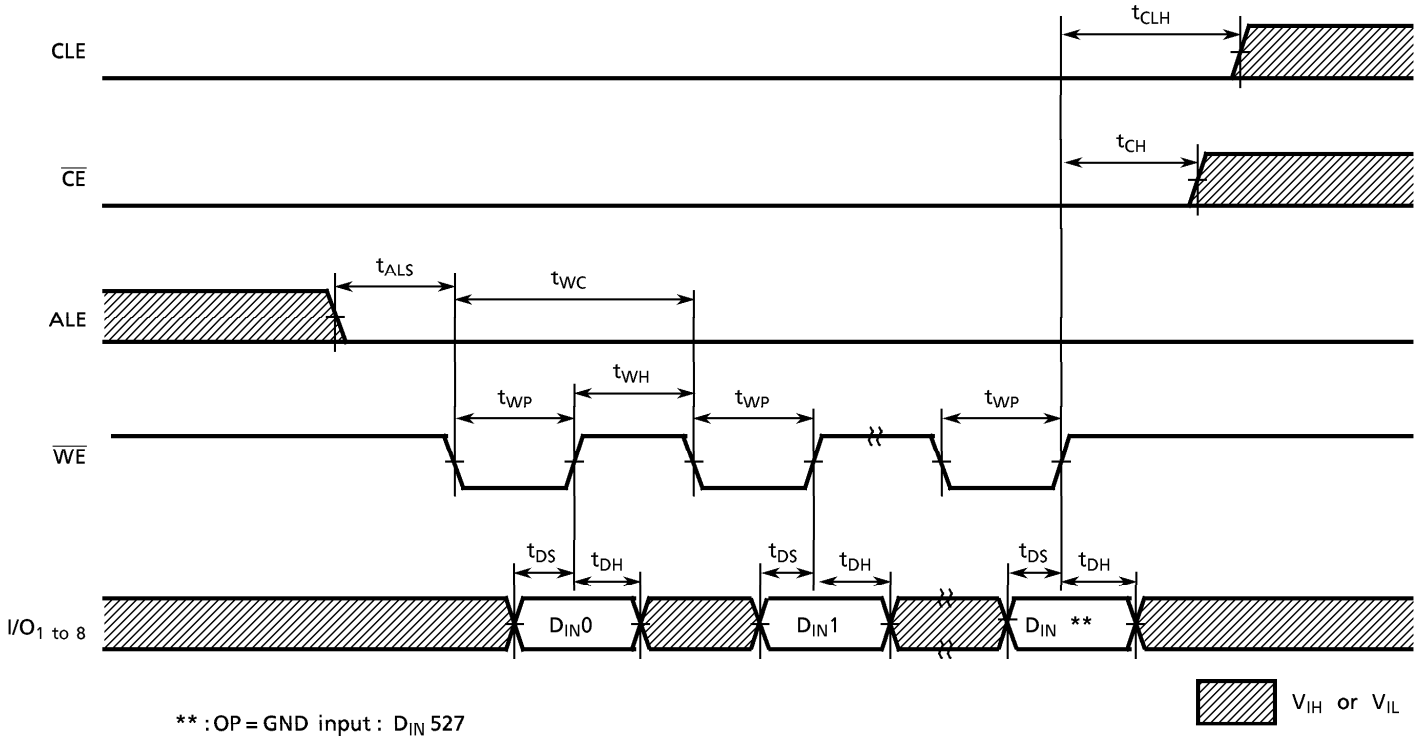
Command Input Cycle Timing Diagram



Address Input Cycle Timing Diagram

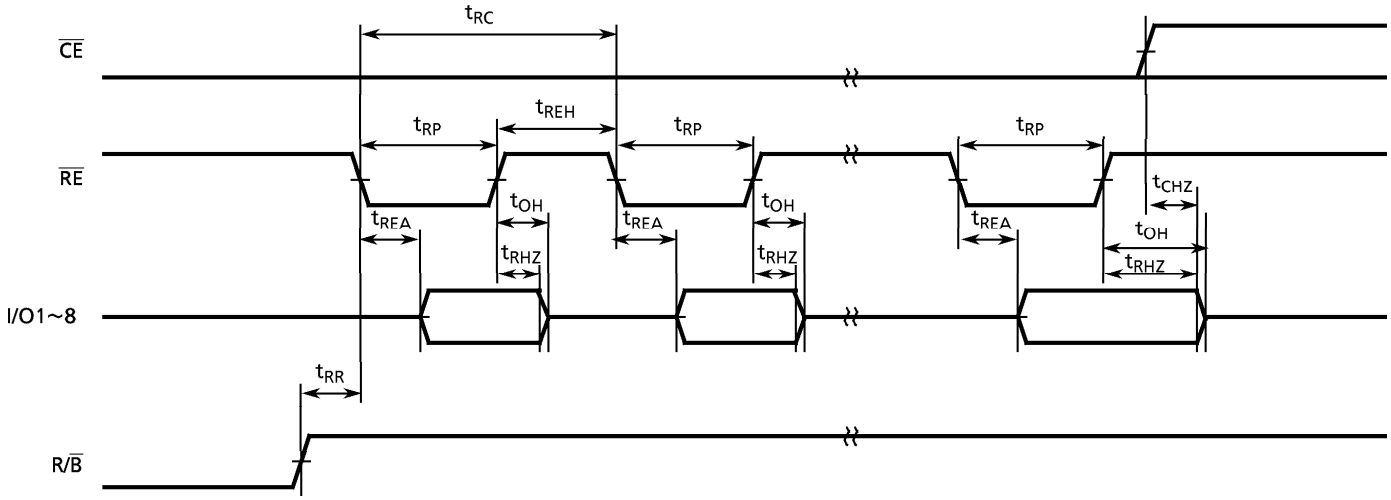


Data Input Cycle Timing Diagram

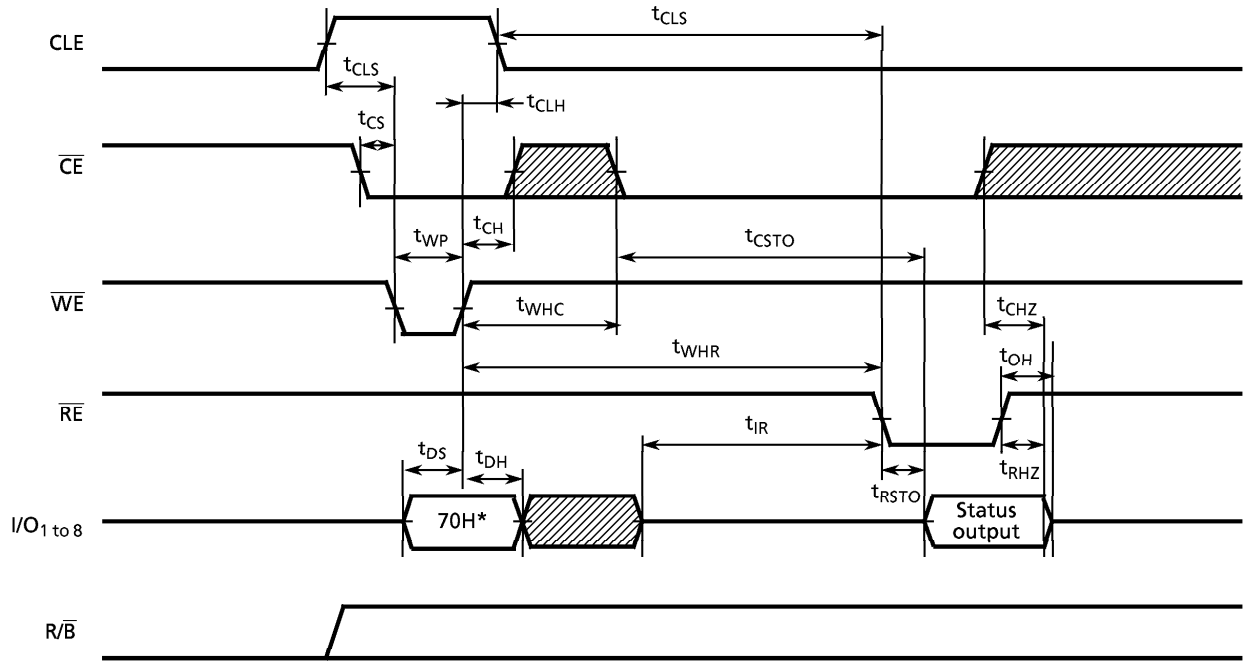


** : OP = GND input : D_{IN} 527
OP = VCC input : D_{IN} 511

Serial Read Cycle Timing Diagram



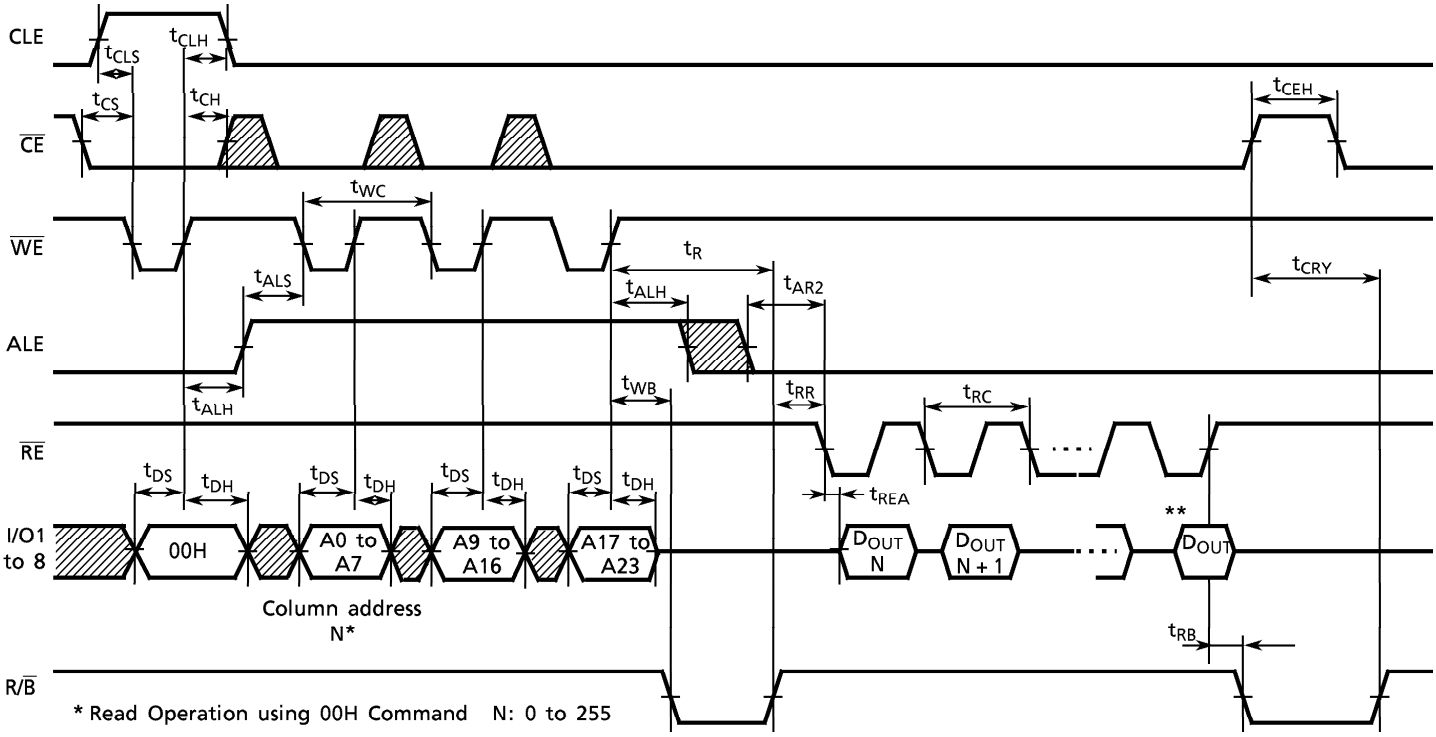
Status Read Cycle Timing Diagram



* 70H - 70 in HEX data

: V_{IH} or V_{IL}

Read Cycle (1) Timing Diagram

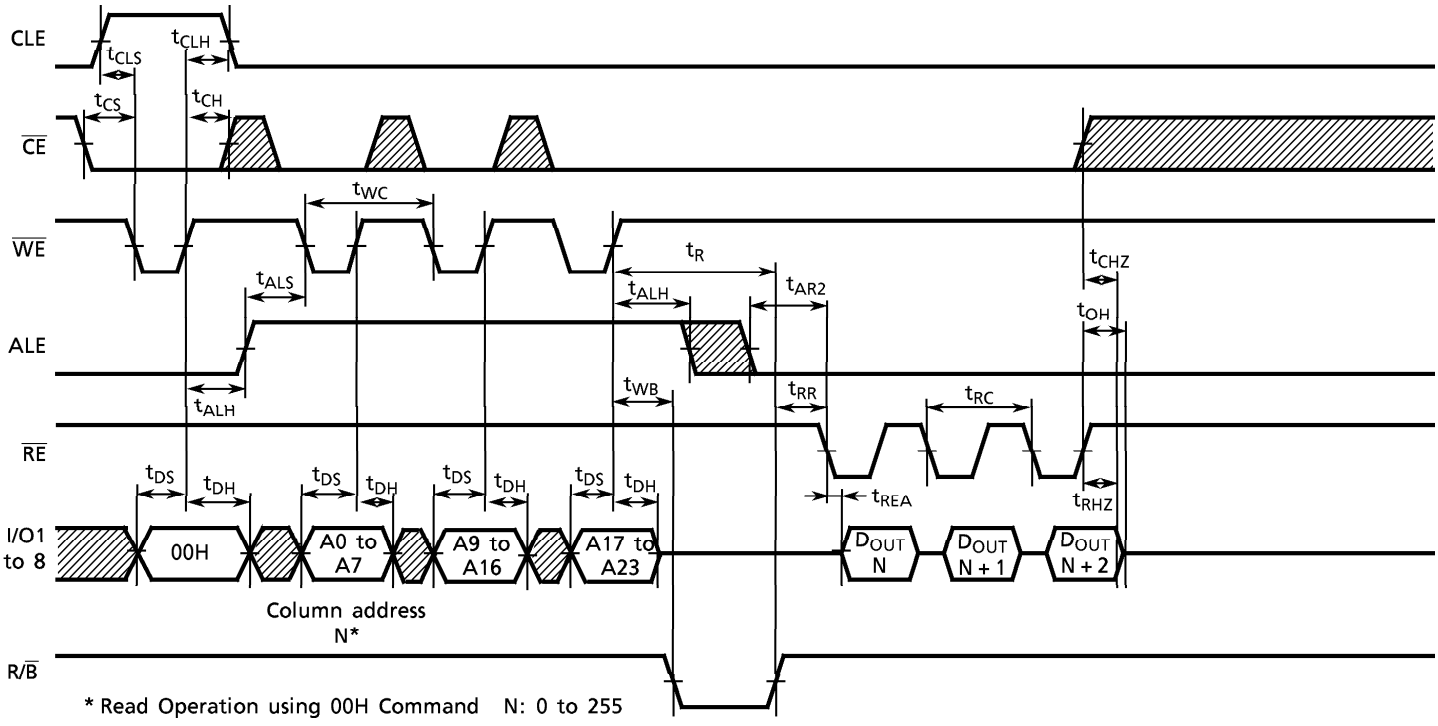


* Read Operation using 00H Command N: 0 to 255

** : OP = GND input : D_{OUT} 527
OP = GND input : D_{OUT} 511

: V_{IH} or V_{IL}

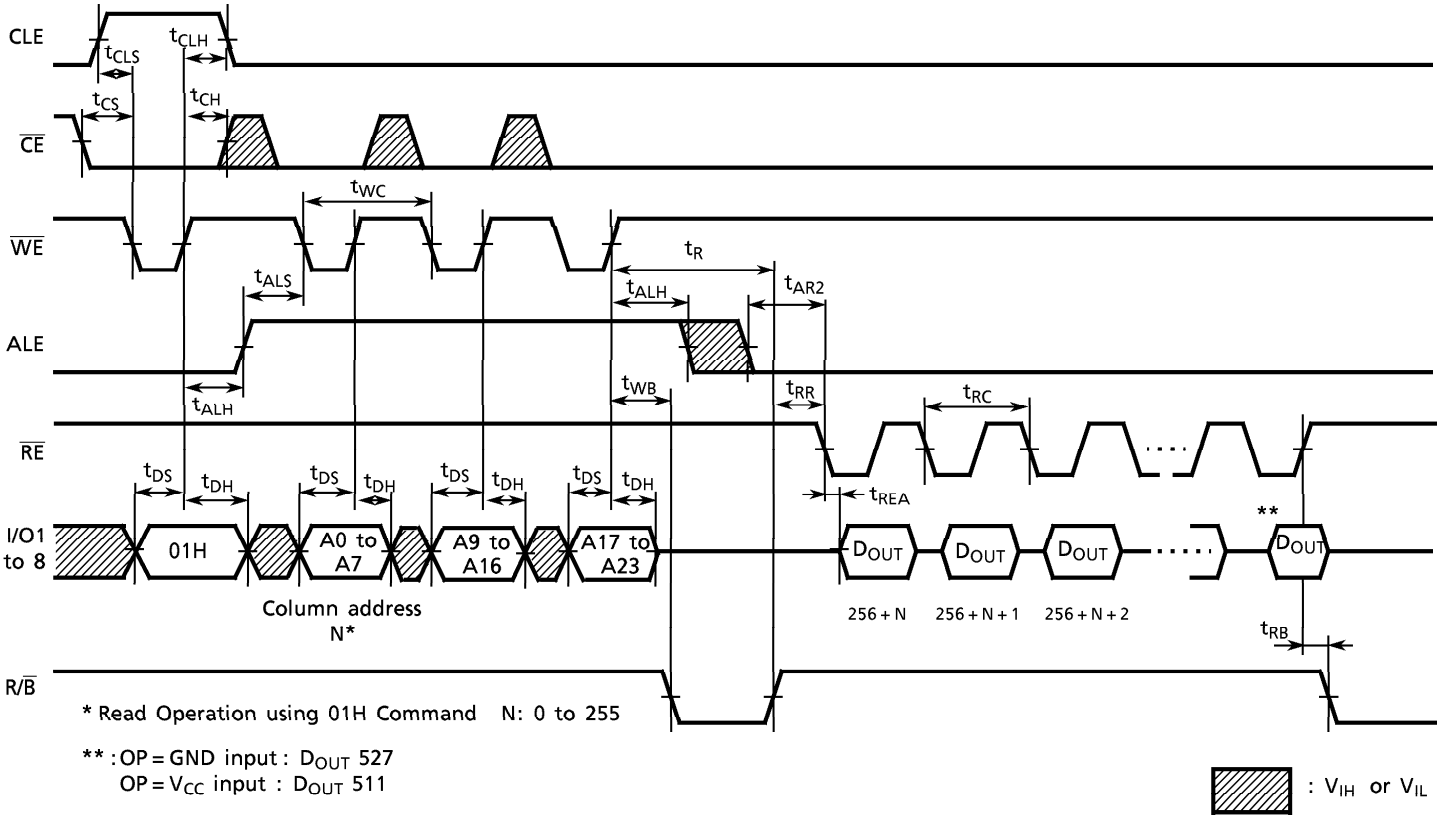
Read Cycle (1) Timing Diagram: Interrupted by $\overline{CE}$



* Read Operation using 00H Command N: 0 to 255

: V_{IH} or V_{IL}

Read Cycle (2) Timing Diagram

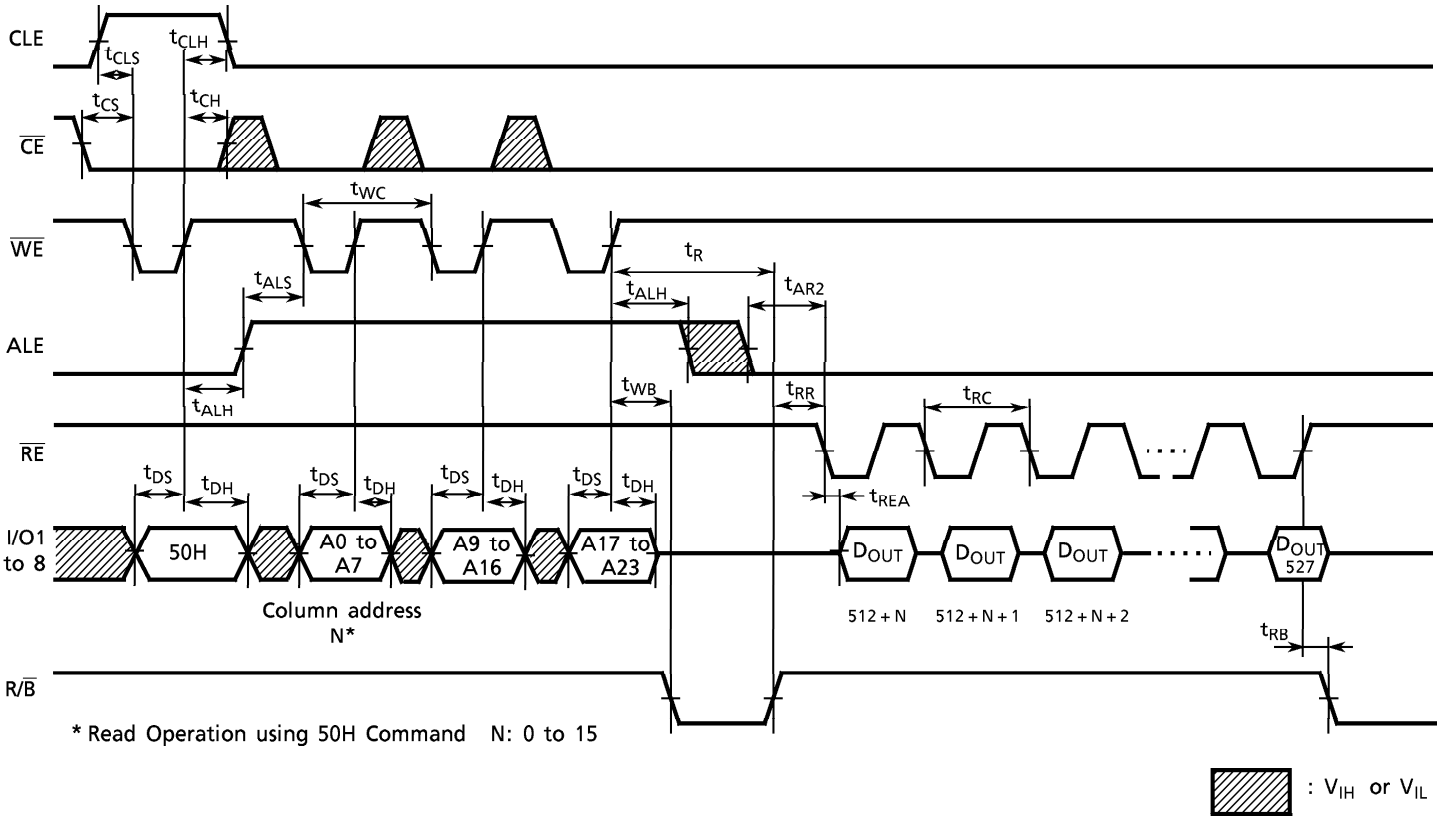


* Read Operation using 01H Command N: 0 to 255

** : OP = GND input : D_{OUT} 527
OP = V_{CC} input : D_{OUT} 511

: V_{IH} or V_{IL}

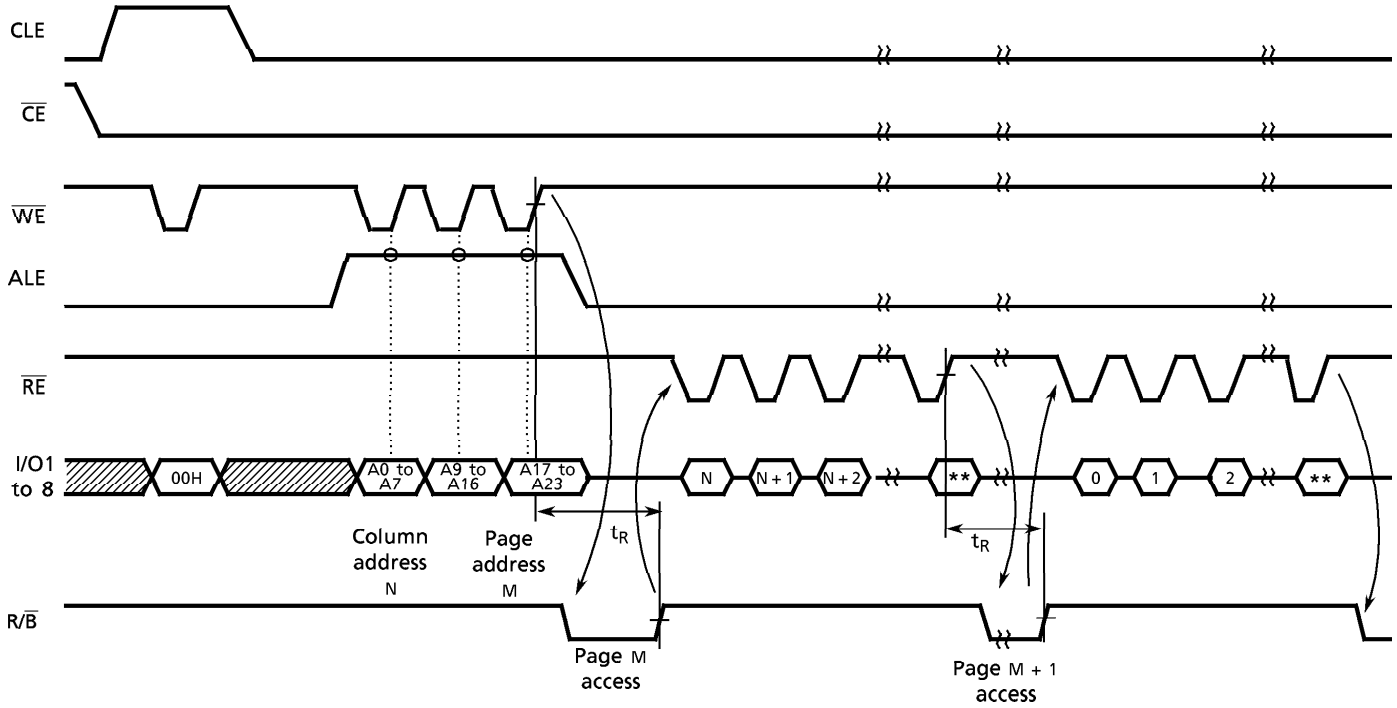
Read Cycle (3) Timing Diagram(OP=GND input)



* Read Operation using 50H Command N: 0 to 15

: V_{IH} or V_{IL}

Sequential Read (1) Timing Diagram

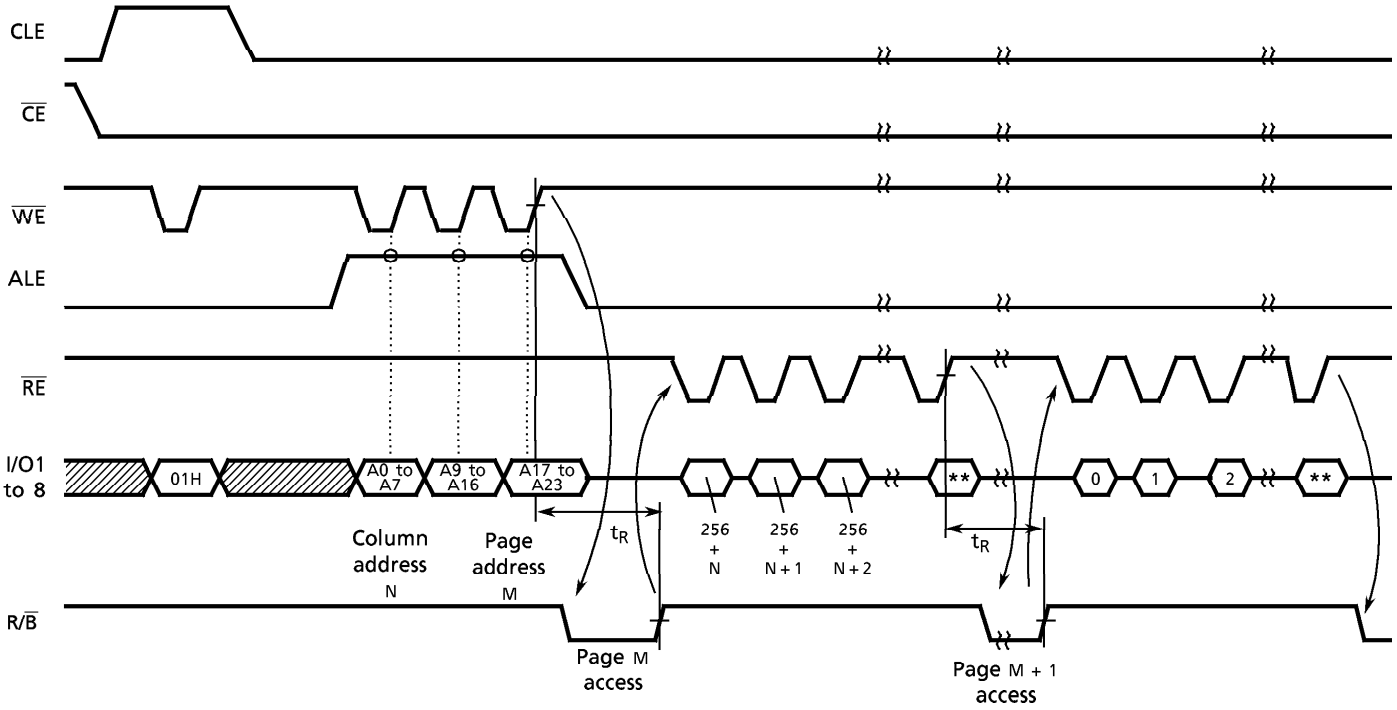


* Read Operation using 00H Command N: 0 to 255

** : OP = GND input : D_{OUT} 527
OP = V_{CC} input : D_{OUT} 511

: V_{IH} or V_{IL}

Sequential Read (2) Timing Diagram

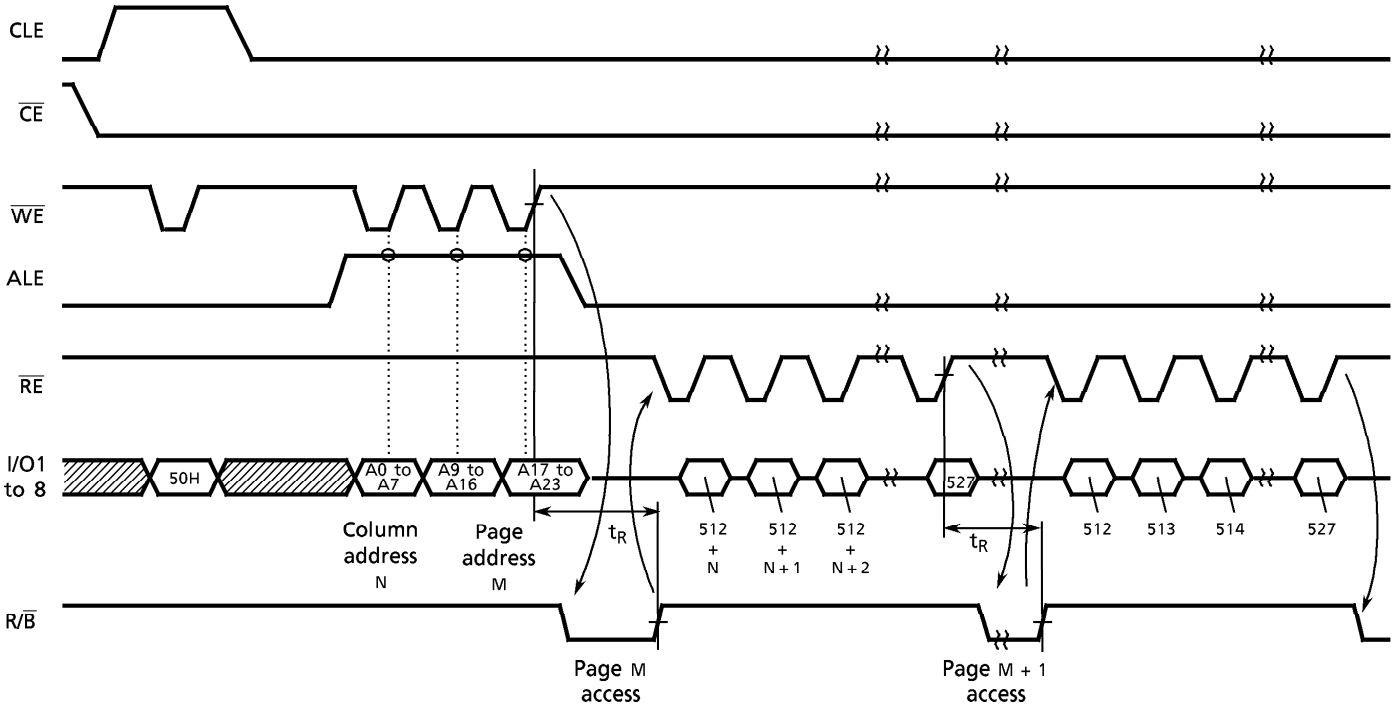


* Read Operation using 01H Command N: 0 to 255

** : OP = GND input : D_{OUT} 527
OP = V_{CC} input : D_{OUT} 511

: V_{IH} or V_{IL}

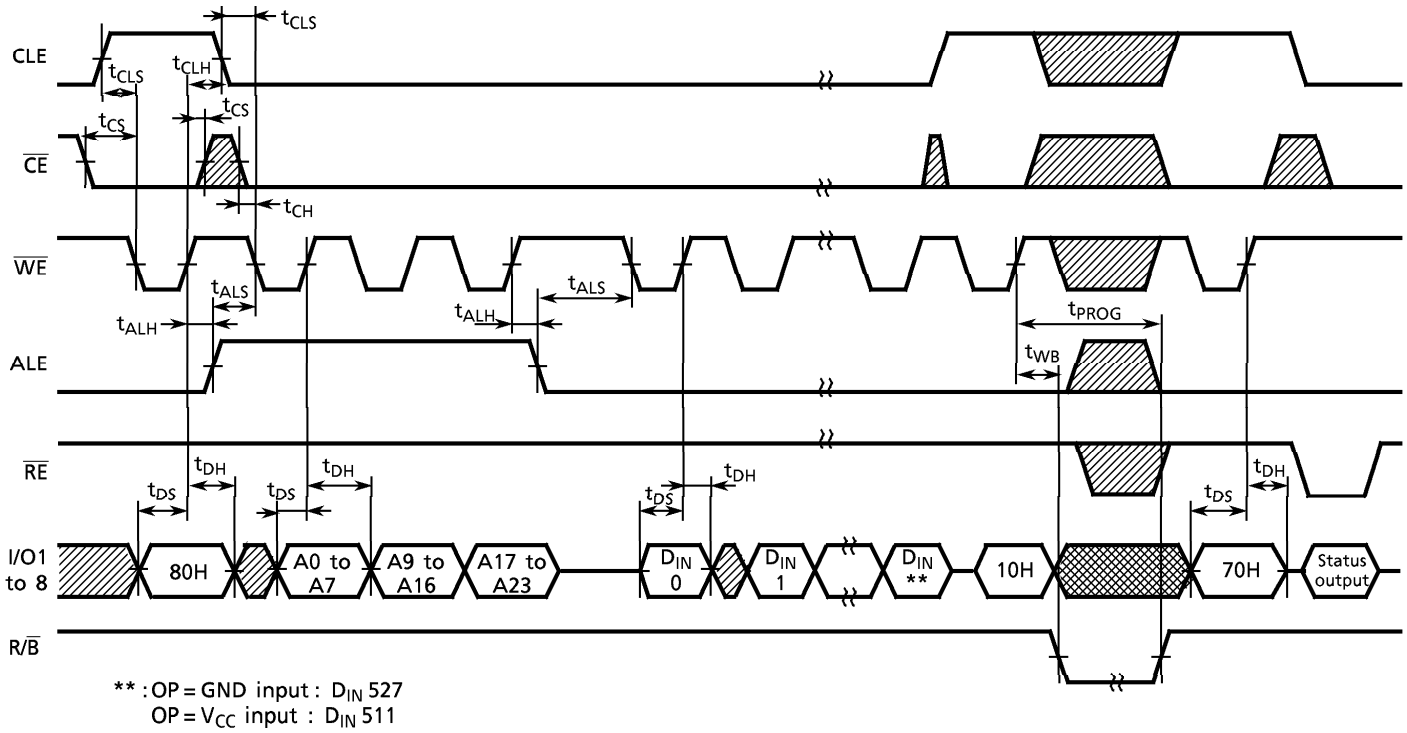
Sequential Read (3) Timing Diagram (OP = GND input)



* Read Operation using 50H Command N: 0 to 15

: V_{IH} or V_{IL}

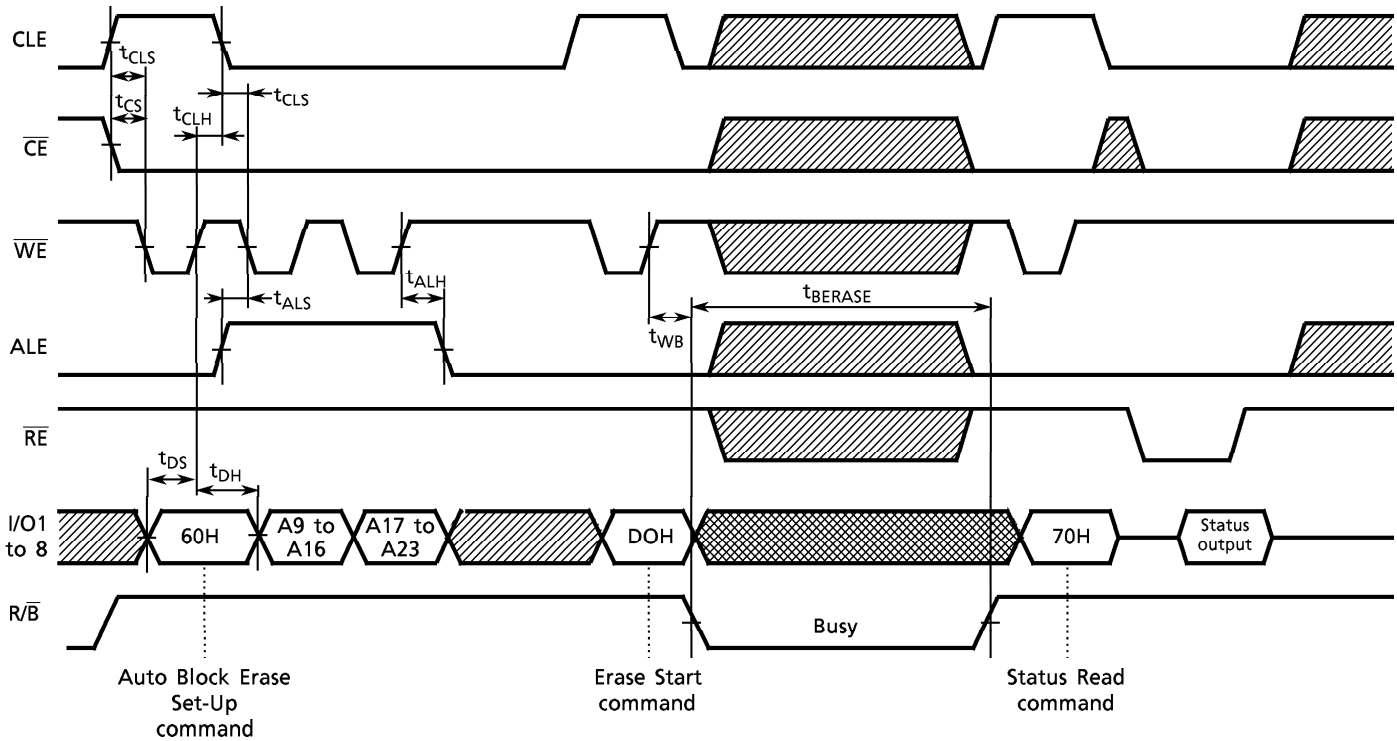
Auto Program Operation Timing Diagram



** : OP = GND input : D_{IN} 527
OP = V_{CC} input : D_{IN} 511

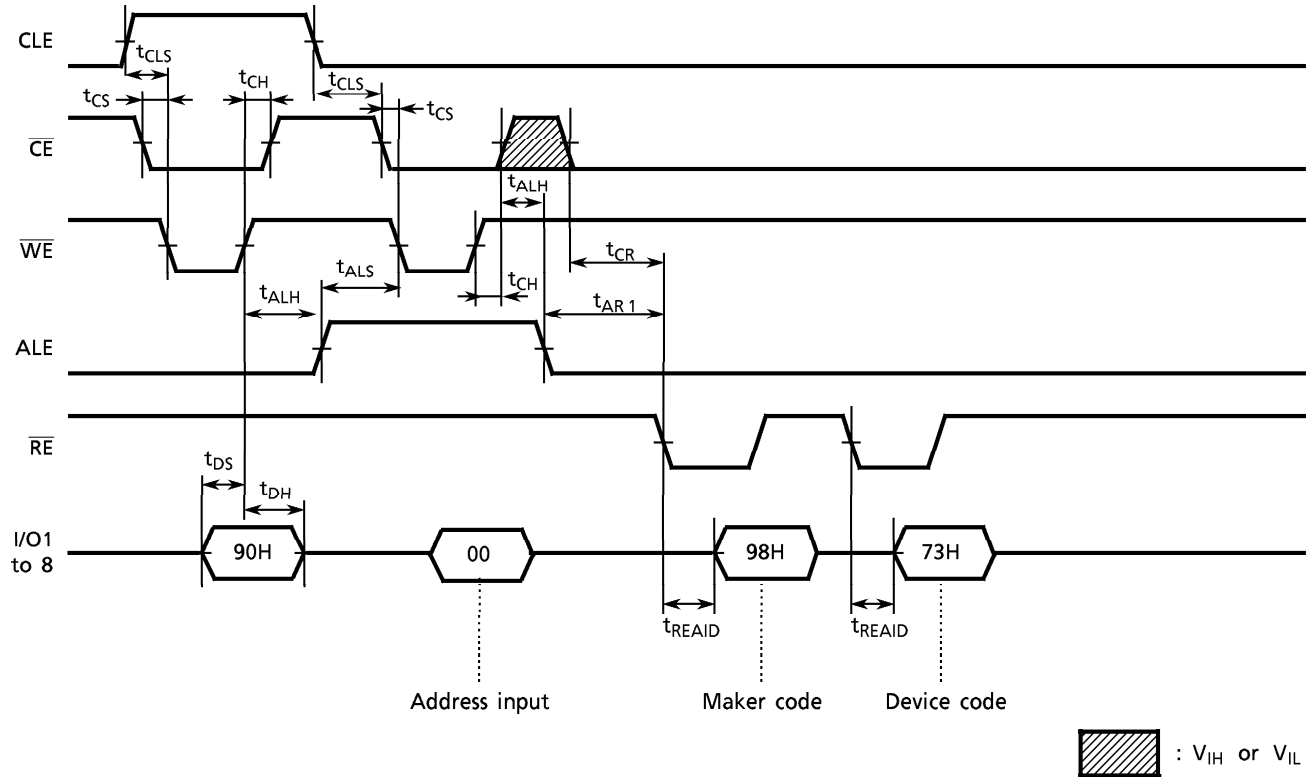
: V_{IH} or V_{IL} : If data is being output, do not allow any input.

Auto Block Erase Timing Diagram



: V_{IH} or V_{IL} : If data is being output, do not allow any input.

ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

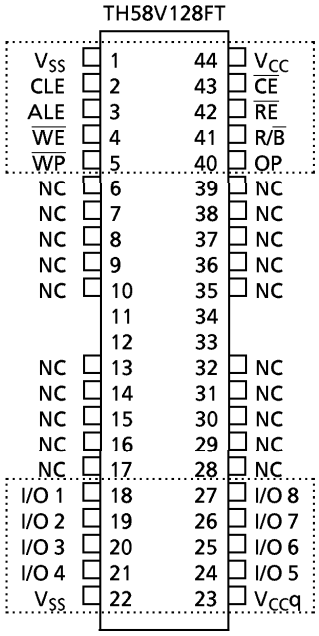


Figure 1. Pinout

Command Latch Enable: CLE

The CLE input signal is used to control the acquisition of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control the acquisition of either address information or input data into the internal address/data resistor. Address information is latched on the rising edge of $\overline{WE}$ if ALE is High. Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$

The device goes into a low power Standby mode when $\overline{CE}$ goes High during a Read operation . The $\overline{CE}$ signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register. However, the $\overline{CE}$ signal is ignored when the device is in Busy state ($R/\overline{B}$ = L) during a Program or Erase operation, and will not go into Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address + 1) on this falling edge.

I/O Port: I/O 1 to 8

The I /O 1 to 8 pins are used as the port for transferring address, command and input/output data to or from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low.This signal is usually used for protecting the data during the power on/off sequence when input signals are invalid.

Ready/Busy: $R/\overline{B}$

The $R/\overline{B}$ output signal is used to indicate the operating condition of the device. The $R/\overline{B}$ signal is in Busy state ($R/\overline{B}$ = L) during the Program, Erase or Read operations and will return to Ready state ($R/\overline{B}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Option Pin: OP

The OP signal is used to change the page size. The device is in 528 byte/page mode when OP = GND, and 512 byte/page mode when OP = V_{CC}.

Schematic Cell Layout and Address Assignment

The Program operation is implemented in a page units while the Erase operation is carried out in block units.

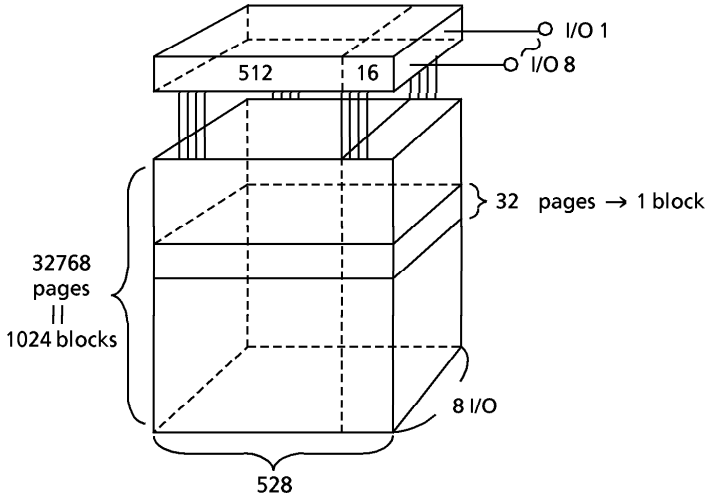


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are for main memory and 16 bytes are for redundancy or other uses.

1 Page = 528 bytes
1 Block = 528 bytes × 32 pages = (16 K + 512) bytes
Total Device Density = 528 bytes × 32 pages × 1024 blocks

The address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	* L	A23	A22	A21	A20	A19	A18	A17

A0 to A7 : column address
A9 to A23 : page address
(A14 to A23: block address
A9 to A13 : NAND address in block)

*: A8 is automatically set to Low or High by a 00H command or a 01H command.
*: I/O8 must be set to Low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the eleven different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

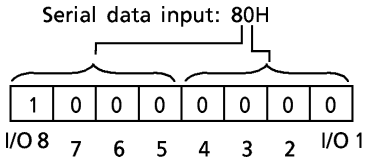
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	⌐↗	H	*
Data Input	L	L	L	⌐↗	H	*
Address Input	L	H	L	⌐↗	H	*
Serial Data Output	L	L	L	H	↘⌐	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

Table 3. Command table (HEX data)

	First Cycle	Second Cycle	Acceptable While Busy
Serial Data Input	80	–	
Read Mode (1)	00	–	
Read Mode (2)	01	–	
Read Mode (3)	50	–	
Reset	FF	–	○
Auto Program	10	–	
Auto Block Erase	60	D0	
Status Read	70	–	○
ID Read	90	–	

HEX data bit assignment
(Example)



Once the device has been set to Read mode by the 00H, 01H or 50H command, additional Read commands are not needed for the following page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

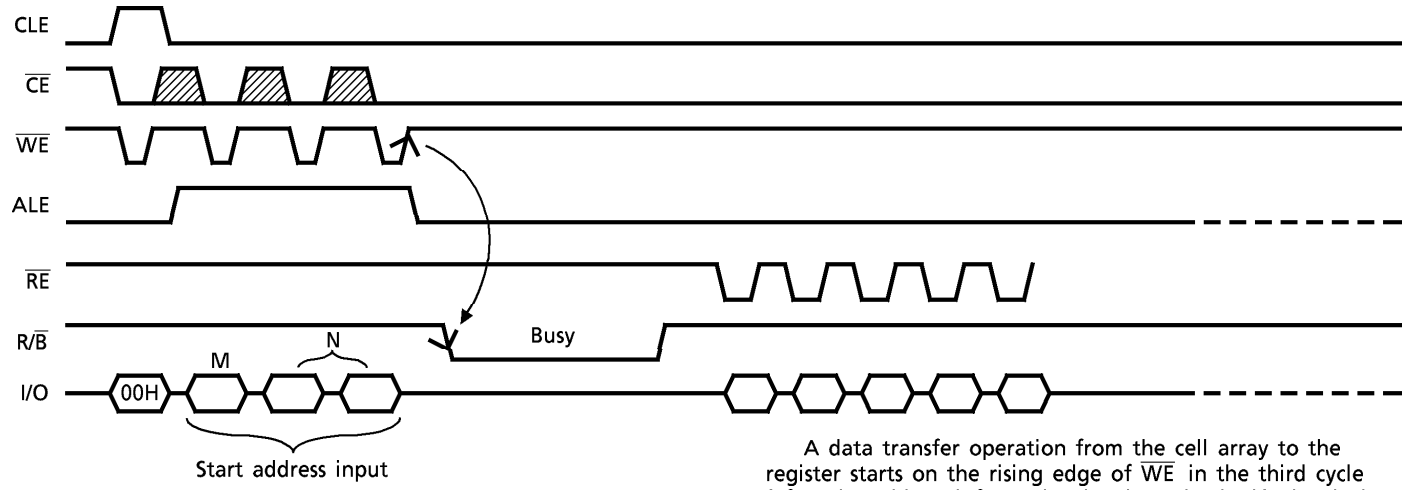
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O 1 TO I/O 8	POWER
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active
Standby	L	L	H	H	*	High impedance	Standby

H : V_{IH} L : V_{IL} * : V_{IH} or V_{IL}

DEVICE OPERATION

Read Mode (1)

Read mode (1) is set by issuing a 00H command to the command register. Refer to Figure 3 below for timing details and block diagram.



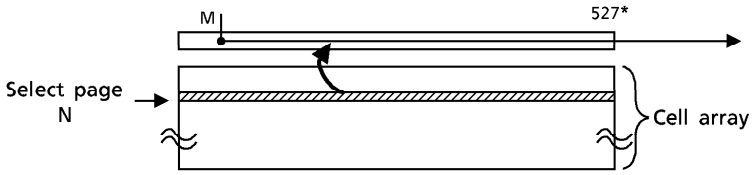


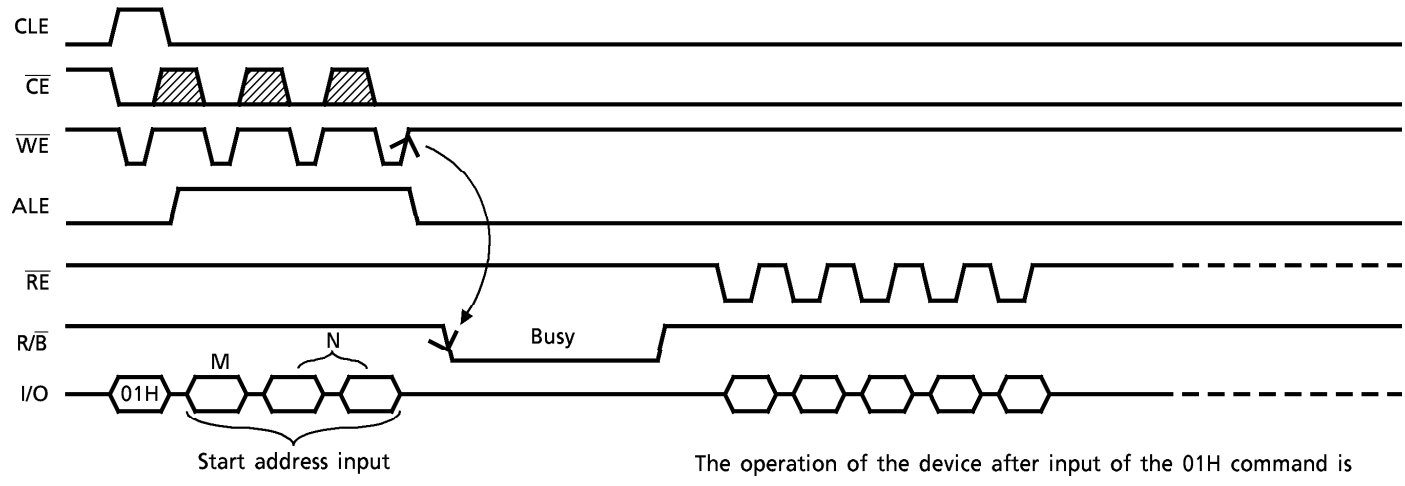
Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the third cycle (after the address information has been latched.) The device will be in Busy state during this transfer period. The $\overline{CE}$ signal must stay Low after the third address input and during Busy state.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

* When OP is V_{CC} Level, column address is up to 511.

Read Mode (2)



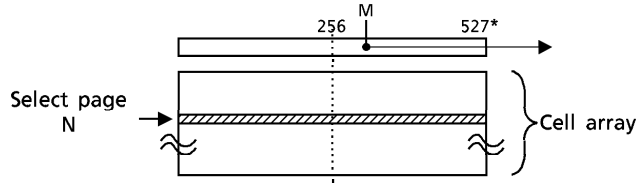


Figure 4. Read mode (2) operation

The operation of the device after input of the 01H command is the same as that of Read mode (1). If the start pointer is to be set after column address 256, use Read mode (2).

Read mode (2) initially sets the address pointer to the second half of the page. However, if you read past byte 527 (sequential read), then output from the next page (N + 1) starts from column address 0, not address 256.

* When OP is at V_{CC} Level, column address is up to 511.

Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore assigned between bytes 512 and 527. Read mode (3) operation is invalid when OP is at V_{CC} Level.

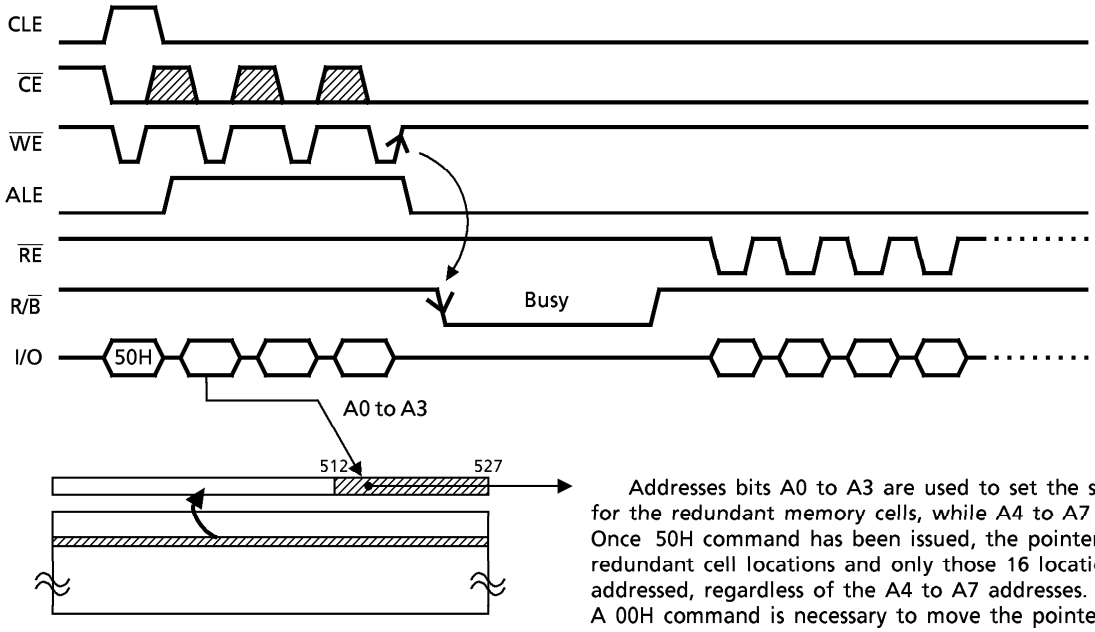
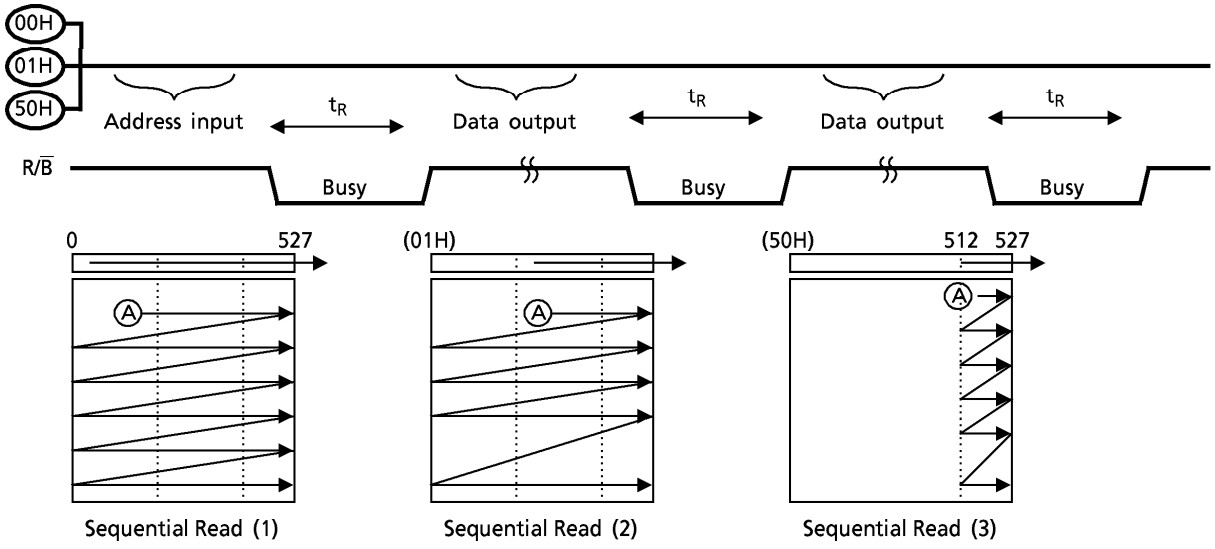


Figure 5. Read mode (3) operation

Addresses bits A0 to A3 are used to set the start pointer for the redundant memory cells, while A4 to A7 are ignored. Once 50H command has been issued, the pointer moves to the redundant cell locations and only those 16 locations can be addressed, regardless of the A4 to A7 addresses.
A 00H command is necessary to move the pointer back to the main memory cell locations (addresses 0 to 511).

Sequential Read (1)(2)(3)

This mode allows the sequential reading of pages without additional address input.
The figure below show each operation of Sequential Read when OP is at Vcc Level.



Sequential Read modes (1) and (2) output the contents of addresses 0 to 527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only.

When the page address reaches the next block address, read commands (00H / 01H / 50H) and address inputs are needed.

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a 70H command input. The resulting information is outlined in Table 5.

Table 5. Status output table

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass : '0'	Fail : '1'
I/O2	Not used	'0'	
I/O3	Not used	'0'	
I/O4	Not used	'0'	
I/O5	Not used	'0'	
I/O6	Not used	'0'	
I/O7	Ready/Busy	Ready : '1'	Busy : '0'
I/O8	Write protect	Protect :'0'	Not Protect : '1'

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

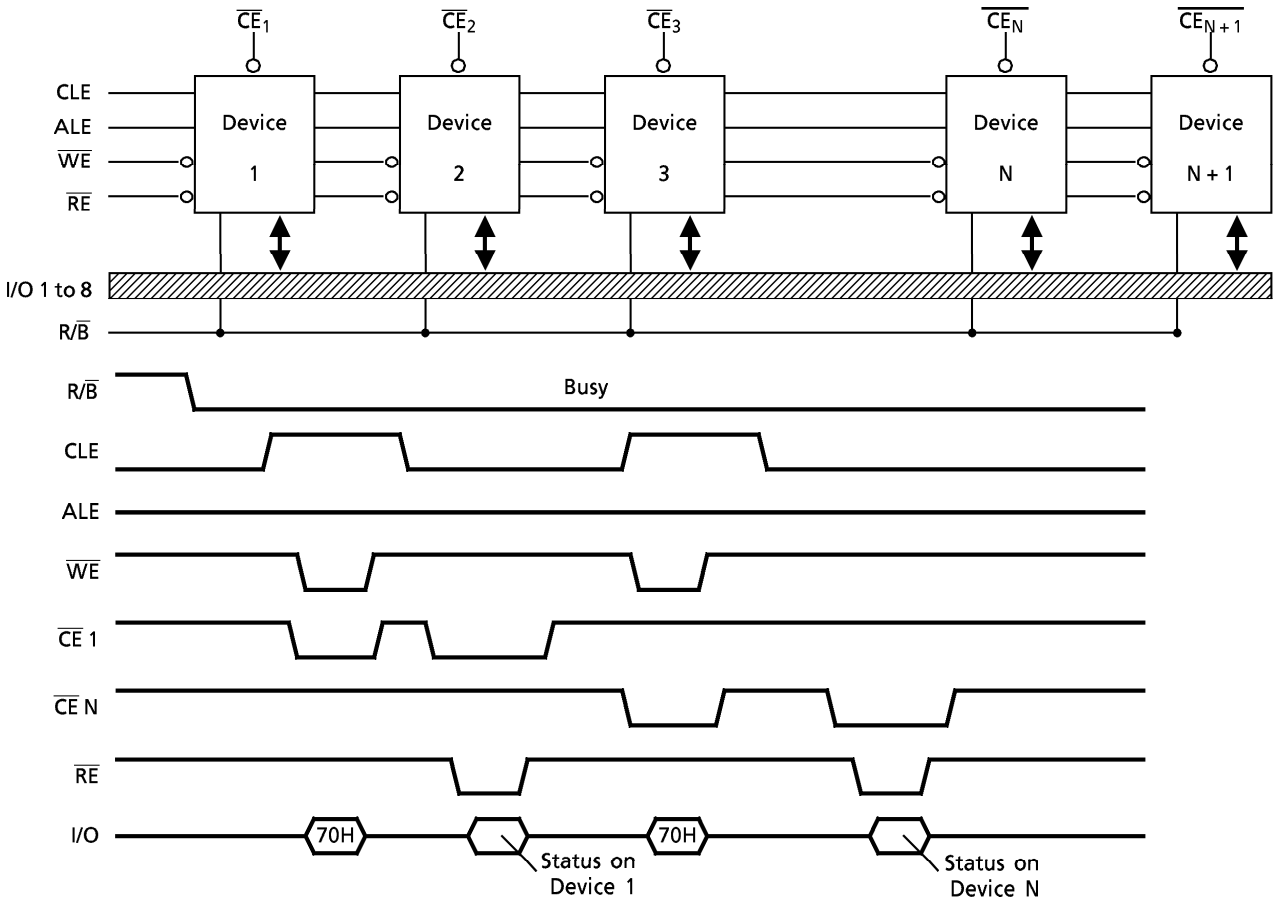
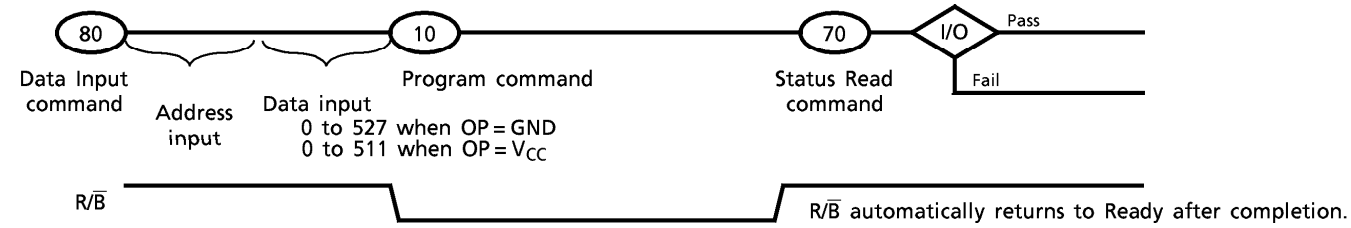


Figure 6. Status read timing application example

SYSTEM DESIGN NOTE : If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device implements the Automatic Page Program operation when it receives a 10H Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



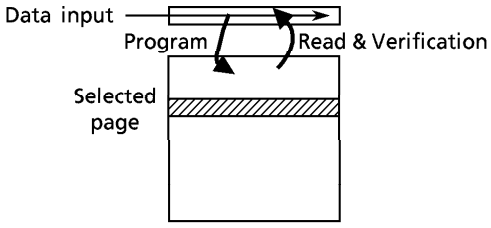
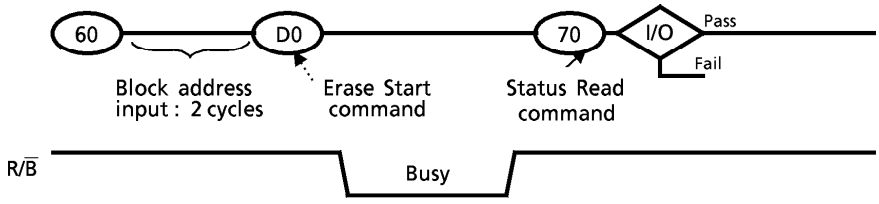


Figure 7. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the 10H command. After programming the programmed data is transferred back to the register to be automatically verified by the device. If the program does not succeed, the above Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command D0H which follows the Erase Set-Up command 60H. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



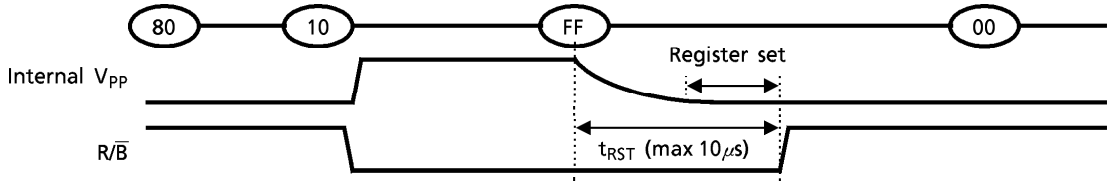
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the regulated voltage is discharged to 0 volts and the device will go into Wait state. The address and data registers are set as follows after a Reset:

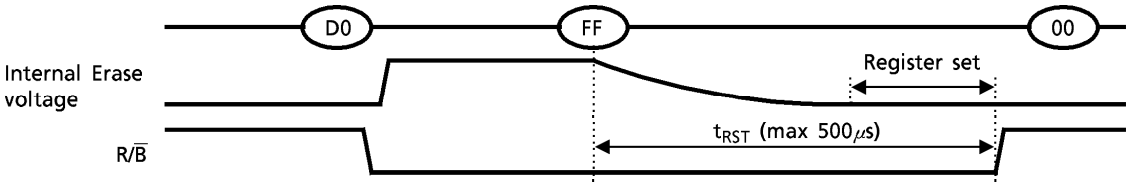
- Address Register : All '0'
- Data Register : All '1'
- Operation Mode : Wait State

The response after an FFH Reset command is input during the various operations are as follows:

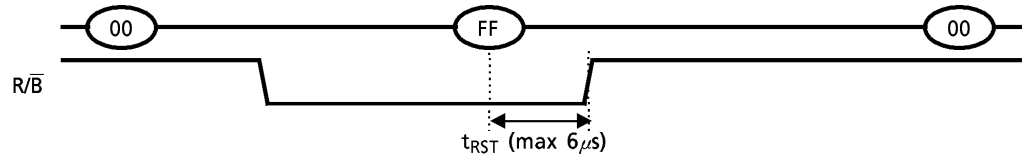
① When a Reset (FFH) command is input during programming



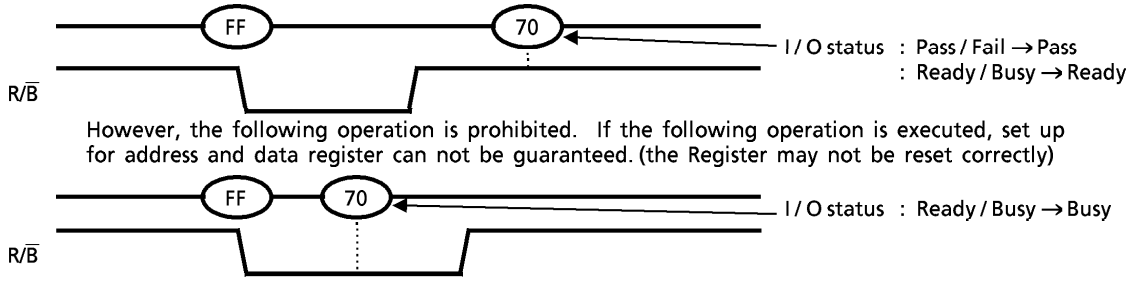
② When a Reset (FFH) command is input during erasing



③ When a reset (FFH) command is input during a Read operation

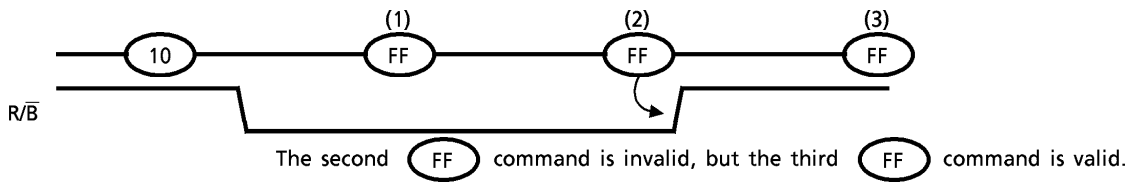


⑤ When a Status Read command (70H) is input after a Reset



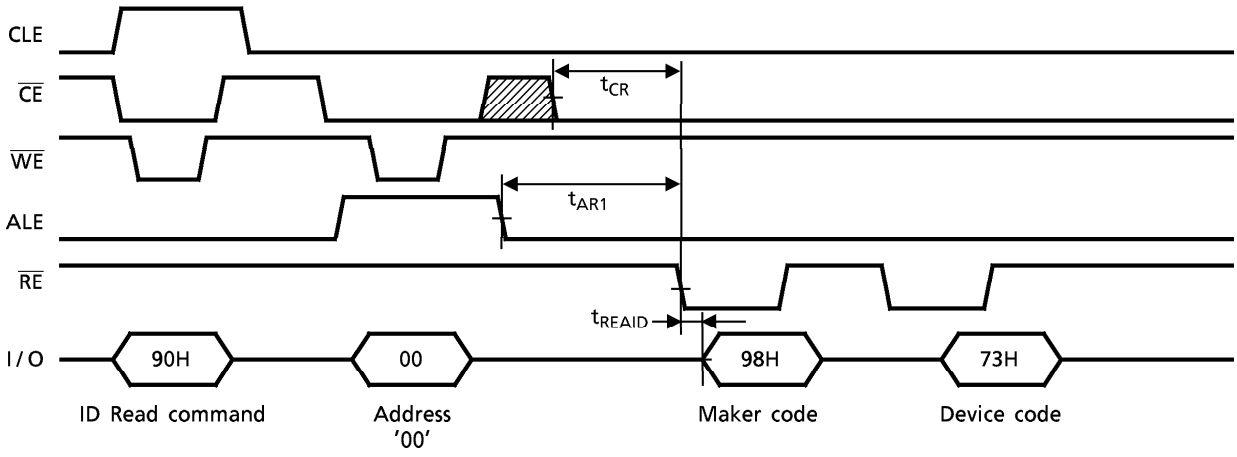
However, the following operation is prohibited. If the following operation is executed, set up for address and data register can not be guaranteed. (the Register may not be reset correctly)

⑥ When two or more Reset command are input in succession



ID Read

The TH58V128 contains ID codes which identify the device type and the manufacturer. The ID codes can be read out using the following timing conditions:



For the specification of the access times t_{REAID}, t_{CR} and t_{AR1} refer to the AC Characteristics.

Table 6. Code table

	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	HEX DATA
Maker code	1	0	0	1	1	0	0	0	98H
Device code	0	1	1	1	0	0	1	1	73H

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Data input as a command other than the specified commands in Table 3 is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(3) Pointer control for 00H, 01H, 50H

The device has three read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and figure 14 shows the block diagram of their operations.

Table 7. Pointer Destination

READ MODE	COMMAND	POINTER
(1)	00H	0 to 255
(2)	01H	256 to 511
(3)	50H	512 to 527

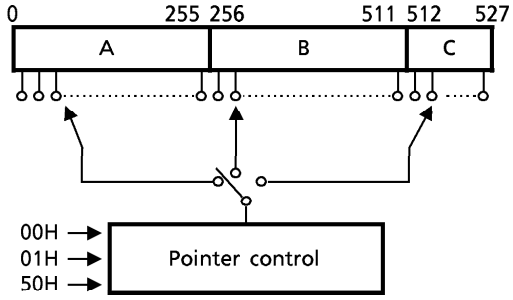
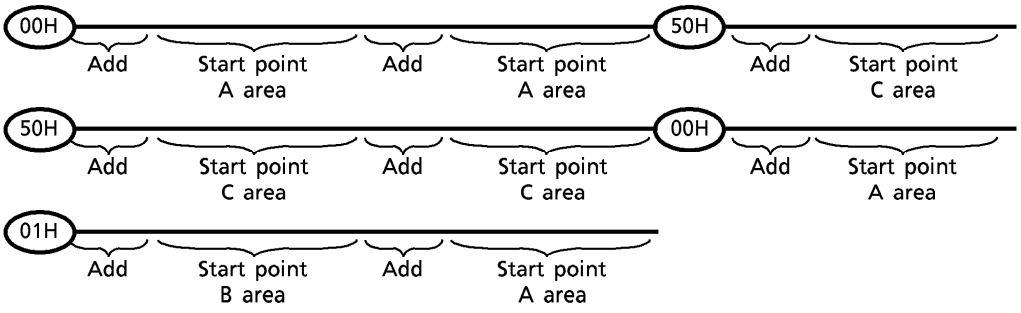


Figure 8. Pointer control

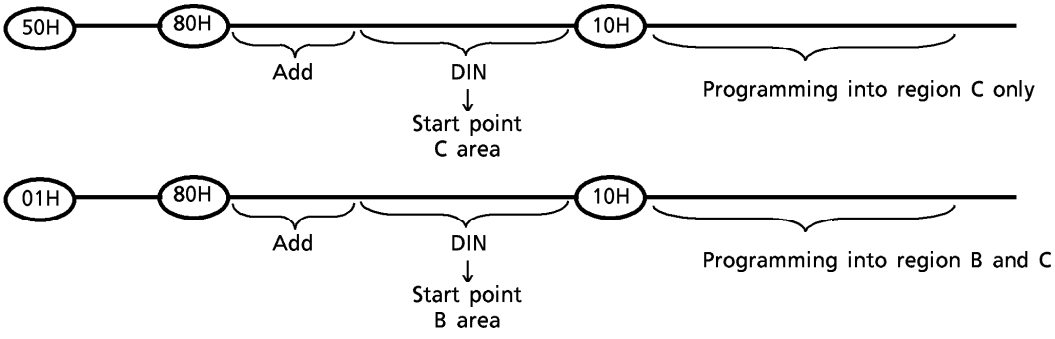
The pointer is set to region A by the 00H command, to region B by the 01H command, and to region C by the 50H command.

(Example)

The 00H command needs to be input to set the pointer back to region 'A' when the pointer points to region C.

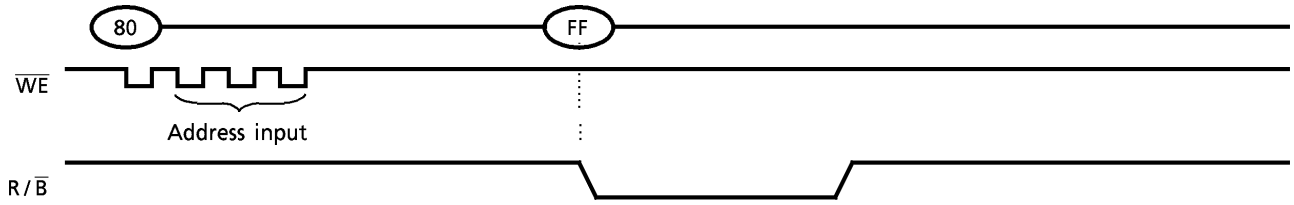


For programming into region C only, set the start point to region C with the 50H command.

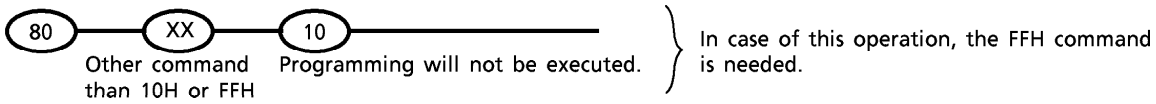


(4) Acceptable commands after Serial Input command 80H

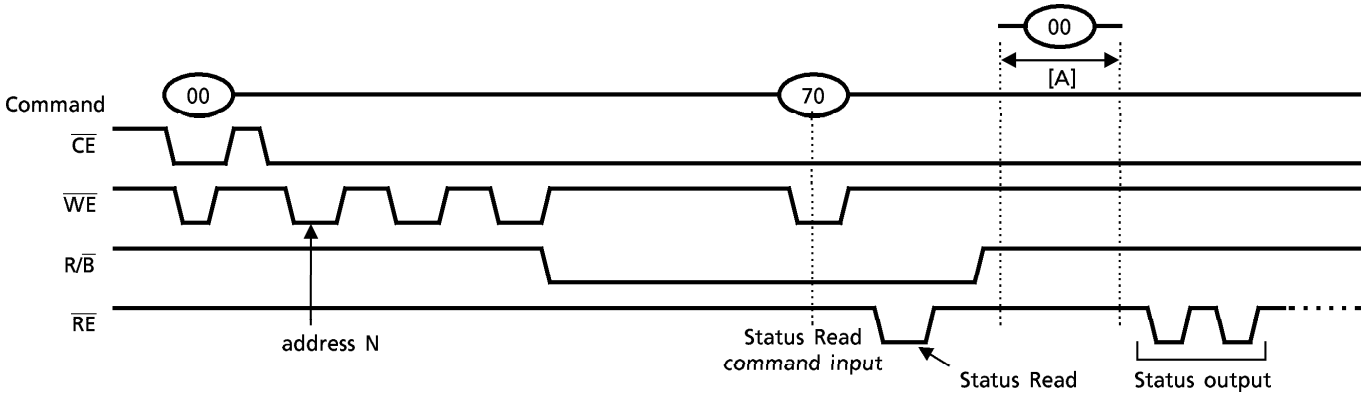
Once the Serial Input command (80H) has been input, do not input any command other than the Program Execution command 10H or the reset command FFH.



If a command other than 10H or FFH is input, the program operation is not performed.



(5) Status Read during the Read operation

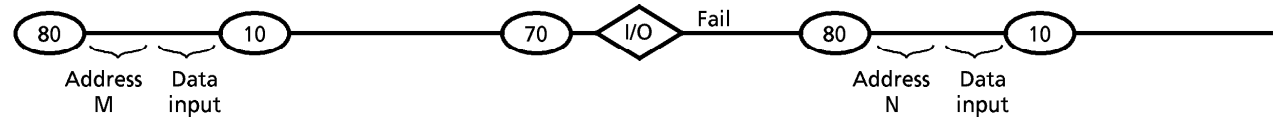


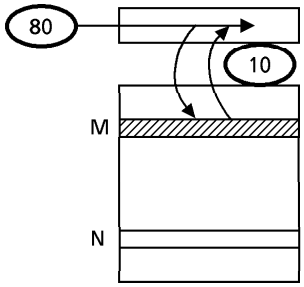
The device status can be read out by inputting the Status Read command (70H). Once the device has been set to the Status Read mode by the 70H command, the device will not return to Read mode.

Therefore, a Status Read during the Read mode is prohibited.

However, if the Read command (00H) is input during [A], the Status Read mode will be terminated, and the device will return to the Read mode. Then, data output will start from address N without address input.

(6) Auto programming failure



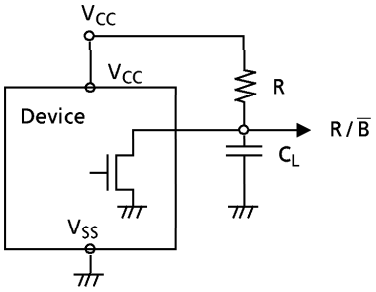


When the programming result for page address M is Fail, try to program the page to address N in another block. Because the previous input data is lost, the same sequence of 80H command, address and data input is necessary.

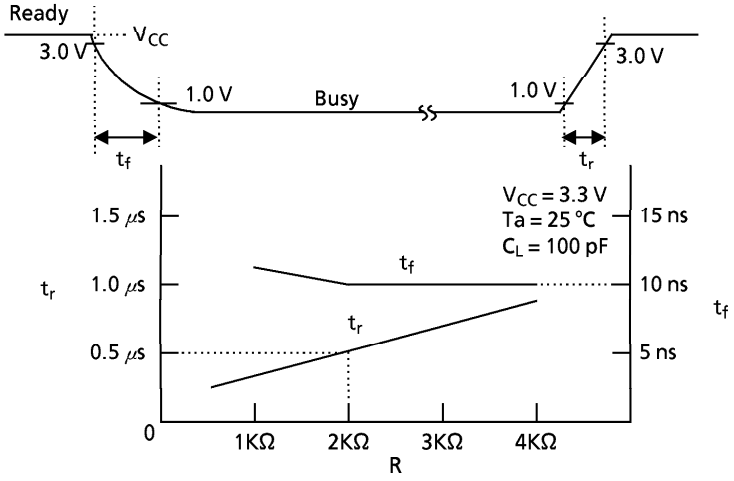
Figure 9.

(7) R/$\overline{B}$: termination for the Ready / Busy pin (R / $\overline{B}$)

A pull-up resistor needs to be used for termination because the R/$\overline{B}$ buffer consists of an open drain circuit.

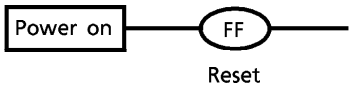


This data may vary by device.
We recommend that you use this data as a reference when selecting a resistor value.



(8) Status after Power On

The following sequence is necessary because same input signals may not be stable at power on.



(9) Power On / Off Sequence :

The $\overline{WP}$ signal is useful for protecting against data corruption at power on / off. The following timing sequence is necessary :

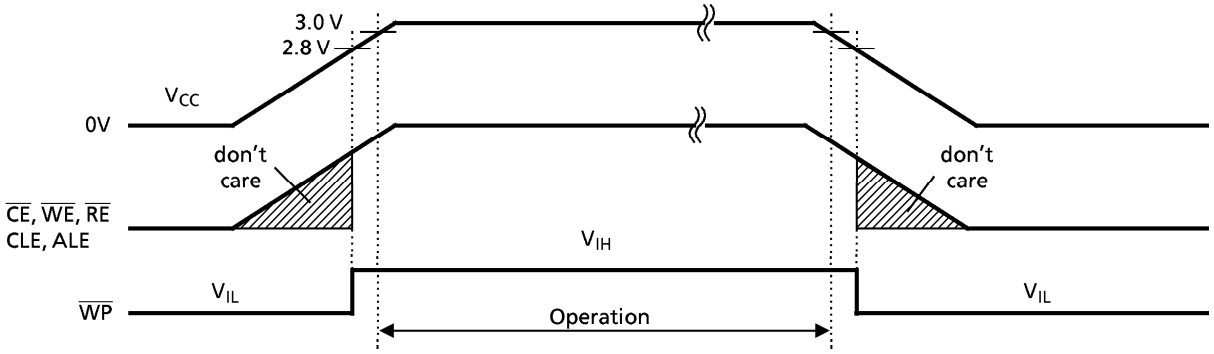
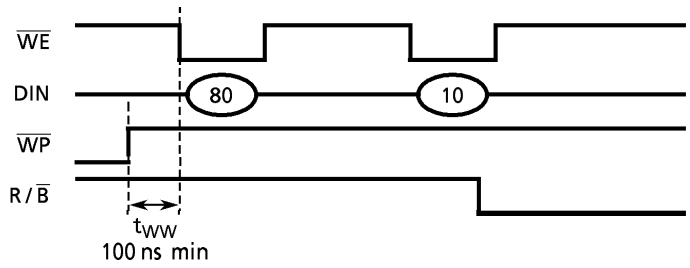


Figure 10. Power On / Off Sequence

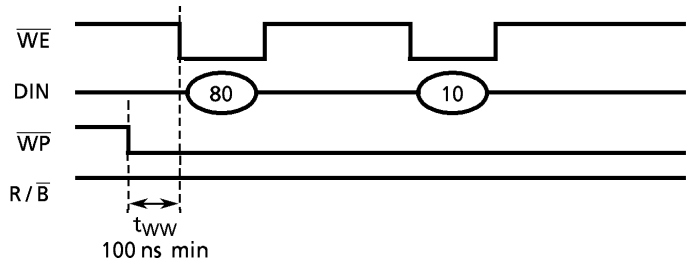
(10) Note regarding $\overline{WP}$ Signal

The Erase and Program operations are compulsively reset when $\overline{WP}$ goes Low. The Operations are enable and disable as follows :

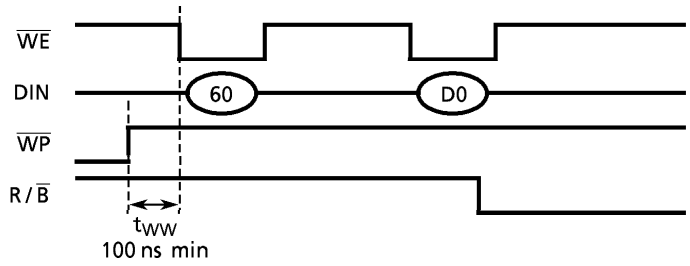
Enable Programming



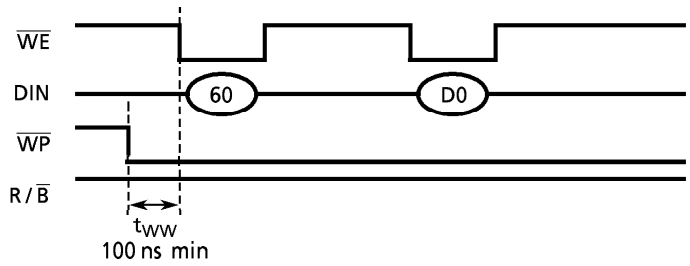
Disable Programming



Enable Erasing



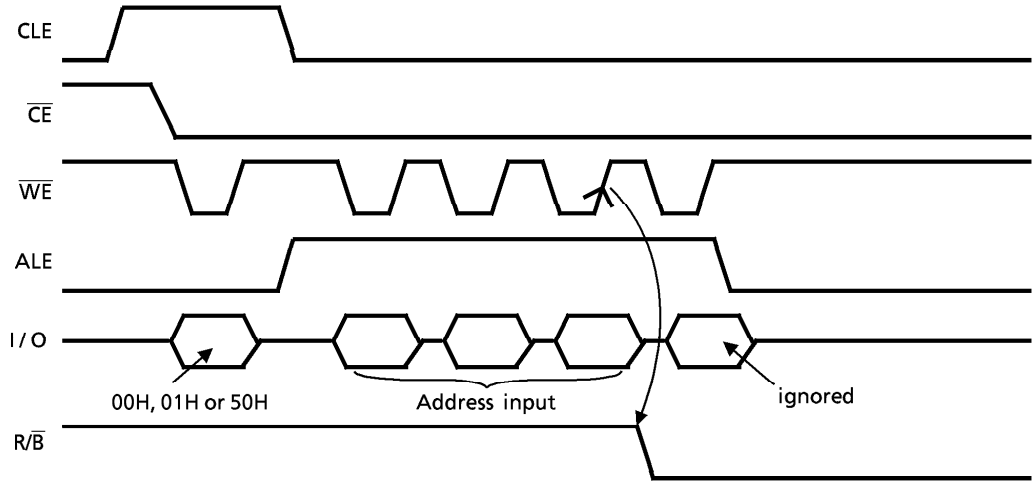
Disable Erasing



(11) When four address cycles are input

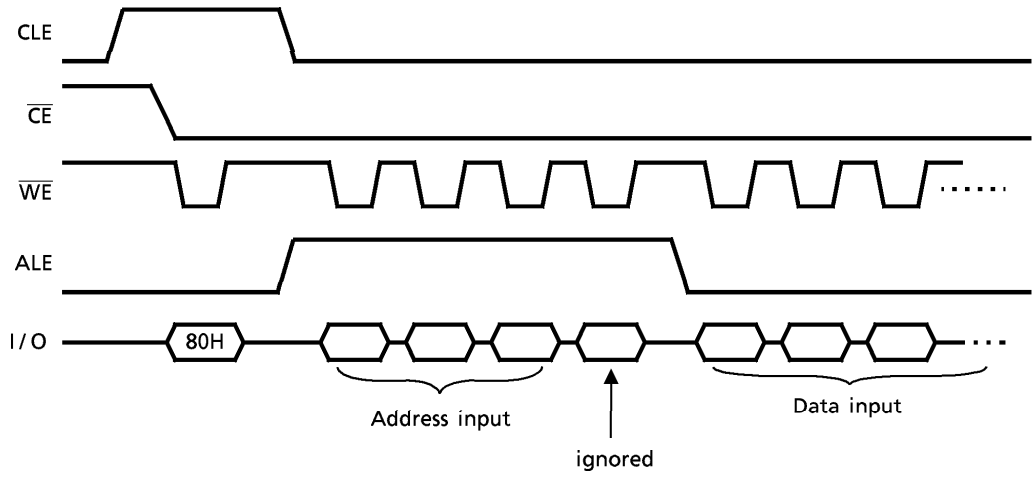
Although the device may acquire the fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when $\overline{WE}$ goes High in the third cycle.

Program operation



(12) Divided program in the same page (Partial page program)

The device allows a page to be divided into 10 segments (maximum) with each page segment programmed individually as follows:

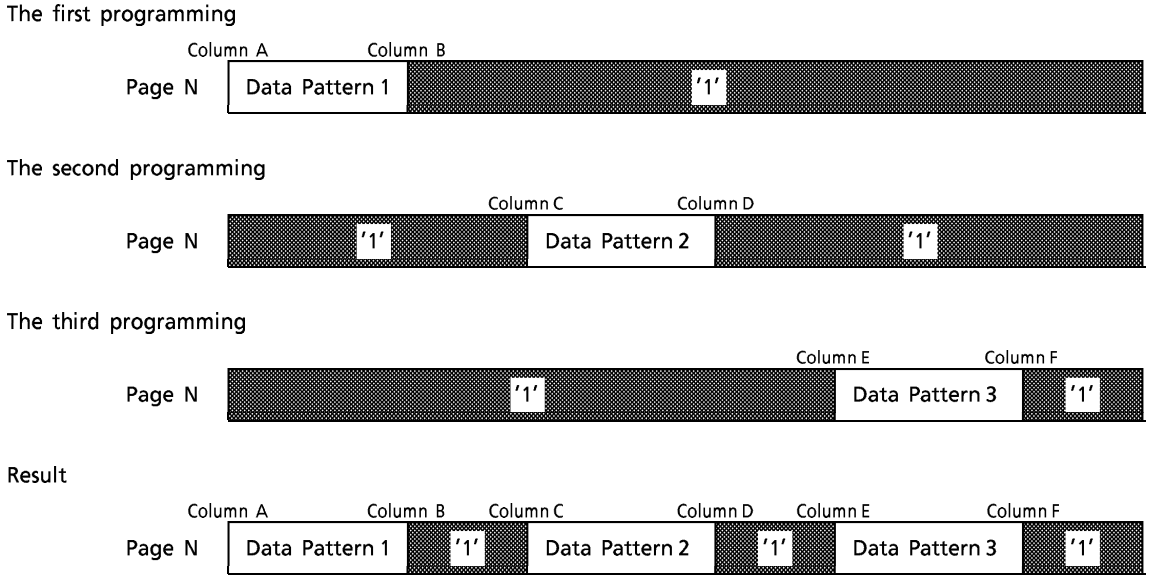
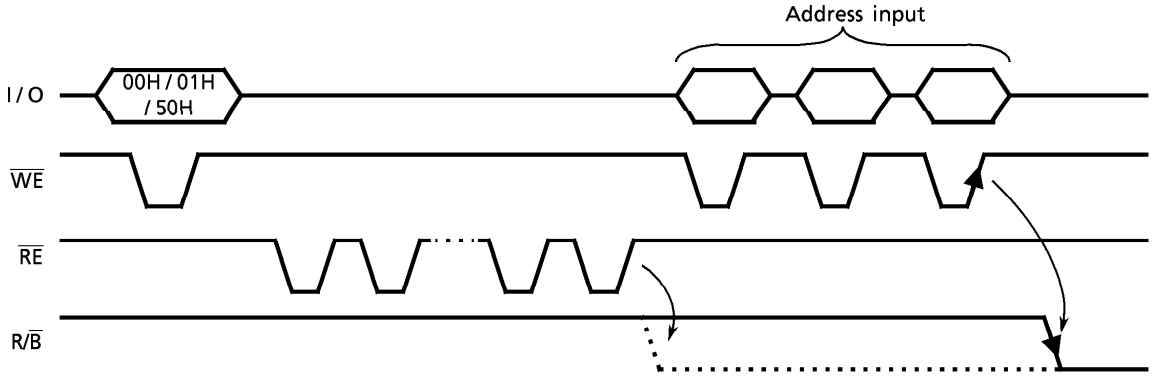


Figure 11.

Note: The input data for unprogrammed or previously programmed page segments must be '1'. (i.e. Mask all page bytes outside the segment to be programmed with '1' data.)

(13) Note regarding the $\overline{RE}$ Signal

The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in the read mode. Therefore, once the device has been set to read mode by a 00H, 01H or 50H command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of (before or after) the address input. Assuming that the $\overline{RE}$ clocks are inputted before address input and the pointer reaches the last column address, internal read operation (array → register) will occur and the device will be in Busy state.



Therefore, $\overline{RE}$ clocks must occur after the address input.

(14) Invalid block (bad block)

The device contains unusable blocks. Therefore, the following issues must be recognized:

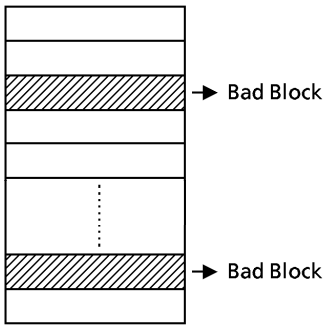


Figure. 12

Check if the device has any bad blocks after device installation into the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate.

The number of valid blocks is as follows:

Table 8.

	MIN	TYP	MAX	UNIT
Valid (Good) Block Number	1004	1016	1024	Block

Figure 14 shows the bad block test flow.

(15) Failure Phenomena for Program and Erase Operations.

The device may fail during program or erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Program Failure	Status Read after Prog. → Block Replacement
Single Bit*	Program Failure '1' → '0'	(1) Block Verify after Prog. → Retry
		(2) ECC

* : (1) or (2)

- ECC : Error Correcting code → Hamming Code etc.
  Example : 1 bit correction & 2 bit detection.
- Block Replacement

Program

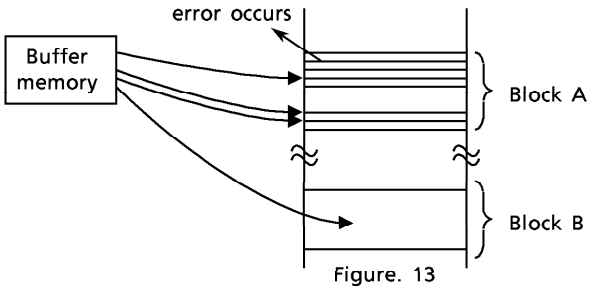


Figure. 13

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Erase

When an error occurs for an erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using other appropriate scheme).

BAD BLOCK TEST FLOW

C : Checker board pattern
$\overline{C}$: Invert checker board pattern
Blank check : 1 Block read (FFH)

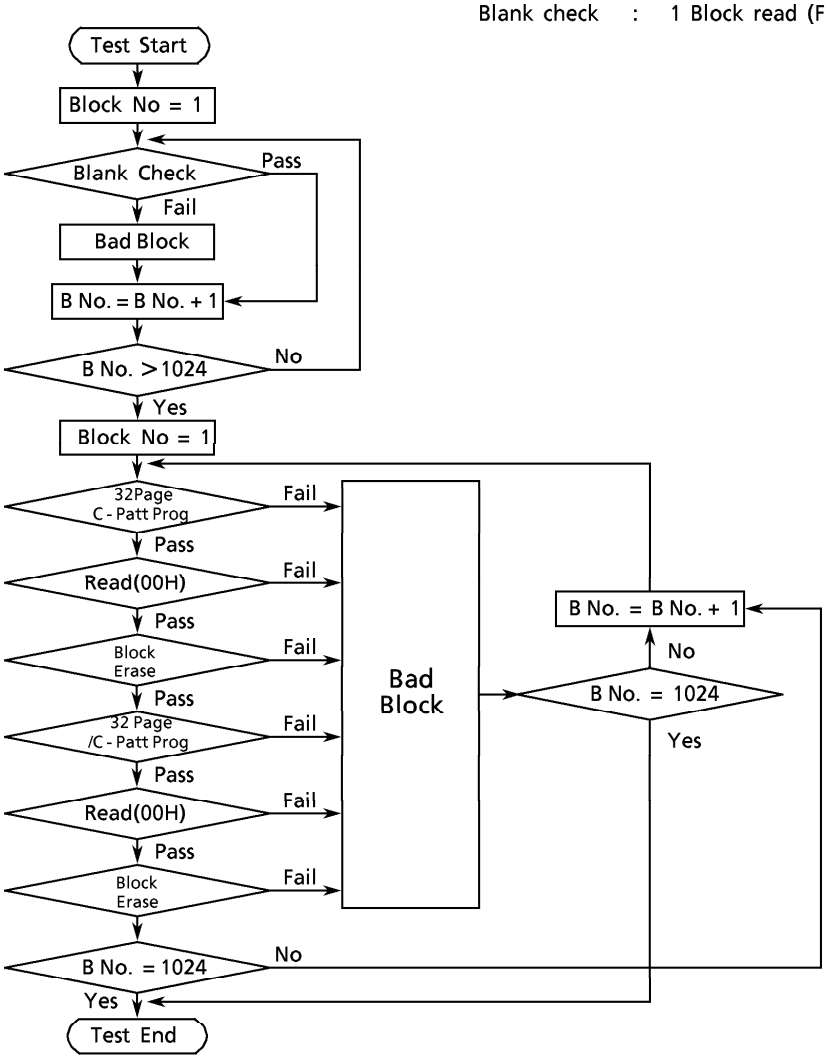


Figure 14.

PACKAGE DIMENSIONS

TSOPII44.40-P-400-0.80J

UNITS: mm