TOSHIBA e-MMC Module

8GB THGBM4G6D2HBAIR

INTRODUCTION

THGBM4G6D2HBAIR is 8-GByte density of e-MMC Module product housed in 153 ball BGA package. This unit utilizes advanced TOSHIBA NAND flash devices and a controller chip assembled as Multi Chip Module. THGBM4G6D2HBAIR has an industry standard MMC protocol for easy use.

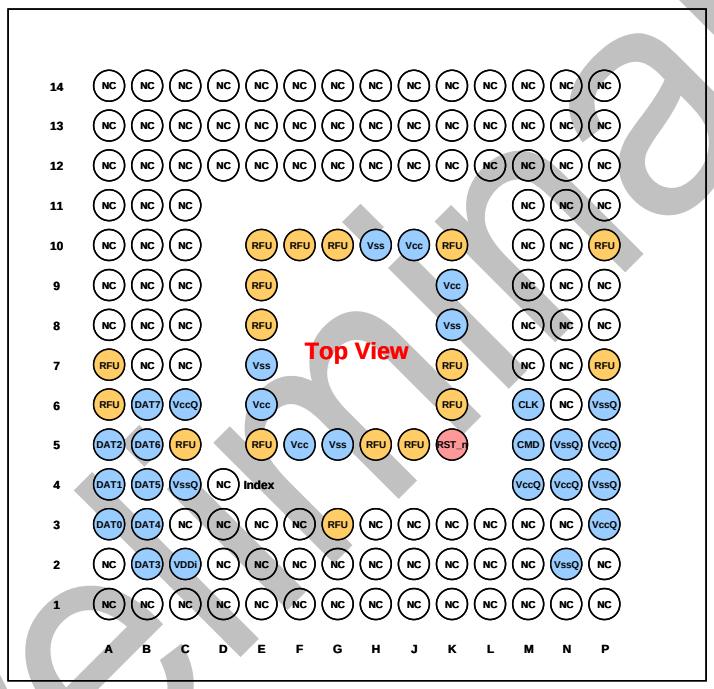
FEATURES

THGBM4G6D2HBAIR Interface

THGBM4G6D2HBAIR has the JEDEC/MMCA Version 4.41 interface with either 1-I/O, 4-I/O and 8-I/O mode support.

Ball / Signal Allocation

P-VFBGA153-1113-0.50-002FP(A) (11.5 x 13mm, H1.0mm max. package)



Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J10	Vcc	N4	VccQ
A4	DAT1	C4	VssQ	K5	RST_n	N5	VssQ
A5	DAT2	C6	VccQ	K8	Vss	P3	VccQ
B2	DAT3	E6	Vcc	K9	Vcc	P4	VssQ
B3	DAT4	E7	Vss	M4	VccQ	P5	VccQ
B4	DAT5	F5	Vcc	M5	CMD	P6	VssQ
B5	DAT6	G5	Vss	M6	CLK		
B6	DAT7	H10	Vss	N2	VssQ		

NC: No Connect, can be connected to ground or left floating.
RFU: Reserved for Future Use, should be left floating for future use.

Part Number

Available e-MMC Module Product – Part Number

TOSHIBA Part Number	Density	Package Size	NAND Flash Type	Weight
THGBM4G6D2HBAIR	8-GByte	11.5mm x 13.0mm x 1.0mm(max)	2 x 32Gbit MLC 24nm	235mg

Operating Temperature and Humidity Conditions

-25°C to +85°C, and 0%RH to 95%RH non-condensing

Storage Temperature and Humidity Conditions

-40°C to +85°C, and 0%RH to 95%RH non-condensing

Performance

52MHz / x8 mode / Sequential Access (2MByte Access Size)

TOSHIBA Part Number	Density	NAND Flash Type	Interleave Operation	Mode	Typ. Performance [MB/sec]	
					Read	Write
THGBM4G6D2HBAIR	8-GByte	2 x 32Gbit MLC 24nm	Interleave	SDR	47 (TBD)	27 (TBD)
				DDR	78 (TBD)	27 (TBD)

Power Supply

Vcc = 2.7V to 3.6V, VccQ = 1.65V to 1.95V / 2.7V to 3.6V

Operating Current (RMS)

TOSHIBA Part Number	Density	NAND Flash Type	Interleave Operation	Mode	Max Operating Current [mA]
THGBM4G6D2HBAIR	8-GByte	2 x 32Gbit MLC 24nm	Interleave	SDR	100 (TBD)
				DDR	130 (TBD)

The measurement for max RMS current is done as average RMS current consumption over a period of 100ms

Sleep Mode Current

TOSHIBA Part Number	Density	NAND Flash Type	Interleave Operation	Iccqs [uA]		Iccqs+Iccs [uA]	
				Typ. *1	Max. *2	Typ. *1	Max. *2
THGBM4G6D2HBAIR	8-GByte	2 x 32Gbit MLC 24nm	Interleave	75 (TBD)	280 (TBD)	115 (TBD)	380 (TBD)

*1 : The conditions of typical values are 25°C, and VccQ = 3.3V or 1.8V.
*2 : The conditions of maximum values are 85°C, and VccQ = 3.6V or 1.95V.

Product Architecture

The diagram in Figure 1 illustrates the main functional blocks of the THGBM4G6D2HBAIR.
Specification of the C_{REG} and recommended values of the C_{VCC}, and C_{VCCQ} in the Figure 1 are as follows.

Parameter	Symbol	Unit	Min.	Typ.	Max.
V_{DDi} capacitor value	C_{REG}	µF	0.10*	-	1.00
V_{CC} capacitor value	C_{VCC}	µF	-	2.2 + 0.1	-
V_{CCQ} capacitor value	C_{VCCQ}	µF	-	2.2 + 0.1	-

* Toshiba recommends that the minimum value should be usually applied as the value of C_{REG}.
C_{REG} shall be compliant with X5R/X7R of EIA standard or B of JIS standard.

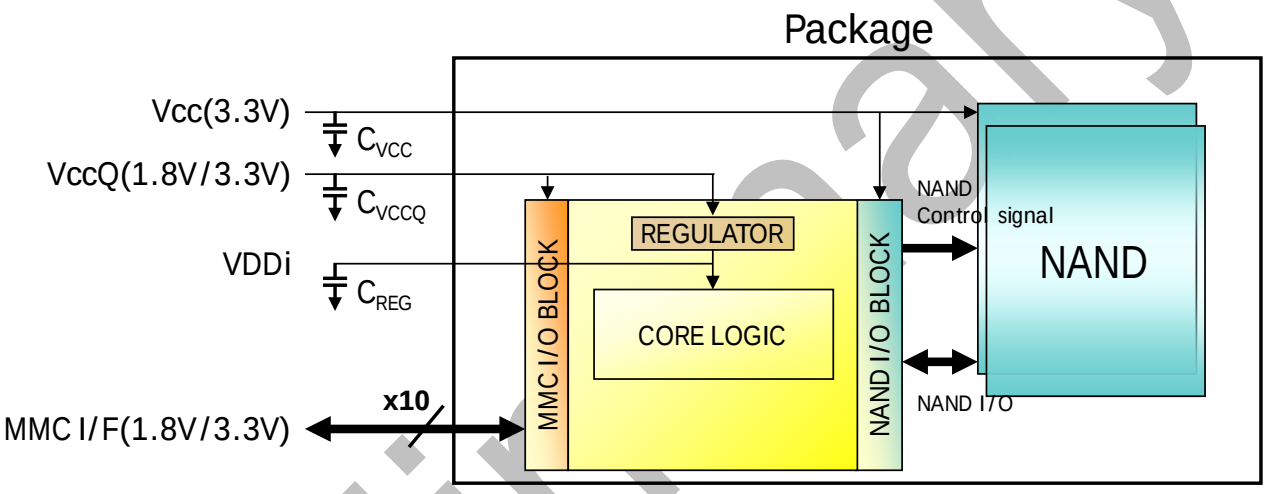
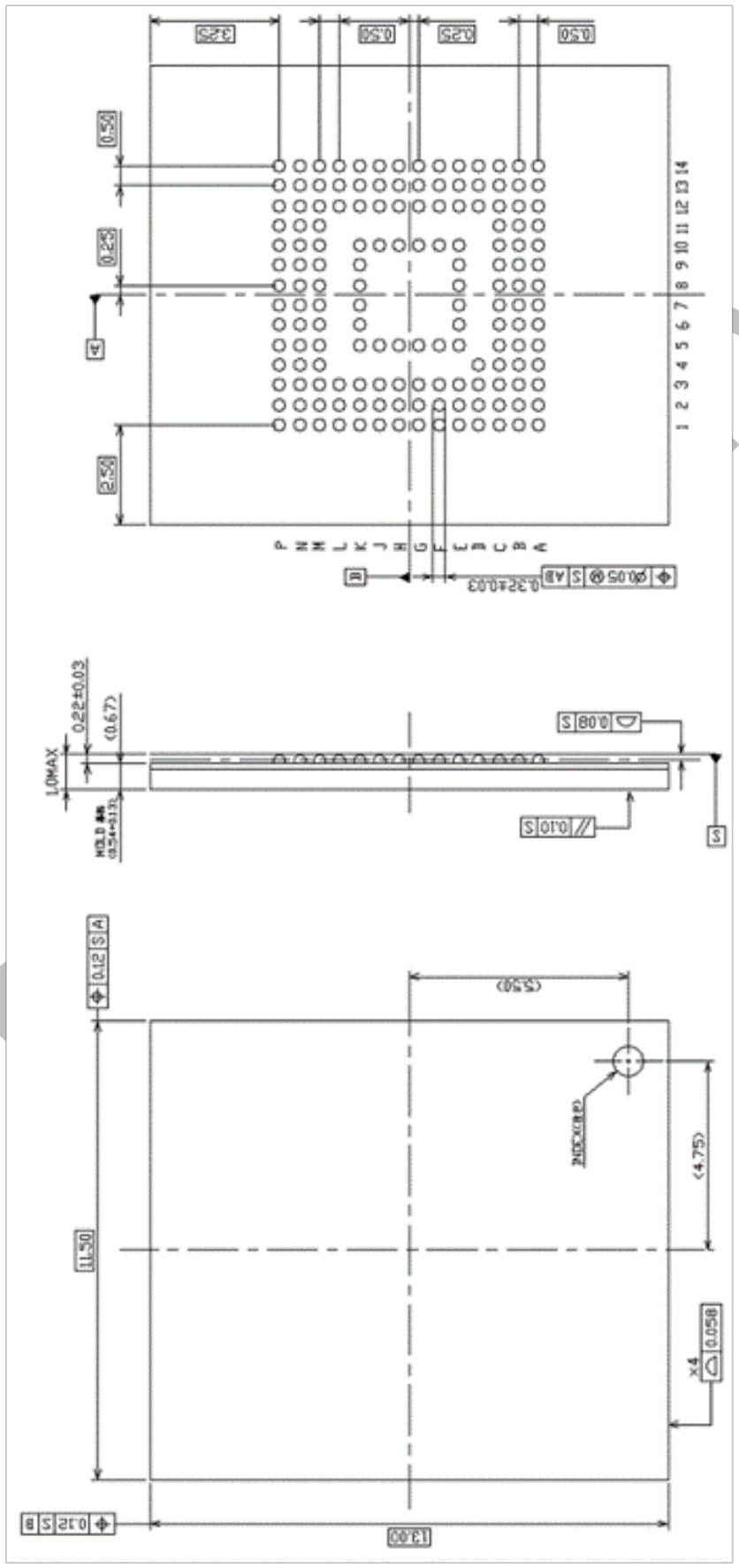


Figure 1 THGBM4G6D2HBAIR Block Diagram

PRODUCT SPECIFICATIONS

Package Dimensions

P-VFBGA153-1113-0.50-002FP(A) (11.5 x 13mm, H1.0mm max. package)



Density Specifications

TOSHIBA Part Number	Density	Interleave Operation	User Area Density [Bytes]	SEC_COUNT in Extended CSD
THGBM4G6D2HBAIR	8-Gbyte	Interleave	7,952,400,384	0x00ED0000

1) User area density shall be reduced if enhanced user data area is defined.

Register Informations

OCR Register

OCR bit	VDD Voltage window	Value
[6:0]	Reserved	000 0000b
[7]	1.70-1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b
[31]	(card power up status bit (busy))[1]	

1) This bit is set to LOW if the card has not finished the power up routine.

CID Register

CID-slice	Name	Field	Width	Value
[127:120]	Manufacturer ID	MID	8	0001 0001b
[119:114] *	Reserved	-	6	0b
[113:112] *	Card/BGA	CBX	2	01b
[111:104] *	OEM/Application ID	OID	8	0b
[103:56]	Product name	PNM	48	0x30 30 38 47 34 42 (008G4B)
[55:48]	Product revision	PRV	8	0x00
[47:16]	Product serial	PSN	32	Serial number
[15:8]	Manufacturing date	MDT	8	see-JEDEC Specification
[7:1]	CRC7 checksum	CRC	7	CRC7
[0]	Not used, always '1'	-	1	1b

CSD Register

CSD-slice	Name	Field	Width	Cell Type	Value
[127:126]	CSD structure	CSD_STRUCTURE	2	R	0x3
[125:122]	System specification version	SPEC_VERS	4	R	0x4
[121:120]	Reserved	-	2	R	0x0
[119:112]	Data read access-time 1	TAAC	8	R	0x0E
[111:104]	Data read access-time 2 in CLK cycles (NSAC * 100)	NSAC	8	R	0x00
[103:96]	Max. bus clock frequency	TRAN_SPEED	8	R	0x32
[95:84]	Card command classes	CCC	12	R	0x0F5
[83:80]	Max. read data block length	READ_BL_LEN	4	R	0x9
[79]	Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0x0
[78]	Write block misalignment	WRITE_BLK_MISALIGN	1	R	0x0
[77]	Read block misalignment	READ_BLK_MISALIGN	1	R	0x0
[76]	DSR implemented	DSR_IMP	1	R	0x0
[75:74]	Reserved	-	2	R	0x0
[73:62]	Device size	C_SIZE	12	R	0xFFF
[61:59]	Max. read current @ VDD min.	VDD_R_CURR_MIN	3	R	0x7
[58:56]	Max. read current @ VDD max.	VDD_R_CURR_MAX	3	R	0x7
[55:53]	Max. write current @ VDD min.	VDD_W_CURR_MIN	3	R	0x7
[52:50]	Max. write current @ VDD max.	VDD_W_CURR_MAX	3	R	0x7
[49:47]	Device size multiplier	C_SIZE_MULT	3	R	0x7
[46:42]	Erase group size	ERASE_GRP_SIZE	5	R	0x1F
[41:37]	Erase group size multiplier	ERASE_GRP_MULT	5	R	0x1F
[36:32]	Write protect group size	WP_GRP_SIZE	5	R	0x07
[31]	Write protect group enable	WP_GRP_ENABLE	1	R	0x1
[30:29]	Manufacturer default ECC	DEFAULT_ECC	2	R	0x0
[28:26]	Write speed factor	R2W_FACTOR	3	R	0x5
[25:22]	Max. write data block length	WRITE_BL_LEN	4	R	0x9
[21]	Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0x0
[20:17]	Reserved	-	4	R	0x0
[16]	Content protection application	CONTENT_PROT_APP	1	R	0x0
[15]	File format group	FILE_FORMAT_GRP	1	R/W	0x0
[14]	Copy flag (OTP)	COPY	1	R/W	0x0
[13]	Permanent write protection	PERM_WRITE_PROTECT	1	R/W	0x0
[12]	Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	0x0
[11:10]	File format	FILE_FORMAT	2	R/W	0x0
[9:8]	ECC code	ECC	2	R/W/E	0x0
[7:1]	CRC	CRC	7	R/W/E	CRC
[0]	Not used, always ‘1’	-	1	-	0x1

Extended CSD Register

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[511:505]	Reserved	-	7	-	All '0'
[504]	Supported Command Sets	S_CMD_SET	1	R	0x00
[503]	HPI features	HPI_FEATURES	1	R	0x01
[502]	Background operations support	BKOPS_SUPPORT	1	R	0x01
[501:247]	Reserved	-	255	-	All '0'
[246]	Background operations status	BKOPS_STATUS	1	R	0x00
[245:242]	Number of correctly programmed sectors	CORRECTLY _PRG_SECTORS_NUM	4	R	0x00000000
[241]	1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	0x1E
[240]	Reserved	-	1	-	0x00
[239]	Power class for 52MHz, DDR @ 3.6V	PWR_CL_DDR_52_360	1	R	0x22 (TBD)
[238]	Power class for 52MHz, DDR @ 1.95V	PWR_CL_DDR_52_195	1	R	0x66 (TBD)
[237:236]	Reserved	-	2	-	All '0'
[235]	Minimum Write Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	0x00
[234]	Minimum Read Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	0x50 (TBD)
[233]	Reserved	-	1	-	0x00
[232]	TRIM Multiplier	TRIM_MULT	1	R	0x04
[231]	Secure Feature support	SEC_FEATURE_SUPPORT	1	R	0x15
[230]	Secure Erase Multiplier	SEC_ERASE_MULT	1	R	0x10
[229]	Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	0x42
[228]	Boot information	BOOT_INFO	1	R	0x07
[227]	Reserved	-	1	R	0x00
[226]	Boot partition size	BOOT_SIZE_MULTI	1	R	0x10
[225]	Access size	ACC_SIZE	1	R	0x07
[224]	High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	0x08
[223]	High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	0x02
[222]	Reliable write sector count	REL_WR_SEC_C	1	R	0x10
[221]	High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	0x01
[220]	Sleep current (Vcc)	S_C_VCC	1	R	0x07 (TBD)
[219]	Sleep current (VccQ)	S_C_VCCQ	1	R	0x09
[218]	Reserved	-	1	-	0x00
[217]	Sleep/awake timeout	S_A_TIMEOUT	1	R	0x11
[216]	Reserved	-	1	-	0x00
[215:212]	Sector Count	SEC_COUNT	4	R	0x00ED0000
[211]	Reserved	-	1	-	0x00
[210]	Minimum Write Performance for 8bit @ 52MHz	MIN_PERF_W_8_52	1	R	0x00
[209]	Minimum Read Performance 8bit @ 52MHz	MIN_PERF_R_8_52	1	R	0x64 (TBD)

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[208]	Minimum Write Performance for 8bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0x00
[207]	Minimum Read Performance for 8 bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	0x3C (TBD)
[206]	Minimum Write Performance for 4bit @ 26MHz	MIN_PERF_W_4_26	1	R	0x00
[205]	Minimum Read Performance for 4bit @ 26MHz	MIN_PERF_R_4_26	1	R	0x1E (TBD)
[204]	Reserved	-	1	-	0x00
[203]	Power class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	0x00 (TBD)
[202]	Power class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	0x00 (TBD)
[201]	Power class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	0x44 (TBD)
[200]	Power class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	0x44 (TBD)
[199]	Partition switching timing	PARTITION_SWITCH_TIME	1	R	0x01
[198]	Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	0x05
[197]	Reserved	-	1	-	0x00
[196]	Card Type	CARD_TYPE	1	R	0x07
[195]	Reserved	-	1	-	0x00
[194]	CSD structure version	CSD_STRUCTURE	1	R	0x02
[193]	Reserved	-	1	-	0x00
[192]	Extended CSD revision	EXT_CSD_REV	1	R	0x05
[191]	Command Set	CMD_SET	1	R/W/E_P	0x00
[190]	Reserved	-	1	-	0x00
[189]	Command set revision	CMD_SET_REV	1	R	0x00
[188]	Reserved	-	1	-	0x00
[187]	Power class [1]	POWER_CLASS	1	R/W/E_P	0x00
[186]	Reserved	-	1	-	0x00
[185]	High-speed interface timing	HS_TIMING	1	R/W/E_P	0x00
[184]	Reserved		1	-	0x00
[183]	Bus width mode	BUS_WIDTH	1	W/E_P	0x00
[182]	Reserved	-	1	-	0x00
[181]	Erased memory content	ERASED_MEM_CONT	1	R	0x01
[180]	Reserved	-	1	-	0x00
[179]	Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	0x00
[178]	Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	0x00
[177]	Boot bus width	BOOT_BUS_WIDTH	1	R/W/E	0x00
[176]	Reserved	-	1	-	0x00
[175]	High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	0x00
[174]	Reserved	-	1	-	0x00
[173]	Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	0x00
[172]	Reserved	-	1	-	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[171]	User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	0x00
[170]	Reserved	-	1	-	0x00
[169]	FW configuration	FW_CONFIG	1	R/W	0x00
[168]	RPMB Size	RPMB_SIZE_MULT	1	R	0x02
[167]	Write reliability setting register	WR_REL_SET	1	R/W	0x00
[166]	Write reliability parameter register	WR_REL_PARAM	1	R	0x05
[165]	Reserved	-	1	-	0x00
[164]	Manually start background operations	BKOPS_START	1	W/E_P	0x00
[163]	Enable background operations handshake	BKOPS_EN	1	R/W	0x00
[162]	H/W reset function	RST_n_FUNCTION	1	R/W	0x00
[161]	HPI management	HPI_MGMT	1	R/W/E_P	0x00
[160]	Partitioning Support	PARTITIONING_SUPPORT	1	R	0x03
[159:157]	Max Enhanced Area Size [2]	MAX_ENH_SIZE_MULT	3	R	0x0003B4
[156]	Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	0x00
[155]	Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	0x00
[154:143]	General Purpose Partition Size [3]	GP_SIZE_MULT	12	R/W	0x00
[142:140]	Enhanced User Data Area Size [4]	ENH_SIZE_MULT	3	R/W	0x00
[139:136]	Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	0x00
[135]	Reserved	-	1	-	0x00
[134]	Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	0x00
[133:0]	Reserved	-	134	-	All '0'

1) Although POWER_CLASS [187] Field can be re-written by host, e-MMC does not support any power budget management.

2) Max Enhanced Area Size (MAX_ENH_SIZE_MULT [159:157]) has to be calculated by following formula.

Max Enhanced Area = MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GPR_SIZE x 512kBytes

$$\sum_{i=1}^{4} \text{Enhanced general partition size}(i) + \text{Enhanced user data area} \le \text{Max enhanced area}$$

3) General Purpose Partition Size (GP_SIZE_MULT_GP0 - GP_SIZE_MULT_GP3 [154:143]) has to be calculated by following formula.

General_Purpose_Partition_X Size = (GP_SIZE_MULT_X_2 x 2^{16} + GP_SIZE_MULT_X_1 x 2^{8} + GP_SIZE_MULT_X_0 x 2^{0}) x HC_WP_GRP_SIZE x HC_ERASE_GPR_SIZE x 512kBytes

4) Enhanced User Data Area Size (ENH_SIZE_MULT [142:140]) has to be calculated by following formula.

Enhanced User Data Area x Size = (ENH_SIZE_MULT_2 x 2^{16} + ENH_SIZE_MULT_1 x 2^{8} + ENH_SIZE_MULT_0 x 2^{0}) x HC_WP_GRP_SIZE x HC_ERASE_GPR_SIZE x 512kBytes

ELECTRICAL CHARACTERISTICS

DC Characteristics

General

Parameter	Symbol	Test Conditions	Min	Max	Unit
Peak voltage on all lines			-0.5	VccQ+0.5	V
All Inputs					
Input Leakage Current (before initialization sequence[1] and/or the internal pull up resistors connected)			-100	100	uA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)			-10	10	uA
All Outputs					
Output Leakage Current (before initialization sequence)			-100	100	uA
Output Leakage Current (after initialization sequence)			-10	10	uA

1) Initialization sequence is defined in Section 12.3 of JEDEC/MMCA Standard 4.4

Power Supply Voltage

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage 1	V_{CC}		2.7	3.6	V
Supply voltage 2	VccQ		1.65	1.95	V
			2.7	3.6	V
Supply power-up for 3.3V	tPRUH			35	ms
Supply power-up for 1.8V	tPRUL			25	ms

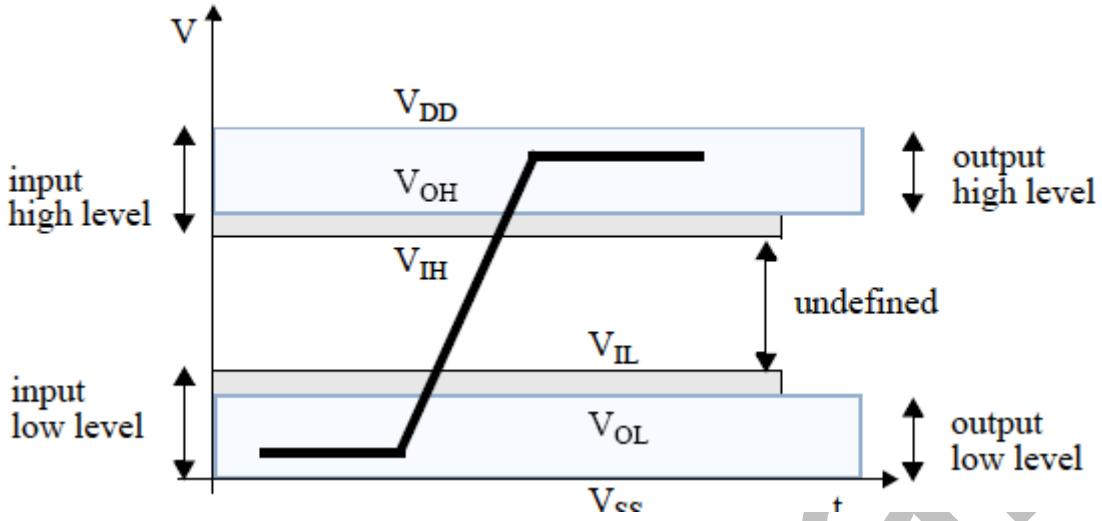
Supply Current

Parameter		Symbol	Interleave Operation	Mode	Min	Max	Unit
Operation (RMS)	Read	I_{ROP}	Interleave	SDR	—	90 (TBD)	mA
				DDR	—	130 (TBD)	mA
	Write	I_{WOP}	Interleave	SDR	—	120 (TBD)	mA
				DDR	—	130 (TBD)	mA

Internal resistance and Device capacitance

Parameter	Symbol	Test Conditions	Min	Max	Unit
Single device capacitance	C_{CARD}		—	9	pF
Internal pull up resistance DAT1 – DAT7	R_{INT}		10	150	kOhm

Bus Signal Levels



Open-Drain Mode Bus Signal Level

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -100uA	VccQ - 0.2	—	V
Output LOW voltage	V_{OL}	I_{OL} = 2mA	—	0.3	V

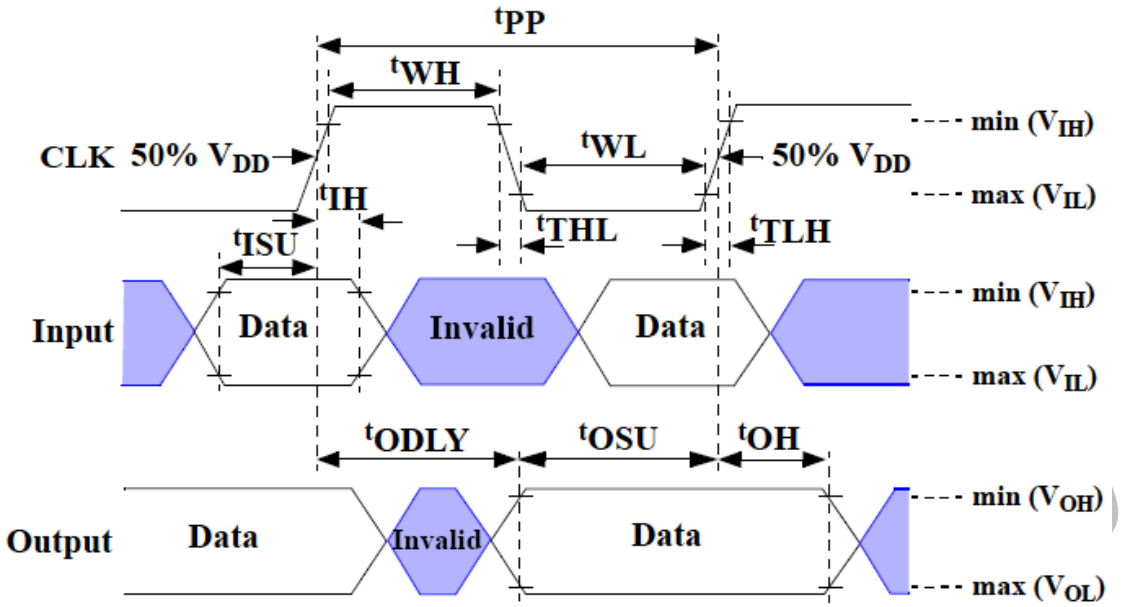
Push-Pull Mode Bus Signal Level (High-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -100uA @ $V_{DD\ min}$	0.75 * VccQ	—	V
Output LOW voltage	V_{OL}	I_{OL} = 100uA @ $V_{DD\ min}$	—	0.125 * VccQ	V
Input HIGH voltage	V_{IH}		0.625* VccQ	VccQ + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.25 * VccQ	V

Push-Pull Mode Bus Signal Level (Dual-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -2mA @ $V_{DD\ min}$	VccQ - 0.45	—	V
Output LOW voltage	V_{OL}	I_{OL} = 2mA @ $V_{DD\ min}$	—	0.45	V
Input HIGH voltage	V_{IH}		0.65 * VccQ	VccQ + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.35 * VccQ	V

Bus Signal Levels



Data must always be sampled on the rising edge of the clock.

Card Interface Timings (High-speed interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	f_{pp} (=1/tPP)	C_L <= 30pF Tolerance: +100KHz	0	52	MHz
Clock frequency Identification Mode (OD)	f_{OD}	Tolerance: +20KHz	0	400	KHz
Clock High time	t_{WH}	C_L <= 30pF	6.5	—	ns
Clock low time	t_{WL}	C_L <= 30pF	6.5	—	ns
Clock rise time	t_{TLH}	C_L <= 30pF	—	3	ns
Clock fall time	t_{THL}	C_L <= 30pF	—	3	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t_{ISU}	C_L <= 30pF	3	—	ns
Input hold time	t_{IH}	C_L <= 30pF	3	—	ns
Outputs CMD,DAT (referenced to CLK)					
Output Delay time during Data Transfer	t_{ODLY}	C_L <= 30pF	—	13.7	ns
Output hold time	t_{OH}	C_L <= 30pF	2.5	—	ns
Signal rise time [4]	t_{rise}	C_L <= 30pF	—	3	ns
Signal fall time	t_{fall}	C_L <= 30pF	—	3	ns

1) CLK timing is measured at 50% of VccQ
2) THGBM4G6D2HBAIR shall support the full frequency range from 0-26MHz, or 0-52MHz
3) e-MMC can operate as high-speed interface timing at 26MHz clock frequency.
4) CLK rise and fall times are measured by min(VIH) and max(VIL).
5) Inputs CMD,DAT rise and fall times area measured by min(VIH) and max(VIL), and outputs CMD, DAT rise and fall times are measured by min(VOH) and max(VOL).

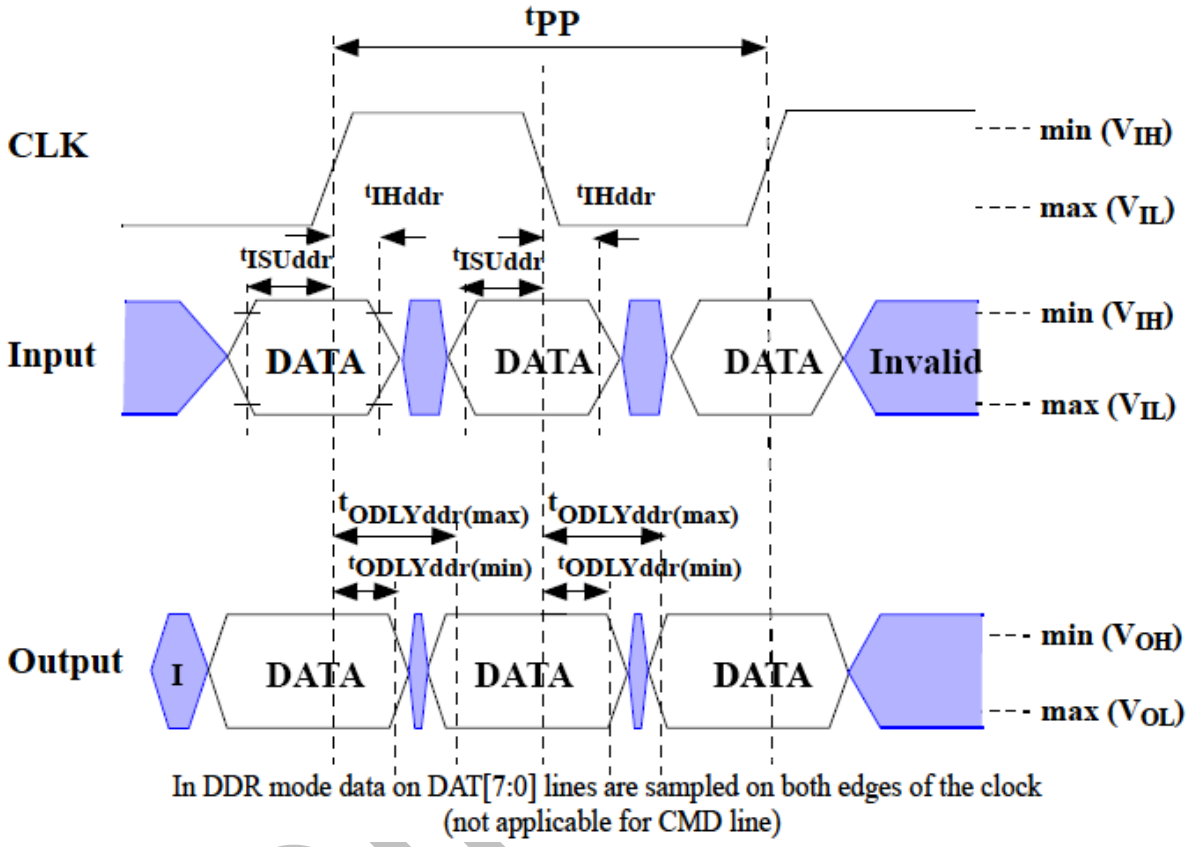
Card Interface Timings (Backward-compatible interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	f_{pp} (=1/tPP)	C_L <= 30pF	0	26	MHz
Clock frequency Identification Mode (OD)	f_{OD}	Tolerance: +20KHz	0	400	KHz
Clock high time	t_{WH}	C_L <= 30pF	10	—	ns
Clock low time	t_{WL}	C_L <= 30pF	10	—	ns
Clock rise time	t_{TLH}	C_L <= 30pF	—	10	ns
Clock fall time	t_{THL}	C_L <= 30pF	—	10	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t_{ISU}	C_L <= 30pF	3	—	ns
Input hold time	t_{IH}	C_L <= 30pF	3	—	ns
Outputs CMD,DAT (referenced to CLK)					
Output set-up time [5]	t_{OSU}	C_L <= 30pF	11.7	—	ns
Output hold time [5]	t_{OH}	C_L <= 30pF	8.3	—	ns

1) The e-MMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VccQ
3) For compatibility with e-MMCs that support the v4.2 standard or earlier, host should not use >20MHz before switching to high-speed interface timing.
4) CLK rise and fall times are measured by min(VIH) and max(VIL).
5) tOSU and tOH are defined as values from clock rising edge. However, the e-MMC device will utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set tWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for the device.

Bus Timing for DAT signals for during 2x data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. the CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in High-speed interface timing or Backward-compatible interface timing.



In DDR mode data on DAT[7:0] lines are sampled on both edges of the clock (not applicable for CMD line)

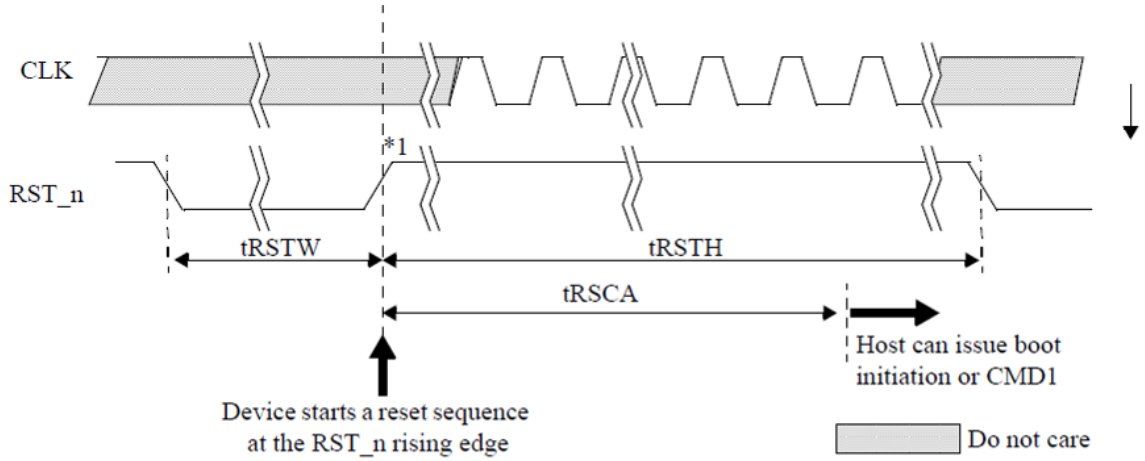
High-speed dual data rate interface timings

Parameter	Symbol	Min	Max	Unit	Remark [1]
Input CLK [1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUddr}	2.5	—	ns	CL ≤ 15pF
Input hold time	t_{IHddr}	2.5	—	ns	CL ≤ 15pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	CL ≤ 15pF
Signal rise time (all signals) [2]	t_{RISE}	—	2	ns	CL ≤ 15pF
Signal fall time (all signals)	t_{FALL}	—	2	ns	CL ≤ 15pF

1) CLK timing is measured at 50% of VccQ.

2) Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

H/W Reset Operation



(Note) *1 : Device will detect the rising edge of RST_n signal to trigger internal reset sequence

H/W Reset Timings

Parameter	Symbol	Test Conditions	Min	Max	Unit
RST_n pulse width	tRSTW		1	—	us
RST_n to Command time	tRSCA		200 [1]	—	us
RST_n high period (interval time)	tRSTH		1	—	us

1) 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA

Functional restrictions

TBD, If necessary.

Reliability Guidance

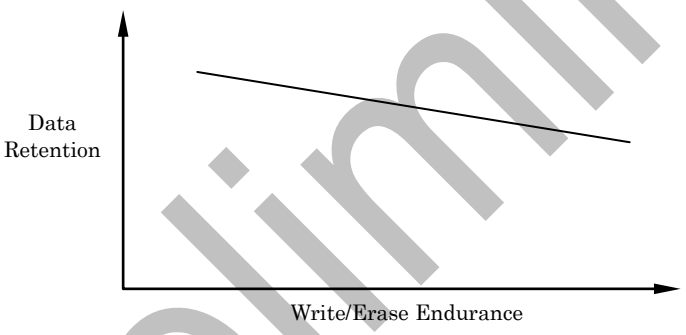
This reliability guidance is intended to notify some guidance related to using raw MLC NAND flash. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

-Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

-Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Also write/erase endurance deteriorates data retention capability. The figure below shows a generic trend of relationship between write/erase endurance and data retention.



-Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Considering the above failure modes, TOSHIBA recommends following usage:

- Please avoid any excessive iteration of resets and initialization sequences (card identification mode) as far as possible after power-on, which may result in read disturb failure. The resets include hardware resets and software resets.

  e.g.1) Iteration of the following command sequence, CMD0 - CMD1 ---
  The assertion of CMD1 implies a count of internal read operation in Raw NAND.
  CMD0 : Reset command, CMD1 : Send operation command

  e.g.2) Iteration of the following commands, CMD30 and/or CMD31
  CMD30 : Send status of write protection bits, CMD31 : Send type of write protection

Document Revision History

Rev0.1	May. 18th, 2011	- Released as preliminary revision.
Rev0.2	May. 23th, 2011	- Product weight were changed from 230 mg to 235 mg. (Page2) - Operating Current was changed from 120 mA to 100 mA as SDR mode. (Page2) - Density Specifications was fixed. (Page5) - Revised the value of [238] PWR_CL_DDR_52_195 in Extended CSD Register. (Page7) - Revised the value of [203] PWR_CL_26_360 in Extended CSD Register. (Page8) - Revised the value of [202] PWR_CL_52_360 in Extended CSD Register. (Page8) - Revised the value of [201] PWR_CL_26_195 in Extended CSD Register. (Page8) - Revised the value of [200] PWR_CL_52_195 in Extended CSD Register. (Page8)

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