TOSHIBA e-MMC Module

8GB THGBM5G6A2JBAIR

INTRODUCTION

THGBM5G6A2JBAIR is 8-GByte density of e-MMC Module product housed in 153 ball BGA package. This unit is utilized advanced TOSHIBA NAND flash device(s) and controller chip assembled as Multi Chip Module. THGBM5G6A2JBAIR has an industry standard MMC protocol for easy use.

FEATURES

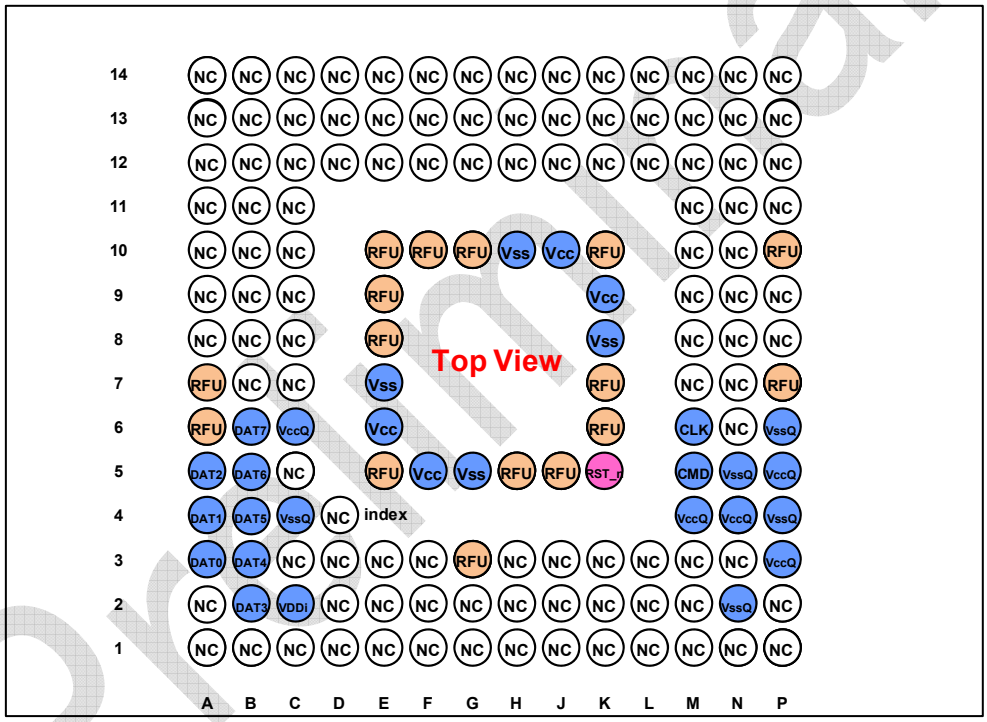
THGBM5G6A2JBAIR Interface

THGBM5G6A2JBAIR has the JEDEC/MMCA Version 4.41 interface with either 1-I/O, 4-I/O and 8-I/O mode support. Furthermore following several new functions that defined in JEDEC/MMCA Version 4.5 were supported.

- 200MHz SDR / Sanitize / Discard / Packed command 8/ Power off notification / Large sector size

Pin Connection

P-VFBGA153-1113-0.50-002 (11.5 x 13mm, H1.0mm max. package)



Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J10	Vcc	N4	VccQ
A4	DAT1	C4	VssQ	K5	RST_n	N5	VssQ
A5	DAT2	C6	VccQ	K8	Vss	P3	VccQ
B2	DAT3	E6	Vcc	K9	Vcc	P4	VssQ
B3	DAT4	E7	Vss	M4	VccQ	P5	VccQ
B4	DAT5	F5	Vcc	M5	CMD	P6	VssQ
B5	DAT6	G5	Vss	M6	CLK		
B6	DAT7	H10	Vss	N2	VssQ		

NC: No Connect, can be connected to ground or left floating.
RFU: Reserved for Future Use, should be left floating for future use.

Part Numbers

Available e-MMC Module Products – Part Numbers

TOSHIBA Part Number	Density	Package Size	NAND Flash Type	Weight
THGBM5G6A2JBAIR	8-GBytes	11.5mm x 13.0mm x 1.0mm(max)	2 x 32Gbit MLC 19nm	0.23g typ.

Operating Temperature and Humidity Conditions

-25°C to +85°C, and 0%RH to 95%RH non-condensing

Storage Temperature and Humidity Conditions

-40°C to +85°C, and 0%RH to 95%RH non-condensing

Performance

x8 mode / Sequential access (2MByte access size)

TOSHIBA Part Number	Density	NAND Flash Type	Interleave Operation	Frequency /Mode	VccQ	Typ. Performance [MB/sec]	
						Read	Write
THGBM5G6A2JBAIR	8-GBytes	2 x 32Gbit MLC 19nm	Interleave	52MHz/SDR	1.8V	(T.B.D)	(T.B.D)
					3.3V	(T.B.D)	(T.B.D)
				52MHz/DDR	1.8V	(T.B.D)	(T.B.D)
					3.3V	(T.B.D)	(T.B.D)
				200MHz/SDR	1.8V	(T.B.D)	(T.B.D)
					3.3V	(T.B.D)	(T.B.D)

Power Supply

Vcc = 2.7V to 3.6V
VccQ = 1.7V to 1.95V / 2.7V to 3.6V

Operating Current (RMS)

TOSHIBA Part Number	Density	NAND Flash Type	Interleave Operation	Frequency /Mode	VccQ	Max Operating Current [mA]
THGBM5G6A2JBAIR	8-GBytes	2 x 32Gbit MLC 19nm	Interleave	52MHz/SDR	1.8V	80(T.B.D)
					3.3V	100(T.B.D)
				52MHz/DDR	1.8V	105(T.B.D)
					3.3V	140(T.B.D)
				200MHz/SDR	1.8V	170(T.B.D)
					3.3V	-

The measurement for max RMS current is done as average RMS current consumption over a period of 100ms

Sleep Mode Current

TOSHIBA Part Number	Density	NAND Flash Type	Interleave Operation	Iccqs [uA]		Iccqs+Iccs [uA]	
				Typ. *1	Max. *2	Typ. *1	Max. *2
THGBM5G6A2JBAIR	8-GBytes	2 x 32Gbit MLC 19nm	Interleave	95(T.B.D)	420(T.B.D)	135(T.B.D)	520(T.B.D)

*1 : The conditions of typical values are 25°C and VccQ = 3.3V or 1.8V.
*2 : The conditions of maximum values are 85°C and VccQ = 3.6V or 1.95V.

Product Architecture

The diagram in Figure 1 illustrates the main functional blocks of the THGBM5G6A2JBAIR.
Specification of the C_{REG} and recommended values of the C_{VCC}, and C_{VCCQ} in the Figure 1 are as follows.

Parameter	Symbol	Unit	Min.	Typ.	Max.
V_{DDi} capacitor value	C_{REG}	µF	0.10*	-	1.00
V_{CC} capacitor value	C_{VCC}	µF	-	2.2 + 0.1	-
V_{CCQ} capacitor value	C_{VCCQ}	µF	-	2.2 + 0.1	-

* Toshiba recommends that the minimum value should be usually applied as the value of C_{REG}.
C_{REG} shall be compliant with X5R/X7R of EIA standard or B of JIS standard.

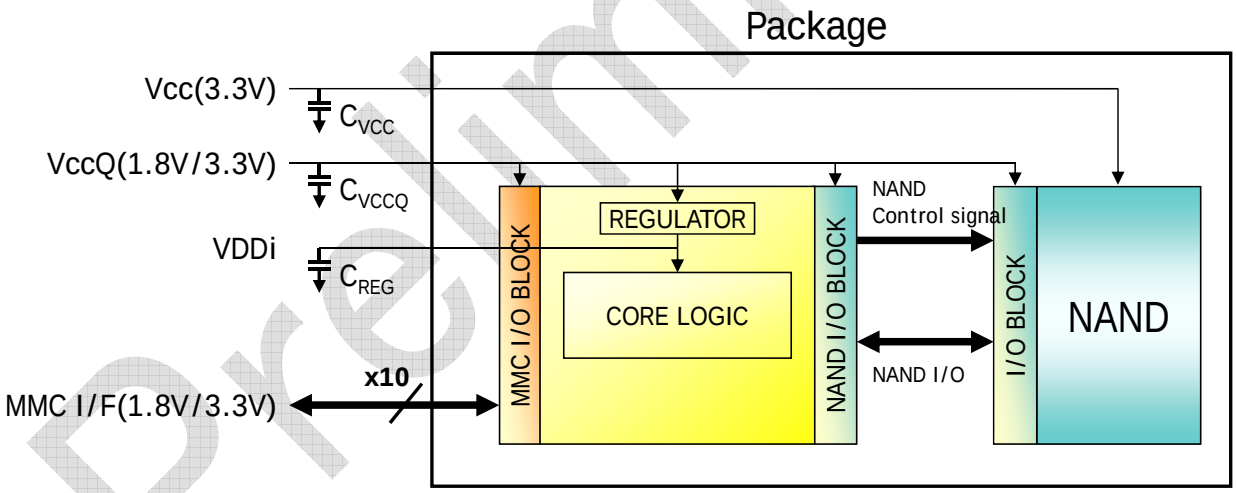


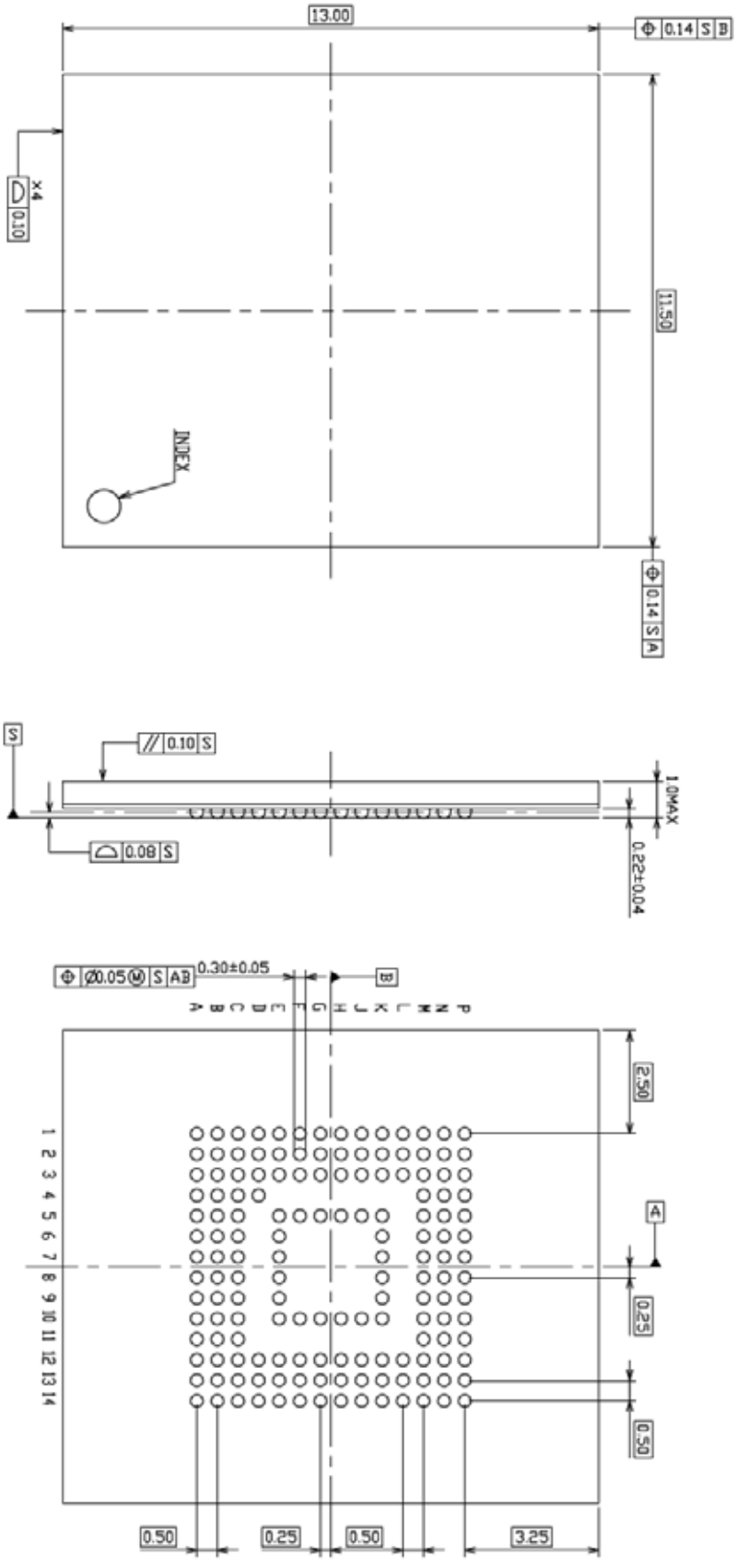
Figure 1 THGBM5G6A2JBAIR Block Diagram

PRODUCT SPECIFICATIONS

Package Dimensions

P-VFBGA153-1113-0.50-002 (11.5 x 13mm, H1.0mm max. package)

Unit : mm



Remark : Data A, B and S are defined by the least square method of all solder balls

Density Specifications

Density	Part Number	Interleave Operation	User Area Density [Bytes]	SEC_COUNT in Extended CSD
8-Gbytes	THGBM5G6A2JBAIR	Interleave	7,818,182,656	0x00E90000

1) User area density shall be reduced if enhanced user data area is defined.

Register Informations

OCR Register

OCR bit	VDD Voltage window	Value
[6:0]	Reserved	000 0000b
[7]	1.70-1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b
[31]	(card power up status bit (busy))[1]	

1) This bit is set to LOW if the card has not finished the power up routine.

CID Register

CID-slice	Name	Field	Width	Value
[127:120]	Manufacturer ID	MID	8	0001 0001b
[119:114] *	Reserved	-	6	0b
[113:112] *	Card/BGA	CBX	2	01b
[111:104] *	OEM/Application ID	OID	8	0b
[103:56]	Product name	PNM	48	0x30 30 38 47 39 32 (008G92)
[55:48]	Product revision	PRV	8	0x00
[47:16]	Product serial	PSN	32	Serial number
[15:8]	Manufacturing date	MDT	8	see-JEDEC Specification
[7:1]	CRC7 checksum	CRC	7	CRC7
[0]	Not used, always '1'	-	1	1b

CSD Register

CSD-slice	Name	Field	Width	Cell Type	Value
[127:126]	CSD structure	CSD_STRUCTURE	2	R	0x3
[125:122]	System specification version	SPEC_VERS	4	R	0x4
[121:120]	Reserved	-	2	R	0x0
[119:112]	Data read access-time 1	TAAC	8	R	0x0E
[111:104]	Data read access-time 2 in CLK cycles (NSAC * 100)	NSAC	8	R	0x00
[103:96]	Max. bus clock frequency	TRAN_SPEED	8	R	0x32
[95:84]	Card command classes	CCC	12	R	0x0F5
[83:80]	Max. read data block length	READ_BL_LEN	4	R	0x9
[79:79]	Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0x0
[78:78]	Write block misalignment	WRITE_BLK_MISALIGN	1	R	0x0
[77:77]	Read block misalignment	READ_BLK_MISALIGN	1	R	0x0
[76:76]	DSR implemented	DSR_IMP	1	R	0x0
[75:74]	Reserved	-	2	R	0x0
[73:62]	Device size	C_SIZE	12	R	0xFFF
[61:59]	Max. read current @ VDD min.	VDD_R_CURR_MIN	3	R	0x7
[58:56]	Max. read current @ VDD max.	VDD_R_CURR_MAX	3	R	0x7
[55:53]	Max. write current @ VDD min.	VDD_W_CURR_MIN	3	R	0x7
[52:50]	Max. write current @ VDD max.	VDD_W_CURR_MAX	3	R	0x7
[49:47]	Device size multiplier	C_SIZE_MULT	3	R	0x7
[46:42]	Erase group size	ERASE_GRP_SIZE	5	R	0x1F
[41:37]	Erase group size multiplier	ERASE_GRP_MULT	5	R	0x1F
[36:32]	Write protect group size	WP_GRP_SIZE	5	R	0x0F
[31:31]	Write protect group enable	WP_GRP_ENABLE	1	R	0x1
[30:29]	Manufacturer default ECC	DEFAULT_ECC	2	R	0x0
[28:26]	Write speed factor	R2W_FACTOR	3	R	0x4
[25:22]	Max. write data block length	WRITE_BL_LEN	4	R	0x9
[21:21]	Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0x0
[20:17]	Reserved	-	4	R	0x0
[16:16]	Content protection application	CONTENT_PROT_APP	1	R	0x0
[15:15]	File format group	FILE_FORMAT_GRP	1	R/W	0x0
[14:14]	Copy flag (OTP)	COPY	1	R/W	0x0
[13:13]	Permanent write protection	PERM_WRITE_PROTECT	1	R/W	0x0
[12:12]	Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	0x0
[11:10]	File format	FILE_FORMAT	2	R/W	0x0
[9:8]	ECC code	ECC	2	R/W/E	0x0
[7:1]	CRC	CRC	7	R/W/E	CRC
[0]	Not used, always ‘1’	-	1	-	0x1

Extended CSD Register

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[511:505]	Reserved	-	7	-	All '0'
[504]	Supported Command Sets	S_CMD_SET	1	R	0x01
[503]	HPI features	HPI_FEATURES	1	R	0x01
[502]	Background operations support	BKOPS_SUPPORT	1	R	0x01
[501]	Max_packed read commands	MAX_PACKED_READS	1	R	0x3F
[500]	Max_packed write commands	MAX_PACKED_WRITES	1	R	0x3F
[499]	Data Tag Support	DATA_TAG_SUPPORT	1	R	0x00
[498]	Tag Unit Size	TAG_UNIT_SIZE	1	R	0x00
[497]	Tag Resource Size	TAG_RES_SIZE	1	R	0x00
[496]	Context management capabilities	CONTEXT_CAPABILITIES	1	R	0x00
[495]	Large Unit size	LARGE_UNIT_SIZE_M1	1	R	0x00
[494]	Extended partitions attribute support	EXT_SUPPORT	1	R	0x00
[493:253]	Reserved	-	241	-	All '0'
[252:249]	Cache size	CACHE_SIZE	4	R	0x00
[248]	Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	0x05
[247]	Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	0x32
[246]	Background operations status	BKOPS_STATUS	1	R	0x00
[245:242]	Number of correctly programmed sectors	CORRECTLY _PRG_SECTORS_NUM	4	R	0x00000000
[241]	1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	0x1E
[240]	Reserved	-	1	-	0x00
[239]	Power class for 52MHz, DDR @ 3.6V	PWR_CL_DDR_52_360	1	R	0x22(T.B.D)
[238]	Power class for 52MHz, DDR @ 1.95V	PWR_CL_DDR_52_195	1	R	0x55(T.B.D)
[237]	Power class for 200MHz @ 3.6V	PWR_CL_200_360	1	R	0x22(T.B.D)
[236]	Power class for 200MHz @ 1.95V	PWR_CL_200_195	1	R	0x88(T.B.D)
[235]	Minimum Write Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	0x0A
[234]	Minimum Read Performance for 8bit @ 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	0x50(T.B.D)
[233]	Reserved	-	1	-	0x00
[232]	TRIM Multiplier	TRIM_MULT	1	R	0x01
[231]	Secure Feature support	SEC_FEATURE_SUPPORT	1	R	0x55 *4
[230]	Secure Erase Multiplier (obsolete*3)	SEC_ERASE_MULT	1	R	0x02(T.B.D)
[229]	Secure TRIM Multiplier (obsolete*3)	SEC_TRIM_MULT	1	R	0x0A(T.B.D)
[228]	Boot information	BOOT_INFO	1	R	0x07
[227]	Reserved	-	1	R	0x00
[226]	Boot partition size	BOOT_SIZE_MULTI	1	R	0x20
[225]	Access size	ACC_SIZE	1	R	0x08
[224]	High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	0x08
[223]	High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	0x02
[222]	Reliable write sector count	REL_WR_SEC_C	1	R	0x10

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[221]	High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	0x02
[220]	Sleep current (Vcc)	S_C_VCC	1	R	0x07(T.B.D)
[219]	Sleep current (VccQ)	S_C_VCCQ	1	R	0x09
[218]	Reserved	-	1	-	0x00
[217]	Sleep/awake timeout	S_A_TIMEOUT	1	R	0x11
[216]	Reserved	-	1	-	0x00
[215:212]	Sector Count	SEC_COUNT	4	R	0x00E90000
[211]	Reserved	-	1	-	0x00
[210]	Minimum Write Performance for 8bit @ 52MHz	MIN_PERF_W_8_52	1	R	0x14(T.B.D)
[209]	Minimum Read Performance 8bit @ 52MHz	MIN_PERF_R_8_52	1	R	0x64(T.B.D)
[208]	Minimum Write Performance for 8bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0x0F(T.B.D)
[207]	Minimum Read Performance for 8 bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	0x3C(T.B.D)
[206]	Minimum Write Performance for 4bit @ 26MHz	MIN_PERF_W_4_26	1	R	0x0F(T.B.D)
[205]	Minimum Read Performance for 4bit @ 26MHz	MIN_PERF_R_4_26	1	R	0x1E(T.B.D)
[204]	Reserved	-	1	-	0x00
[203]	Power class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	0x00(T.B.D)
[202]	Power class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	0x00(T.B.D)
[201]	Power class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	0x44(T.B.D)
[200]	Power class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	0x44(T.B.D)
[199]	Partition switching timing	PARTITION_SWITCH_TIME	1	R	0x01
[198]	Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	0x0A
[197]	I/O Driver Strength	DRIVER_STRENGTH	1	R	0x0F
[196]	Card Type	CARD_TYPE	1	R	0x17
[195]	Reserved	-	1	-	0x00
[194]	CSD structure version	CSD_STRUCTURE	1	R	0x02
[193]	Reserved	-	1	-	0x00
[192]	Extended CSD revision	EXT_CSD_REV	1	R	0x06
[191]	Command Set	CMD_SET	1	R/W/E_P	0x00
[190]	Reserved	-	1	-	0x00
[189]	Command set revision	CMD_SET_REV	1	R	0x00
[188]	Reserved	-	1	-	0x00
[187]	Power class [1]	POWER_CLASS	1	R/W/E_P	0x00 *1
[186]	Reserved	-	1	-	0x00
[185]	High-speed interface timing	HS_TIMING	1	R/W/E_P	0x00
[184]	Reserved		1	-	0x00
[183]	Bus width mode	BUS_WIDTH	1	W/E_P	0x00
[182]	Reserved	-	1	-	0x00
[181]	Erased memory content	ERASED_MEM_CONT	1	R	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[180]	Reserved	-	1	-	0x00
[179]	Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	0x00
[178]	Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	0x00
[177]	Boot bus width	BOOT_BUS_WIDTH	1	R/W/E	0x00
[176]	Reserved	-	1	-	0x00
[175]	High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	0x00
[174]	Boot write protection status registers	BOOT_WP_STATUS	1	R	0x00
[173]	Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	0x00
[172]	Reserved	-	1	-	0x00
[171]	User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	0x00
[170]	Reserved	-	1	-	0x00
[169]	FW configuration	FW_CONFIG	1	R/W	0x00
[168]	RPMB Size	RPMB_SIZE_MULT	1	R	0x04
[167]	Write reliability setting register	WR_REL_SET	1	R/W	0x1F
[166]	Write reliability parameter register	WR_REL_PARAM	1	R	0x05
[165]	Start Sanitize operation	SANITIZE_START	1	W/E_P	0x00
[164]	Manually start background operations	BKOPS_START	1	W/E_P	0x00
[163]	Enable background operations handshake	BKOPS_EN	1	R/W	0x00
[162]	H/W reset function	RST_n_FUNCTION	1	R/W	0x00
[161]	HPI management	HPI_MGMT	1	R/W/E_P	0x00
[160]	Partitioning Support	PARTITIONING_SUPPORT	1	R	0x03
[159:157]	Max Enhanced Area Size [2]	MAX_ENH_SIZE_MULT	3	R	0x0001D2
[156]	Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	0x00
[155]	Partitioning Setting	PARTITION_SETTING_ COMPLETED	1	R/W	0x00
[154:143]	General Purpose Partition Size [3]	GP_SIZE_MULT	12	R/W	0x00
[142:140]	Enhanced User Data Area Size [4]	ENH_SIZE_MULT	3	R/W	0x00
[139:136]	Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	0x00
[135]	Reserved	-	1	-	0x00
[134]	Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	0x00
[133]	Reserved	-	1	-	0x00
[132]	Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	0x00 *1
[131]	Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	0x00 *1
[130]	Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SU PPORT	1	R	0x01
[129:128]	Reserved	-	2	-	All '0'
[127:64]	Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	-	-
[63]	Native sector size	NATIVE_SECTOR_SIZE	1	R	0x01
[62]	Sector size emulation	USE_NATIVE_SECTOR	1	R/W	0x00
[61]	Sector size	DATA_SECTOR_SIZE	1	R	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[60]	1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	0x0A
[59]	Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	0x00 *1
[58]	Number of addressed group to be Released	DYNCAP_NEEDED	1	R	0x00
[57:56]	Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	All '0' *2
[55:54]	Exception events status	EXCEPTION_EVENTS_STATUS	2	R	All '0'
[53:52]	Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	0x00 *1
[51:37]	Context configuration	CONTEXT_CONF	15	R/W/E_P	0x00 *1
[36]	Packed command status	PACKED_COMMAND_STATUS	1	R	0x00
[35]	Packed command failure index	PACKED_FAILURE_INDEX	1	R	0x00
[34]	Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	0x00
[33]	Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	0x00 *1
[32]	Flushing of the cache	FLUSH_CACHE	1	W/E_P	0x00 *1
[31:0]	Reserved	-	32	-	All '0'

*1 Although these fields can be re-written by host, TOSHIBA e-MMC does not support.
*2 Although Bit3(SYSPOOL_EVENT_EN) and Bit2(DYNCAP_EVENT_EN) field can be re-written by host, TOSHIBA e-MMC does not support.
*3 In Ver4.5, Byte[230](SEC_ERASE_MULT) and Byte[229](SEC_TRIM_MULT) is obsolete. However, TOSHIBA e-MMC supports these functions.
*4 In Ver4.5, Bit0(SECURE_ER_EN) and Bit4(SEC_GB_CL_EN) of Byte[231](SEC_FEATURE_SUPPORT) is obsolete. However, TOSHIBA e-MMC supports these functions.

a) Although POWER_CLASS [187] Field can be re-written by host, e-MMC does not support any power budget management.

b) Max Enhanced Area Size (MAX_ENH_SIZE_MULT [159:157]) has to be calculated by following formula.

Max Enhanced Area = MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GPR_SIZE x 512kBytes

$$\sum_{i=1}^{4} \text{Enhanced general partition size}(i) + \text{Enhanced user data area} \leq \text{Max enhanced area}$$

c) General Purpose Partition Size (GP_SIZE_MULT_GP0 - GP_SIZE_MULT_GP3 [154:143]) has to be calculated by following formula.

General_Purpose_Partition_X Size = (GP_SIZE_MULT_X_2 x 2^{16} + GP_SIZE_MULT_X_1 x 2^{8} + GP_SIZE_MULT_X_0 x 2^{0}) x HC_WP_GRP_SIZE x HC_ERASE_GPR_SIZE x 512kBytes

d) Enhanced User Data Area Size (ENH_SIZE_MULT [142:140]) has to be calculated by following formula.

Enhanced User Data Area x Size = (ENH_SIZE_MULT_2 x 2^{16} + ENH_SIZE_MULT_1 x 2^{8} + ENH_SIZE_MULT_0 x 2^{0}) x HC_WP_GRP_SIZE x HC_ERASE_GPR_SIZE x 512kBytes

Unsupported register fields (V4.41α)

This device V4.41α does not support the following functions defined in JEDEC V4.5.
Following table shows related register fields and behavior when the host accesses to it.

CSD-slice	Field	behavior	Width	Cell Type	Value
[127:64]	VENDOR_SPECIFIC_FIELD	Please don't access to these fields without vender recommendation.	64	<vendor specific>	<vendor specific>
[187]	POWER_CLASS	Host can access these fields according to the cell types without any error, but each function is disabled.	1	R/W/E_P	0x00
[132]	TCASE_SUPPORT		1	W/E_P	0x00
[131]	PERIODIC_WAKEUP		1	R/W/E	0x00
[59]	CLASS_6_CTRL		1	R/W/E_P	0x00
[53:52]	EXT_PARTITIONS_ATTRIBUTE		2	R/W	0x00
[51:37]	CONTEXT_CONF		15	R/W/E_P	0x00
[33]	CACHE_CTRL		1	R/W/E_P	0x00
[32]	FLUSH_CACHE		1	W/E_P	0x00

*CMD23 argument bit[29:24] that defined as data tag, context ID and forced programming in JEDEC V4.5 are also ignored.

Remark on the value of [192]EXT_CSD_REV in EXT_CSD register

Linux kernel might check if the value of EXT_CSD[192]EXT_CSD_REV is suitable for the kernel itself or not and return the initialize error when the device indicates JEDEC/MMCA V4.5 or later because the old kernel version does not support V4.5.

In case of V4.41α device, EXT_CSD[192]EXT_CSD_REV indicates 0x06 that means V4.5.

If the Host could not initialize the V4.41α device, Host should modify the treatment of EXT_CSD[192] EXT_CSD_REV to accept V4.5 or use Linux kernel release 3.0.1 or later that can initialize V4.41α device.

ELECTRICAL CHARACTERISTICS

DC Characteristics

General

Parameter	Symbol	Test Conditions	Min	Max	Unit
Peak voltage on all lines			-0.5	VccQ+0.5	V
All Inputs					
Input Leakage Current (before initialization sequence[1] and/or the internal pull up resistors connected)			-100	100	uA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)			-2	2	uA
All Outputs					
Output Leakage Current (before initialization sequence)			-100	100	uA
Output Leakage Current (after initialization sequence)			-2	2	uA

1) Initialization sequence is defined in Power-Up chapter of JEDEC/MMCA Standard

Power Supply Voltage

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage 1	V_{CC}		2.7	3.6	V
Supply voltage 2	VccQ		1.7	1.95	V
			2.7	3.6	V
Supply power-up for 3.3V	tPRUH		5 us	35 ms	
Supply power-up for 1.8V	tPRUL		5 us	25 ms	

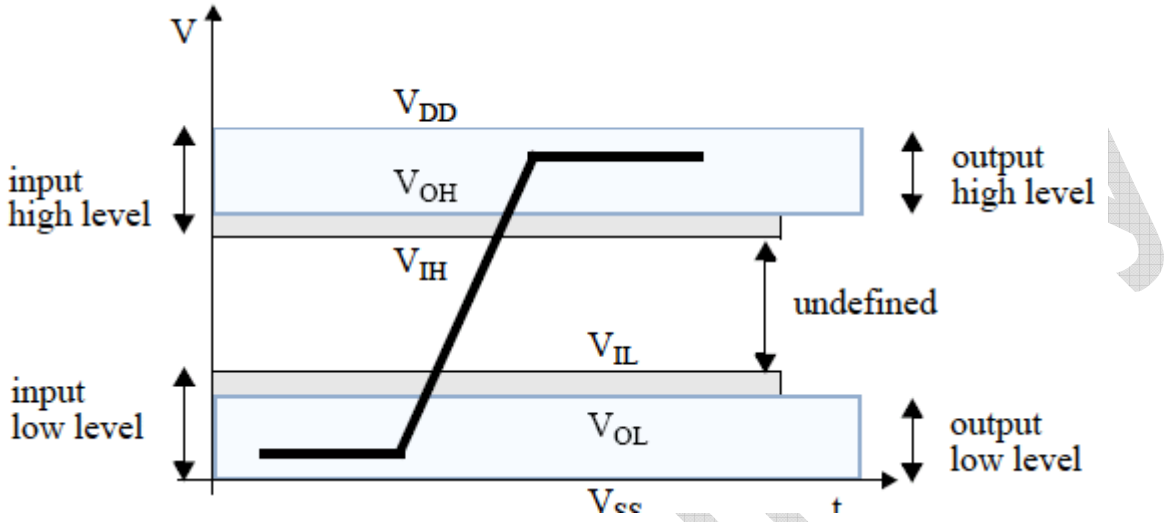
Supply Current

Parameter		Symbol	Interleave Operation	Mode	VccQ	Min	Max	Unit
Operation (RMS)	Read	I_{ROP}	Interleave	SDR	1.8V	—	75(T.B.D)	mA
					3.3V	—	100(T.B.D)	
				DDR	1.8V	—	105(T.B.D)	mA
					3.3V	—	140(T.B.D)	
				HS200	1.8V	—	170(T.B.D)	mA
					3.3V	—	—	
	Write	I_{WOP}	Interleave	SDR	1.8V	—	80(T.B.D)	mA
					3.3V	—	85(T.B.D)	
				DDR	1.8V	—	90(T.B.D)	mA
					3.3V	—	100(T.B.D)	
				HS200	1.8V	—	100(T.B.D)	mA
					3.3V	—	—	

Internal resistance and Device capacitance

Parameter	Symbol	Test Conditions	Min	Max	Unit
Single device capacitance	C_{DEVICE}		—	9	pF
Internal pull up resistance DAT1 – DAT7	R_{INT}		10	150	kOhm

Bus Signal Levels



Open-Drain Mode Bus Signal Level

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -100uA	VccQ - 0.2	—	V
Output LOW voltage	V_{OL}	I_{OL} = 2mA	—	0.3	V

Push-Pull Mode Bus Signal Level (High-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -100uA @ $V_{DD\ min}$	0.75 * VccQ	—	V
Output LOW voltage	V_{OL}	I_{OL} = 100uA @ $V_{DD\ min}$	—	0.125 * VccQ	V
Input HIGH voltage	V_{IH}		0.625* VccQ	VccQ + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.25 * VccQ	V

Push-Pull Mode Bus Signal Level (Dual-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -2mA @ $V_{DD\ min}$	VccQ - 0.45	—	V
Output LOW voltage	V_{OL}	I_{OL} = 2mA @ $V_{DD\ min}$	—	0.45	V
Input HIGH voltage	V_{IH}		0.65 * VccQ	VccQ + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.35 * VccQ	V

Driver Types Definition

Driver Type-0 is defined as mandatory for e-MMC HS200 Device. While three additional Driver Types (1, 2 and 3) are defined as optional, to allow the support of wider Host loads. The Host may select the most appropriate Driver Type of the Device to achieve optimal signal integrity performance.

NOTE : Drive strength definitions are same for 1.8V signaling level and for 1.2V signaling level.

Driver Type-0 is targeted for transmission line, based distributed system with 50Ω nominal line impedance. Therefore, it is defined as 50Ω nominal driver. When tested with C_L = 15pF Driver Type-0 shall meet all AC characteristics and HS200 Device output timing requirements. The test circuit defined in section 10.4.4.3 of JEDEC/MMCA Standard 4.5 is used for testing of Driver Type-0.

The Optional Driver Types are defined with reference to Driver Type-0.

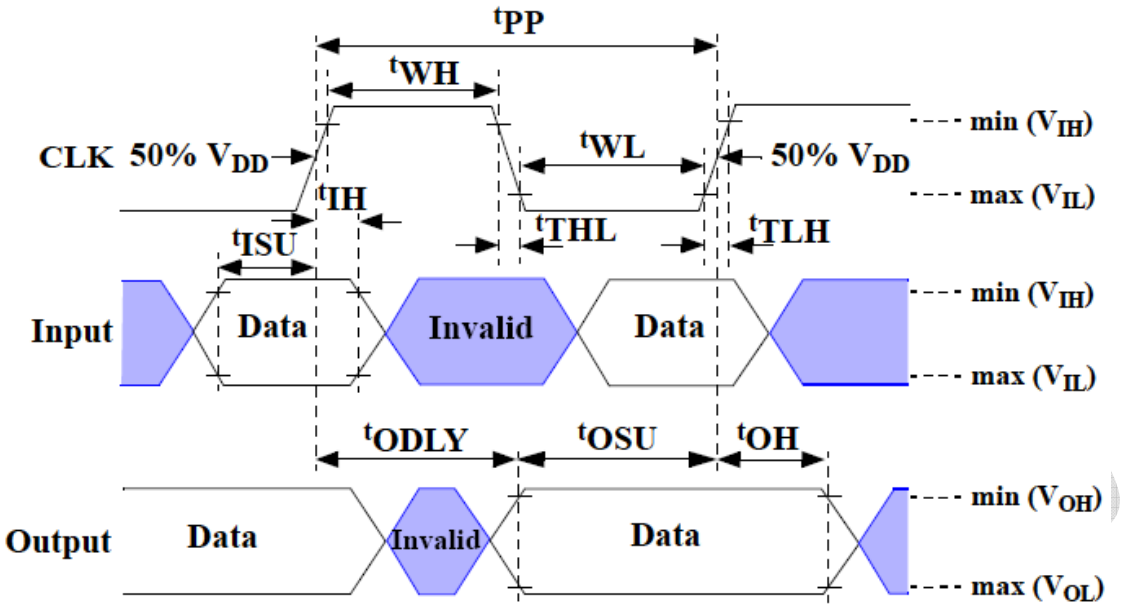
Driver Type	HS200 Support	TOSHIBA e-MMC	Normal Impedance	Approximated driving capability compared to Type-0	Remark
0	Mandatory	Supported	50 Ω	x1	Default Driver Type.Supports up to 200MHz operation.
1	Optional	Supported	33 Ω	x1.5	Supports up to 200MHz operation.
2	Optional	Supported	66 Ω	x0.75	The weakest driver that supports up to 200MHz operation.
3	Optional	Supported	100 Ω	x0.5	For low noise and low EMI systems. Maximal operating frequency is decided by Host design.

1) Support of Driver Type-0 is mandatory for HS200 Device, while supporting Driver types 1, 2 and 3 is optional for HS200 Device.

2) Nominal impedance is defined by I-V characteristics of output driver at 0.9V when V_{CCQ} = 1.8V.

3) Nominal impedance is defined by I-V characteristics of output driver at 0.6V when V_{CCQ} = 1.2V.

Bus Timing



Data must always be sampled on the rising edge of the clock.

Card Interface Timings (High-speed interface timing)

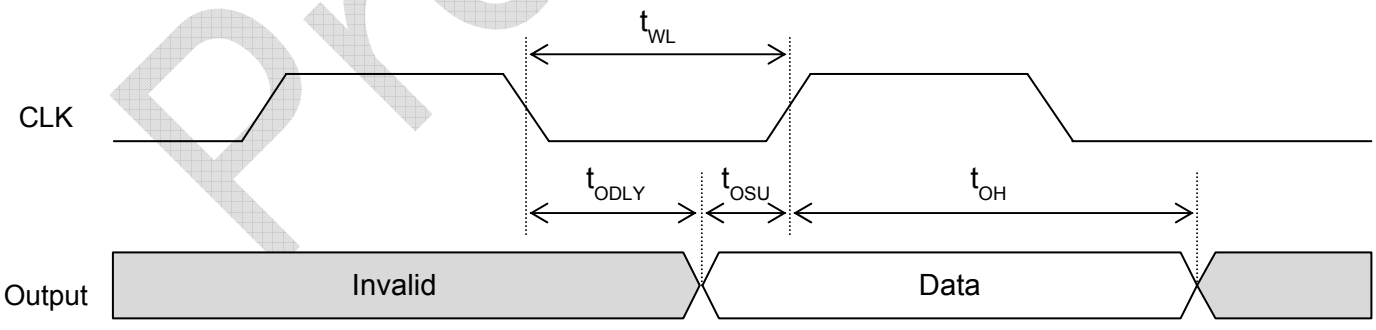
Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	f_{pp}	C_L <= 30pF Tolerance: +100KHz	0	52[3]	MHz
Clock frequency Identification Mode (OD)	f_{OD}	Tolerance: +20KHz	0	400	KHz
Clock high time	t_{WH}	C_L <= 30pF	6.5	—	ns
Clock low time	t_{WL}	C_L <= 30pF	6.5	—	ns
Clock rise time[4]	t_{TLH}	C_L <= 30pF	—	3	ns
Clock fall time	t_{THL}	C_L <= 30pF	—	3	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t_{ISU}	C_L <= 30pF	3	—	ns
Input hold time	t_{IH}	C_L <= 30pF	3	—	ns
Outputs CMD,DAT (referenced to CLK)					
Output Delay time during Data Transfer	t_{ODLY}	C_L <= 30pF	—	13.7	ns
Output hold time	t_{OH}	C_L <= 30pF	2.5	—	ns
Signal rise time [5]	t_{rise}	C_L <= 30pF	—	3	ns
Signal fall time	t_{fall}	C_L <= 30pF	—	3	ns

1) CLK timing is measured at 50% of VccQ
2) THGBM5G6A2JBAIR shall support the full frequency range from 0-26MHz, or 0-52MHz
3) e-MMC can operate as high-speed interface timing at 26MHz clock frequency.
4) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).
5) Inputs CMD,DAT rise and fall times area measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

Card Interface Timings (Backward-compatible interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[3]	f_{pp}	C_L <= 30pF	0	26	MHz
Clock frequency Identification Mode (OD)	f_{OD}	Tolerance: +20KHz	0	400	KHz
Clock high time	t_{WH}	C_L <= 30pF	10	—	ns
Clock low time	t_{WL}	C_L <= 30pF	10	—	ns
Clock rise time[4]	t_{TLH}	C_L <= 30pF	—	10	ns
Clock fall time	t_{THL}	C_L <= 30pF	—	10	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t_{ISU}	C_L <= 30pF	3	—	ns
Input hold time	t_{IH}	C_L <= 30pF	3	—	ns
Outputs CMD,DAT (referenced to CLK)					
Output set-up time[5]	t_{OSU}	C_L <= 30pF	11.7	—	ns
Output hold time[5]	t_{OH}	C_L <= 30pF	8.3	—	ns

1) The e-MMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VccQ
3) For compatibility with e-MMCs that support the v4.2 standard or earlier, host should not use >26MHz before switching to high-speed interface timing.
4) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).
5) t_{OSU} and t_{OH} are defined as values from clock rising edge. However, the e-MMC device will utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set t_{WL} value as long as possible within the range which will not go over t_{CK} - t_{OH}(min) in the system or to use slow clock frequency, so that host could have data set up margin for the device.
Toshiba e-MMC device utilize clock falling edge to output data in backward compatibility mode.
Host should optimize the timing in order to have data set up margin as follows.

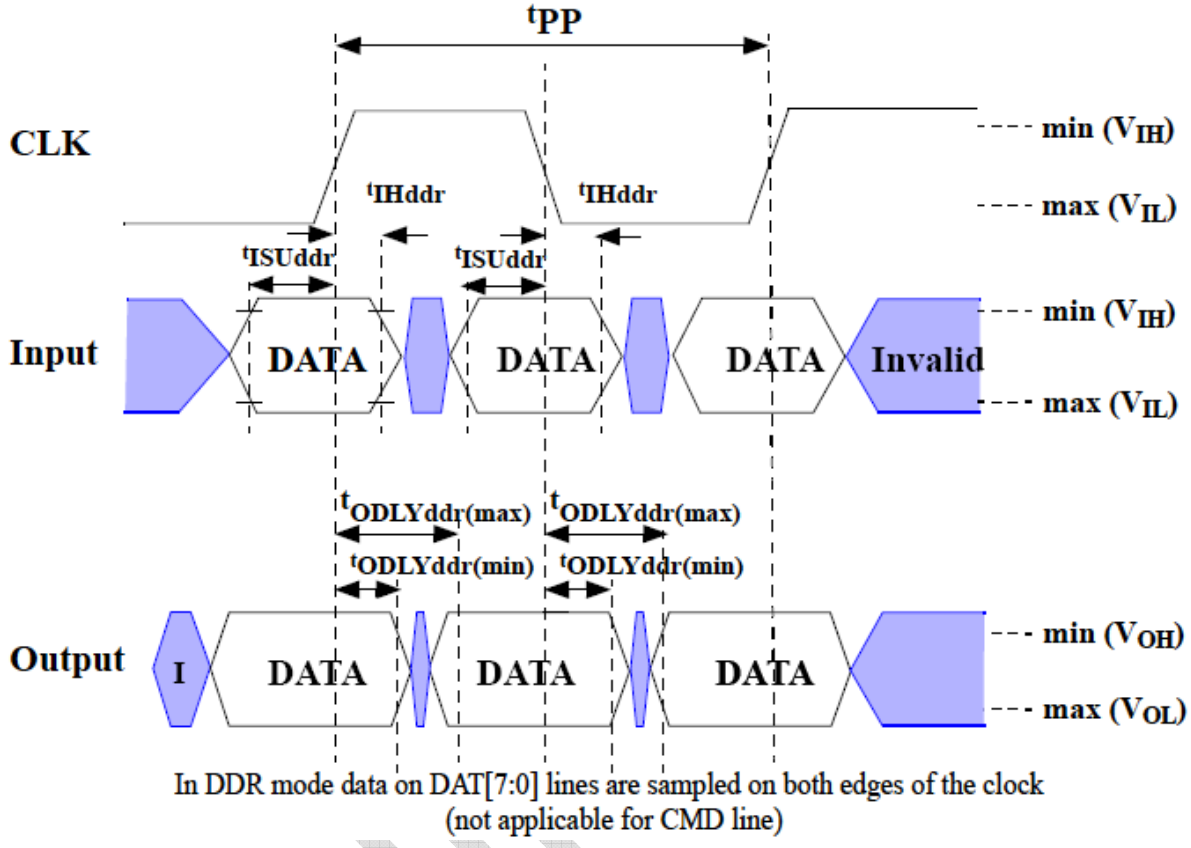


$$t_{OSU}(\text{min}) = t_{WL}(\text{min}) - t_{ODLY}(\text{max 8ns})$$

Figure 2 Output timing

Bus Timing for DAT signals for during 2x data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. the CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in High-speed interface timing or Backward-compatible interface timing.



High-speed dual data rate interface timings

Parameter	Symbol	Min	Max	Unit	Remark [1]
Input CLK [1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUddr}	2.5	—	ns	CL ≤ 20pF
Input hold time	t_{IHddr}	2.5	—	ns	CL ≤ 20pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	CL ≤ 20pF
Signal rise time (all signals) [2]	t_{RISE}	—	2	ns	CL ≤ 20pF
Signal fall time (all signals)	t_{FALL}	—	2	ns	CL ≤ 20pF

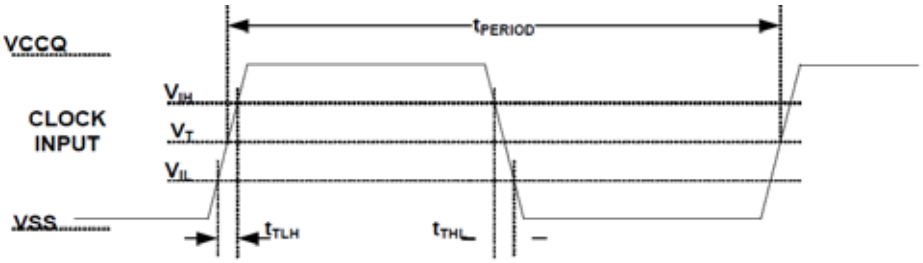
1) CLK timing is measured at 50% of VccQ.

2) Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Bus Timing Specification in HS200 mode

HS200 Clock Timing

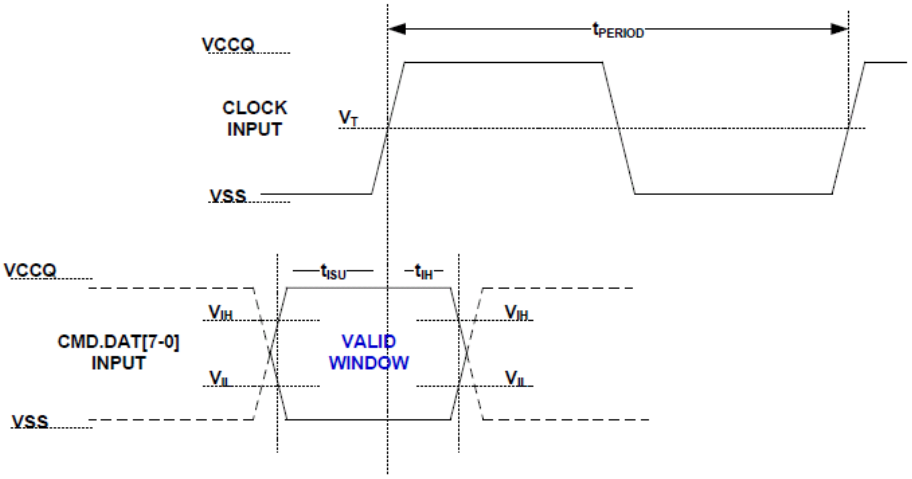
Host CLK Timing in HS200 mode shall conform to the timing specified in following figure and Table. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device. The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.



N OTE 1 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).
N OTE 2 V_T=0.975V - Clock Threshold, indicates clock reference point for timing measurements.

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5	—	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	—	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{BGA}=9pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	90	%	

HS200 Device Input Timing



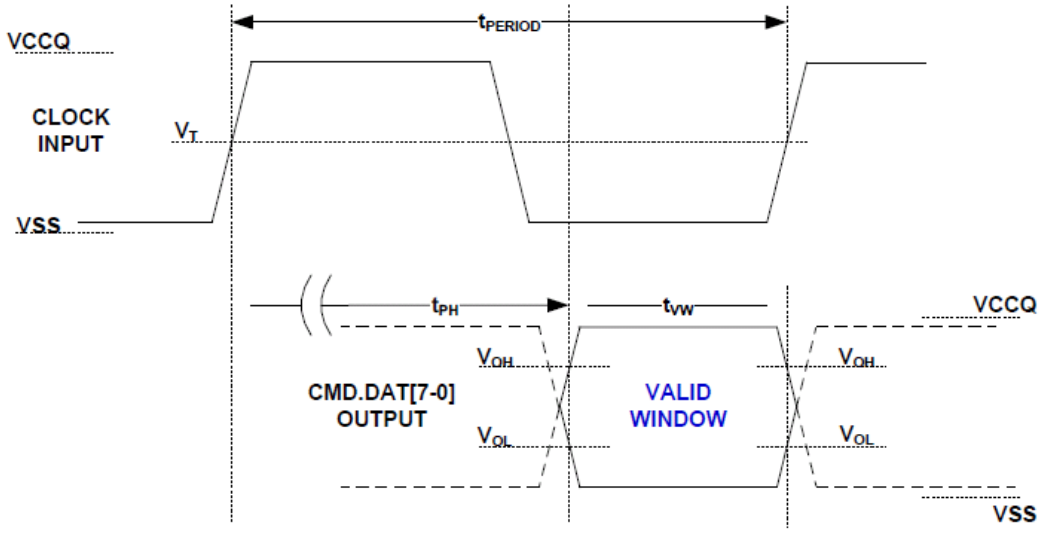
Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Symbol	Min	Max	Unit	Remark
t_{ISU}	1.40	—	ns	5pF <= C_{BGA} <= 9pF
t_{IH}	0.8		ns	5pF <= C_{BGA} <= 9pF

HS200 Device Output Timing

t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD}. After initialization, the t_{PH} may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

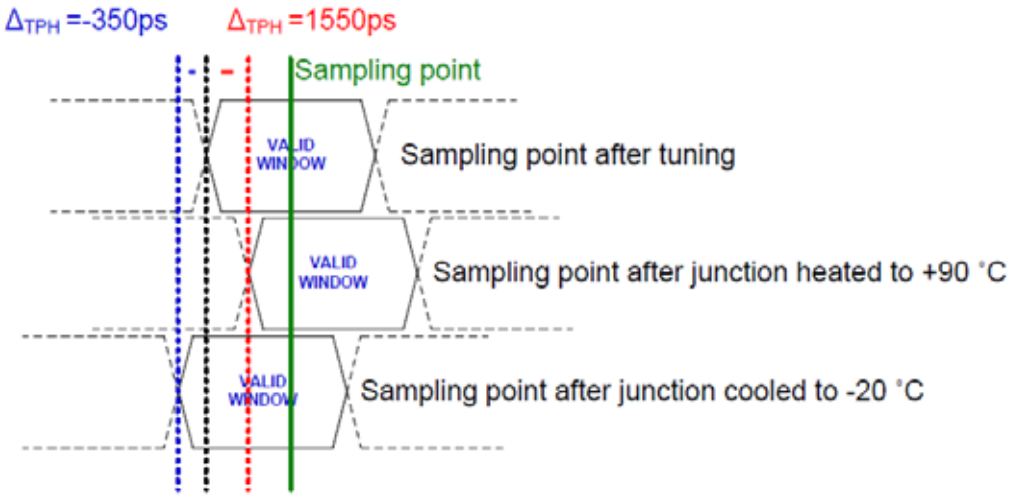
While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by Δ_{TPH}. Output valid data window (t_{VW}) is available regardless of the drift (Δ_{TPH}) but position of data window varies by the drift.



Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

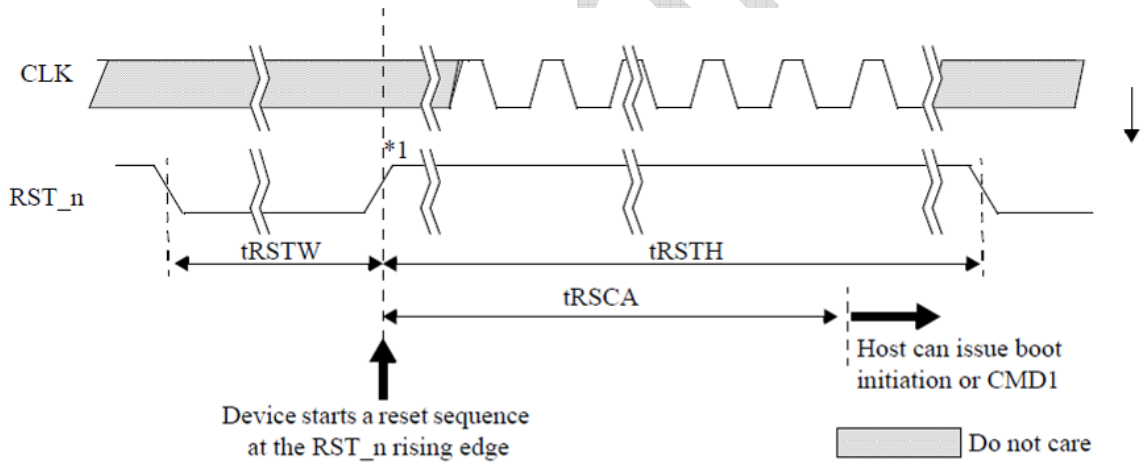
Symbol	Min	Max	Unit	Remark [1]
t_{PH}	0	2	ns	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ_{TPH}	-350 (ΔT = -20deg.C)	+1550 (ΔT = -90deg.C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure Δ_{TPH} is 2600ps for ΔT from -25 deg.C to 125 deg.C during operation.
t_{VW}	0.575	—	UI	t_{VW} =2.88ns at 200MHz Using test circuit in following figure including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected t_{VW} at Host input is larger than 0.475UI.

Δ_{TPH} consideration



Implementation Guide:
Host should design to avoid sampling errors that may be caused by the Δ_{TPH} drift.
It is recommended to perform tuning procedure while Device wakes up, after sleep.
One simple way to overcome the Δ_{TPH} drift is by reduction of operating frequency.

H/W Reset Operation



(Note) *1 : Device will detect the rising edge of RST_n signal to trigger internal reset sequence

H/W Reset Timings

Parameter	Symbol	Test Conditions	Min	Max	Unit
RST_n pulse width	tRSTW		1	—	us
RST_n to Command time	tRSCA		200 [1]	—	us
RST_n high period (interval time)	tRSTH		1	—	us

1) 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA

Functional restrictions

None.

Reliability Guidance

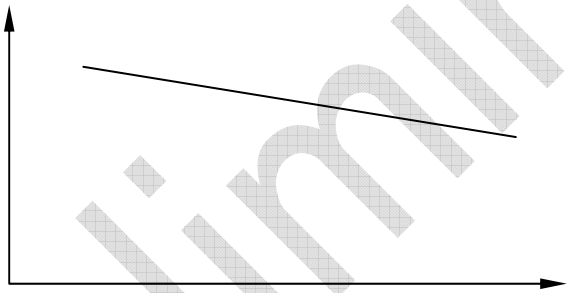
This reliability guidance is intended to notify some guidance related to using raw MLC NAND flash. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

-Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

-Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Also write/erase endurance deteriorates data retention capability. The figure below shows a generic trend of relationship between write/erase endurance and data retention.



-Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Considering the above failure modes, TOSHIBA recommends following usage:

- Please avoid any excessive iteration of resets and initialization sequences (card identification mode) as far as possible after power-on, which may result in read disturb failure. The resets include hardware resets and software resets.

  e.g.1) Iteration of the following command sequence, CMD0 - CMD1 ---
  The assertion of CMD1 implies a count of internal read operation in Raw NAND.
  CMD0 : Reset command, CMD1 : Send operation command

  e.g.2) Iteration of the following commands, CMD30 and/or CMD31
  CMD30 : Send status of write protection bits, CMD31 : Send type of write protection

Document Revision History

Rev0.1	May 24th, 2012	- Released as preliminary revision.
Rev0.2	June 7th, 2012	- Revised the Bytes Size of [129:128] RESERVED in EXT_CSD register. (Page9) Revised the RESTRICTIONS ON PRODUCT USE. (Page 23) Revised the weight value. (Page 2)

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