524,288 WORDS × 40 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM405120ASG/BSG is a 524,288 words by 40 bits dynamic RAM module which assembled 20 pcs of TC514256AJ/BJ on the printed circuit board.

The THM405120ASG/BSG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

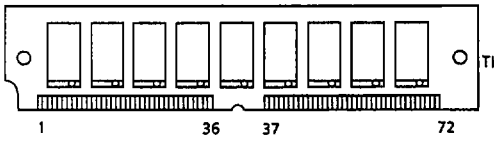
FEATURES

- 524,288 words by 40 bits organization

	-60	-70	-80	-10
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA} Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC} Cycle Time	110ns	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns	60ns

- Low power
  - 5,060mW MAX. Operating (THMxxxxxx-60)
  - 4,510mW MAX. Operating (THMxxxxxx-70)
  - 3,960mW MAX. Operating (THMxxxxxx-80)
  - 3,410mW MAX. Operating (THMxxxxxx-10)
  - 110mW MAX. Standby
- Read-Modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- 512 Refresh cycles / 8ms
- Fast access time and cycle time
- Single power supply of 5V ± 10%
- All inputs and outputs TTL compatible
- Gold Contact
- JEDEC OUTLILNE : THM405120BSG - 60, ASG - 70, 80, 10

PIN CONNECTION (TOP VIEW)



THM405120ASG/BSG

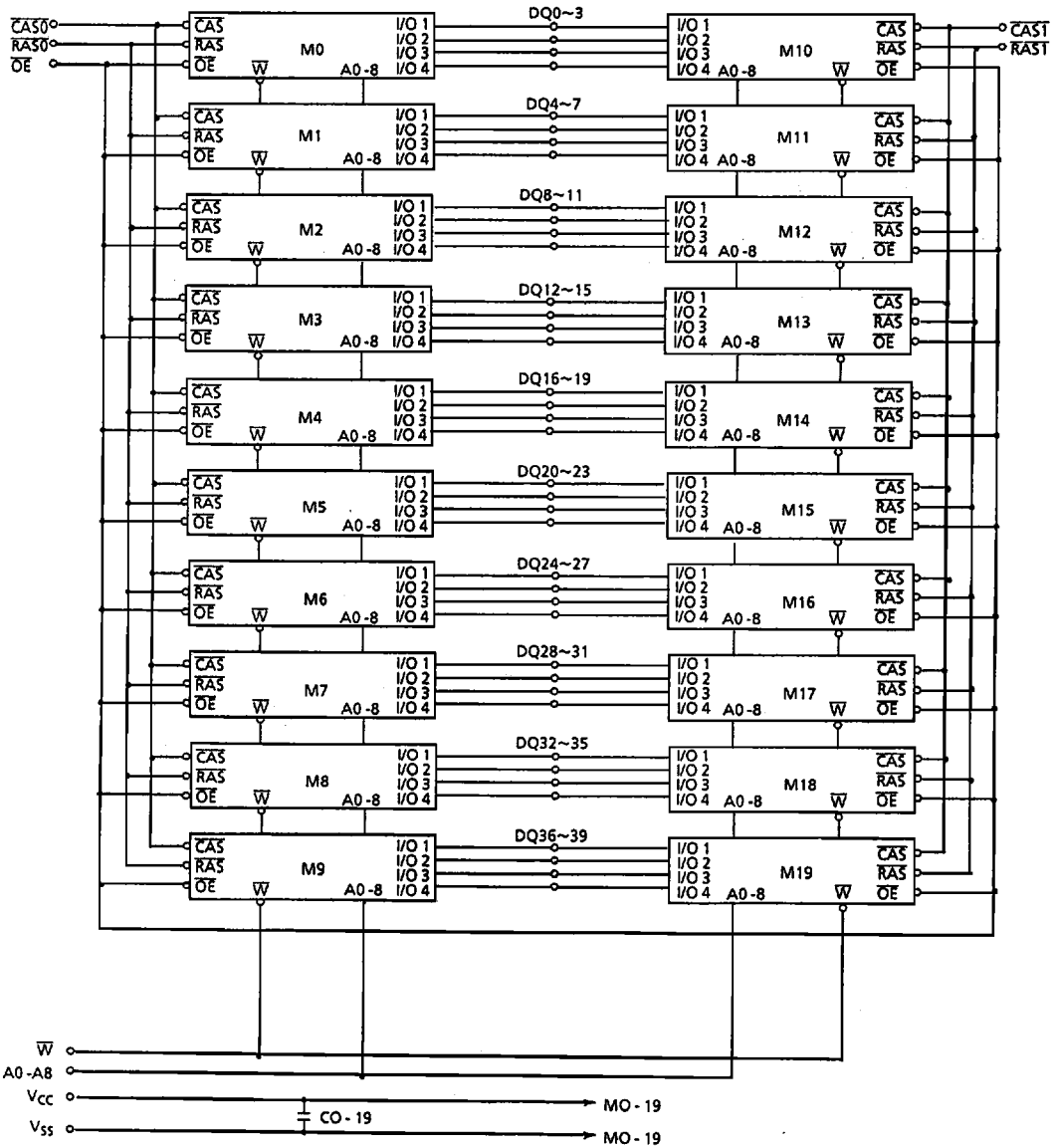
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ39	Data Inputs/Outputs
$\overline{CAS0}$,$\overline{CAS1}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS1}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	NC	44	$\overline{RAS0}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	NC	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

	-60	-70	-80	-10
PD0	NC	NC	NC	NC
PD1	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	12.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxx-60	–	920	mA	3, 4 5
		THMxxxxx-70	–	820		
		THMxxxxx-80	–	720		
		THMxxxxx-10	–	620		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	40	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THMxxxxx-60	–	920	mA	3,5
		THMxxxxx-70	–	820		
		THMxxxxx-80	–	720		
		THMxxxxx-10	–	620		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	THMxxxxx-60	–	620	mA	3, 4 5
		THMxxxxx-70	–	620		
		THMxxxxx-80	–	520		
		THMxxxxx-10	–	420		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	20	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxx-60	–	920	mA	3,5
		THMxxxxx-70	–	820		
		THMxxxxx-80	–	720		
		THMxxxxx-10	–	620		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 200	200	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	–	95	–	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	0	25	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	20	–	25	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	0	–	0	–	ns	

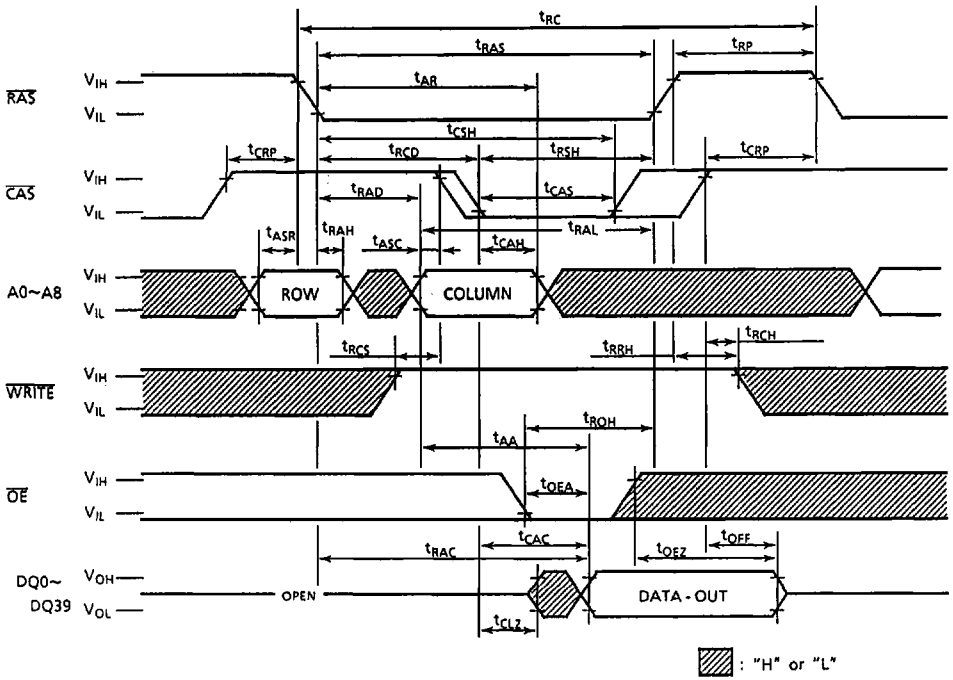
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	130	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	110	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	-	60	pF
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	-	50	pF
CDQ	I/O Capacitance (DQ0~DQ39)	-	20	pF

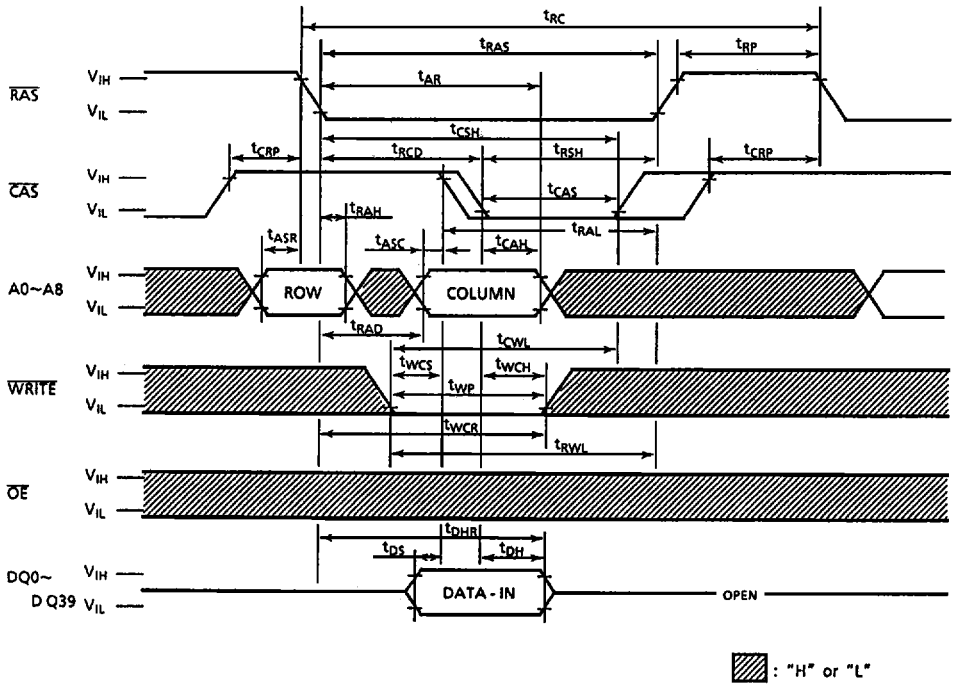
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWD} \geq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

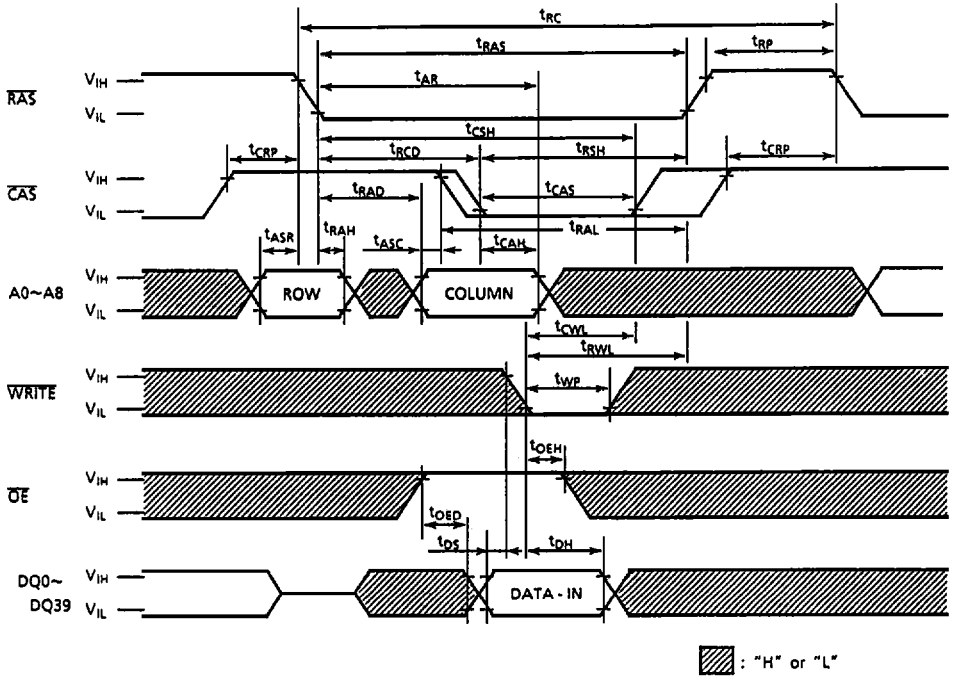
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tAR
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH
VIL
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A8
VIH
VIL
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
VIH
VIL
tROH
tAA
OE
VIH
VIL
tOEA
tCAC
tOFF
tRAC
tOEZ
DQ0~
DQ39
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

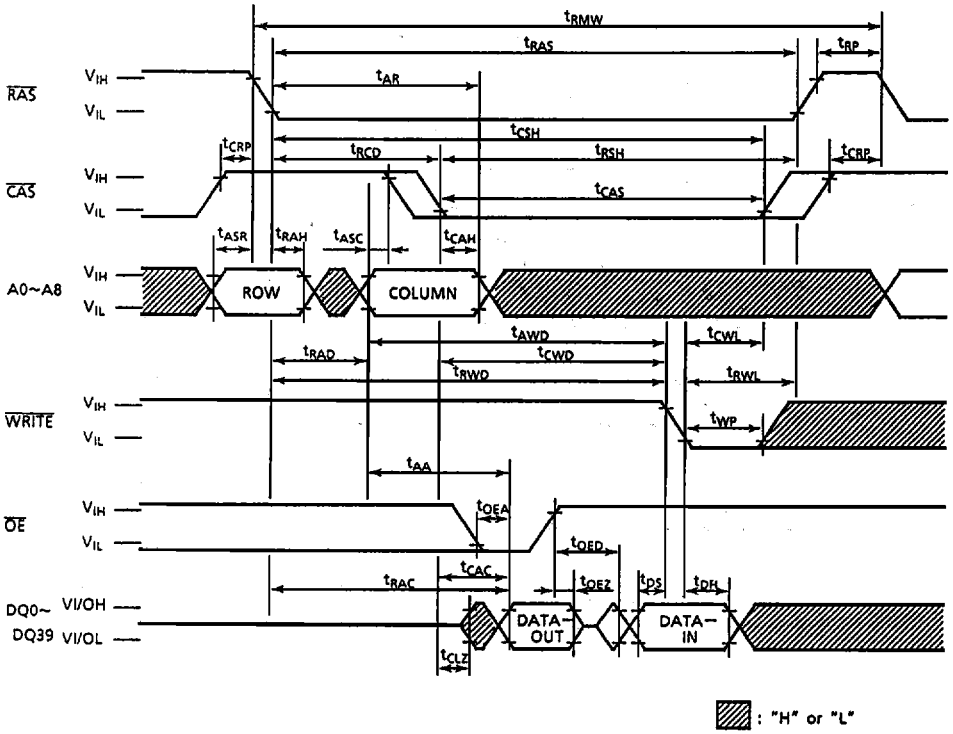
WRITE CYCLE (EARLY WRITE)



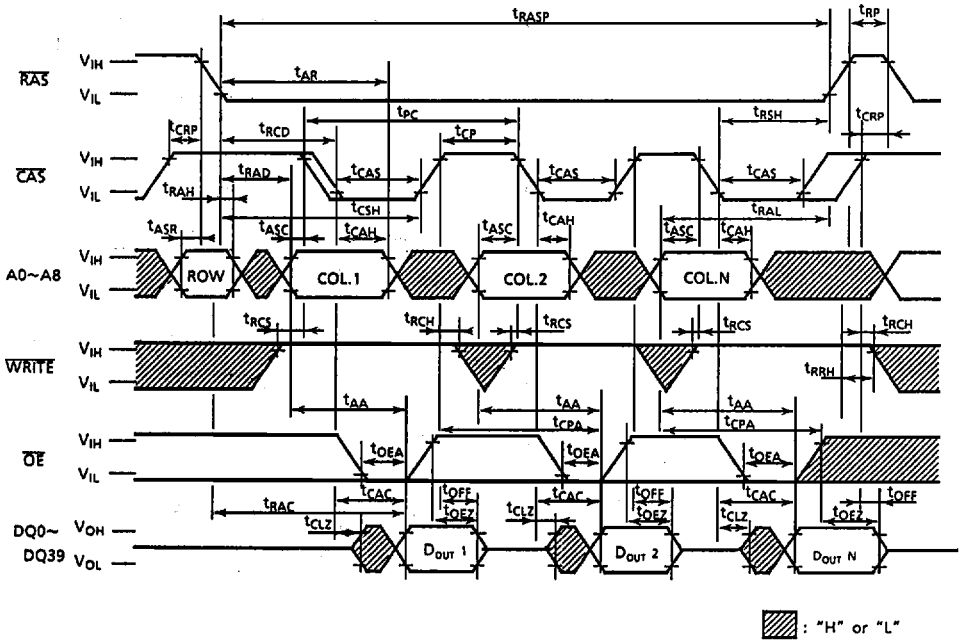
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



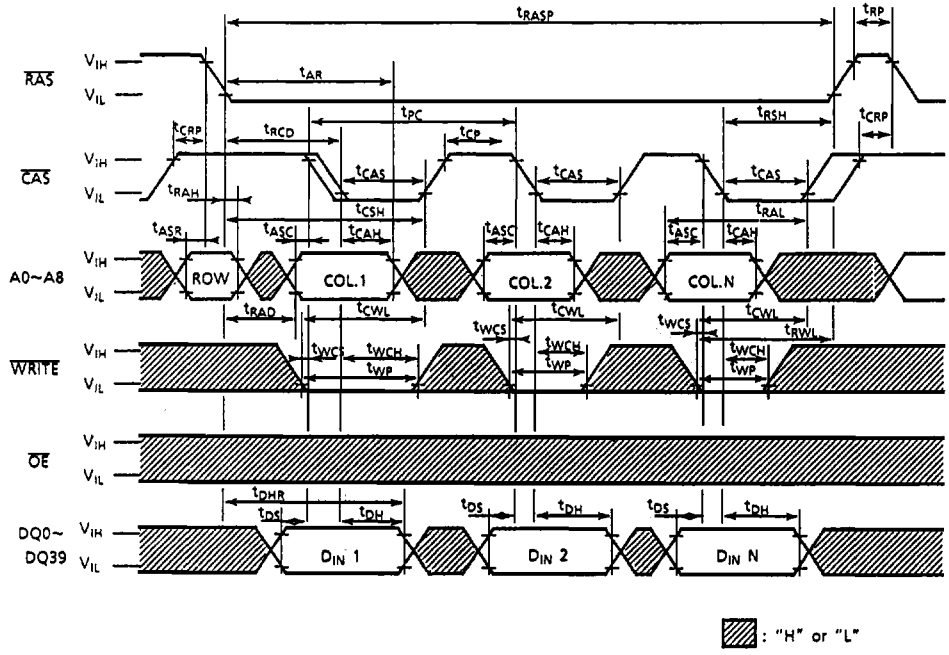
READ-MODIFY-WRITE CYCLE



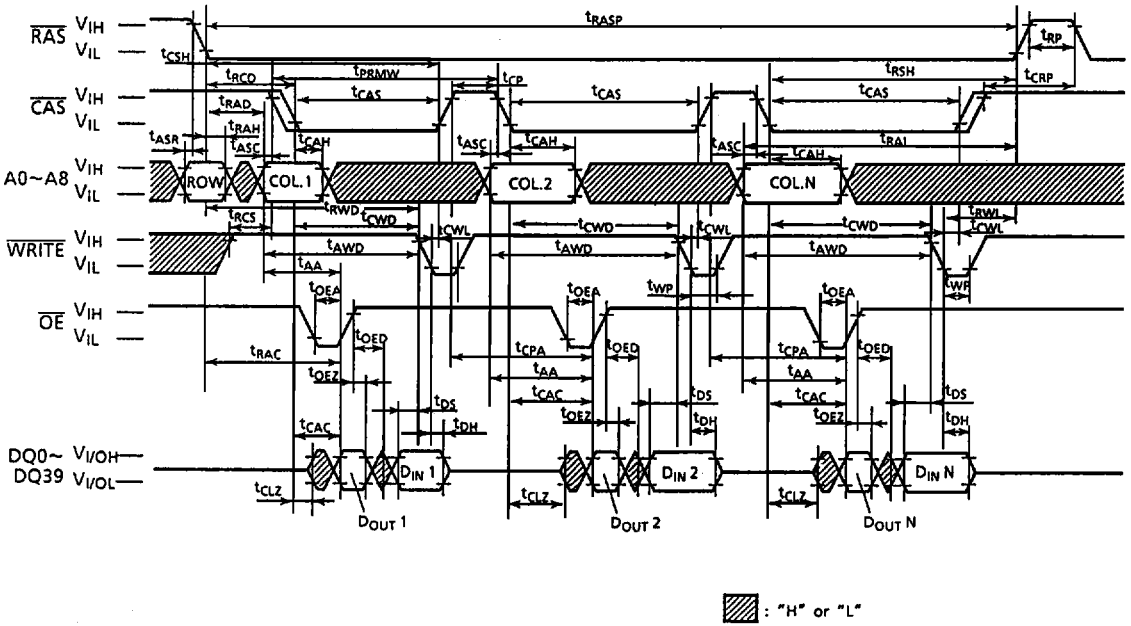
FAST PAGE MODE READ CYCLE



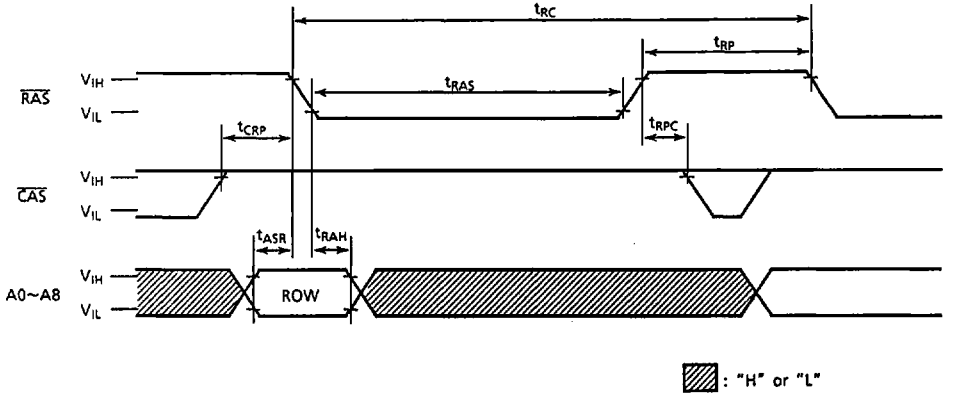
FAST PAGE MODE WRITE CYCLE



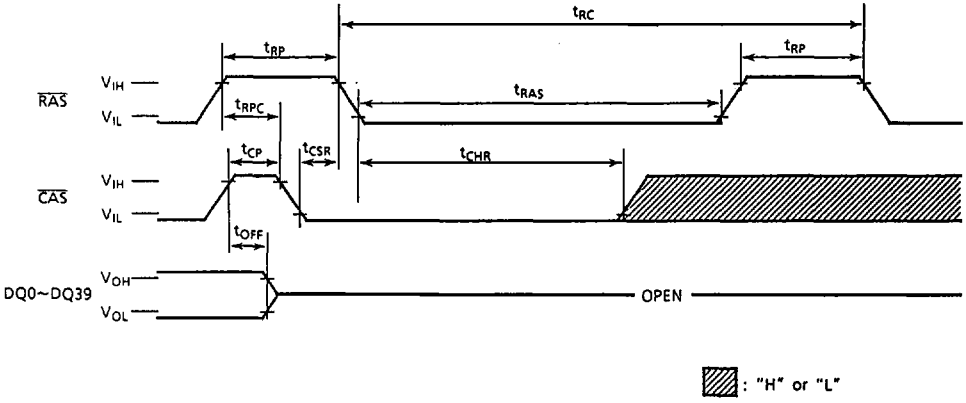
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



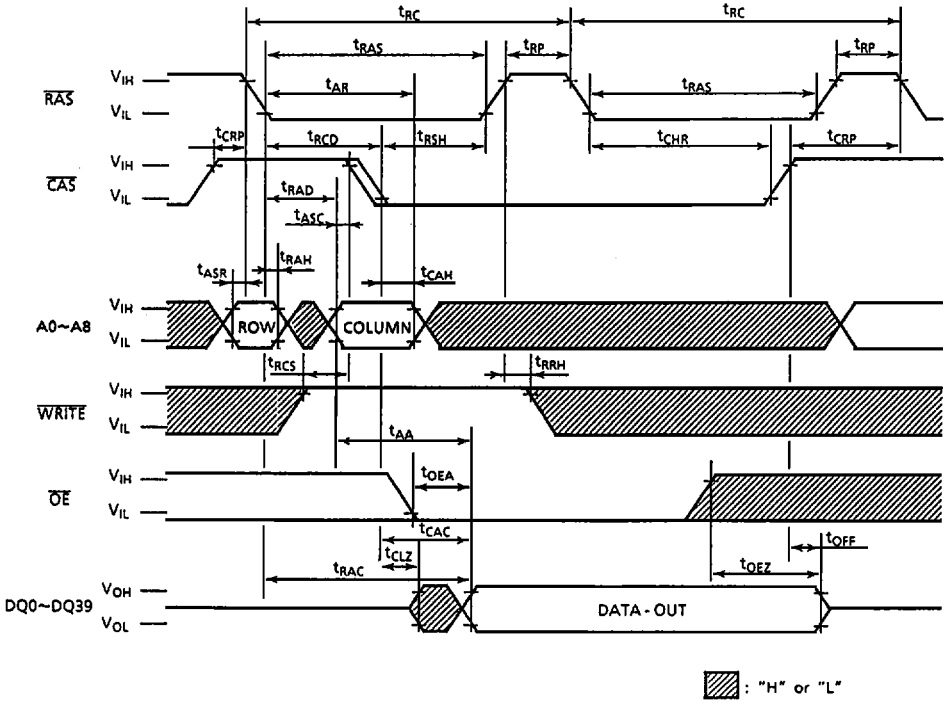
RAS ONLY REFRESH CYCLE



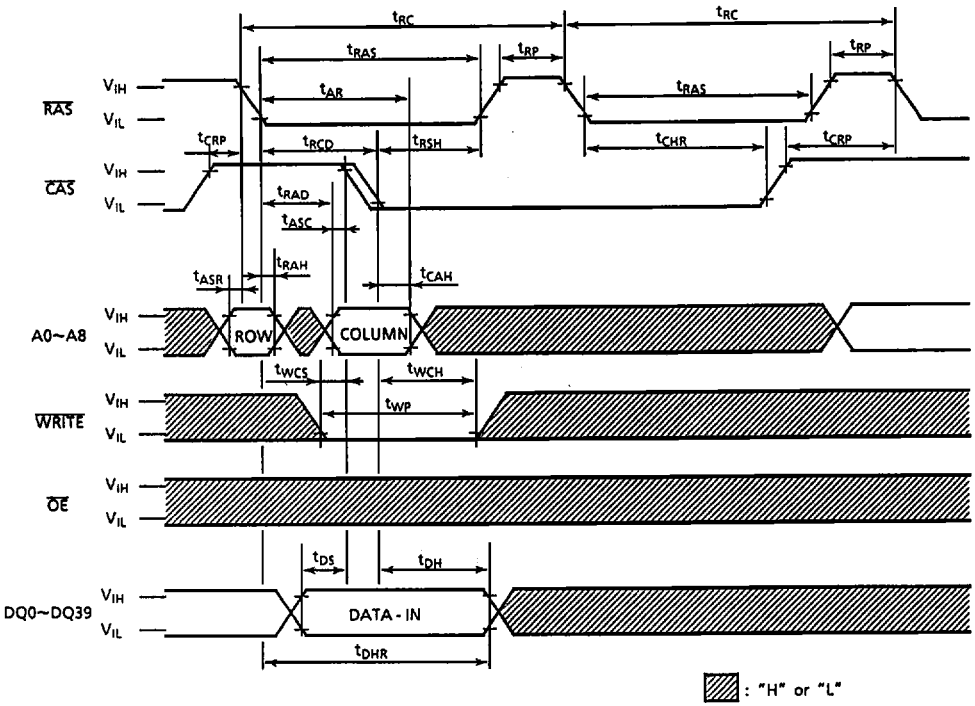
CAS BEFORE RAS REFRESH CYCLE



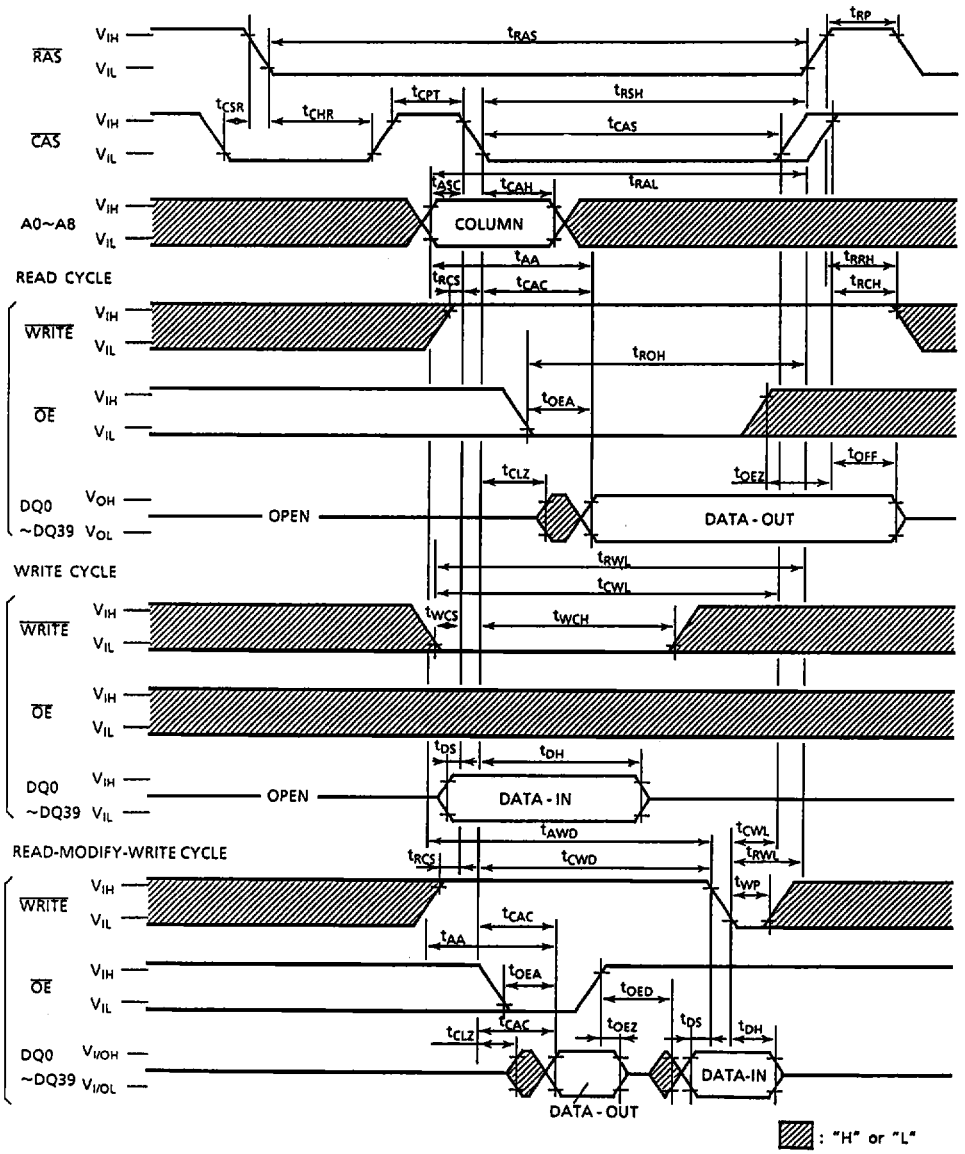
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

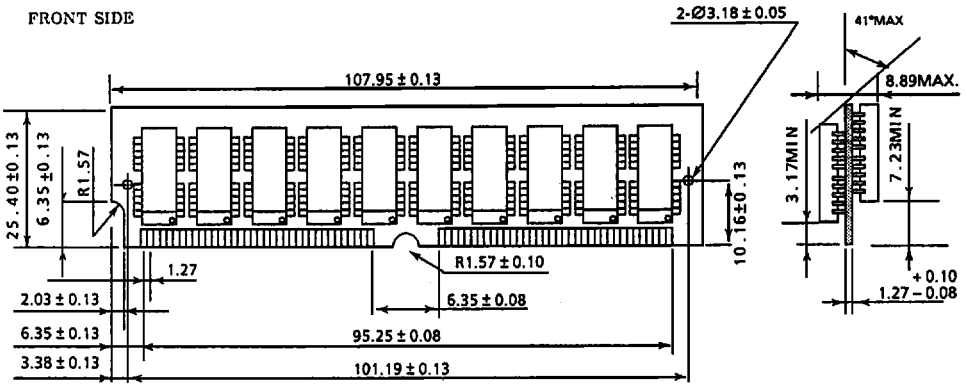


OUTLINE DRAWINGS

• THM405120ASG/BSG (JEDEC OUTLINE)

Unit in mm

FRONT SIDE



BACK SIDE