TOSHIBA MOS MEMORY PRODUCT

1,048,576 WORDS × 8 BIT
DYNAMIC RAM MODULE

THM81000S/L-10/12

DESCRIPTION

The THM81000S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000J on the printed circuit board.

The THM81000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

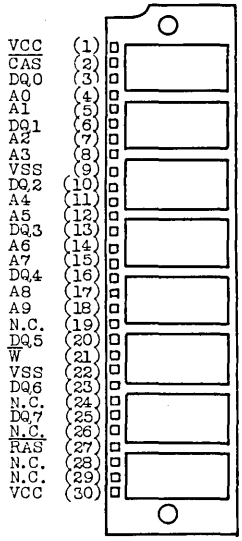
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81000S/L-10	THM81000S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	45ns
t_{RC}	Cycle Time	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10%
- Low power
  2,640mW MAX. Operating (THM81000S/L-10)
  2,200mW MAX. Operating (THM81000S/L-12)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

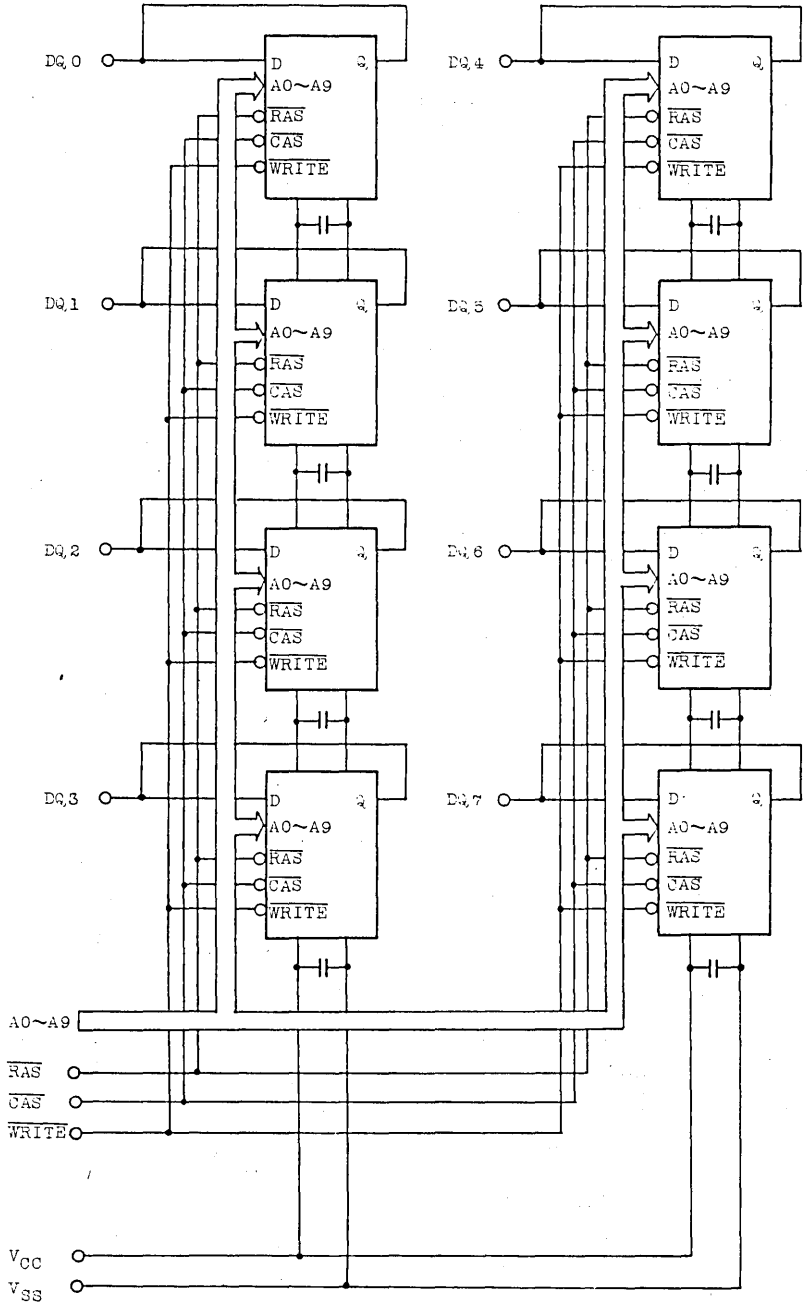
(TOP VIEW)



PIN NAMES

A0 ∿ 9	Address Inputs
DQ0 ∿ 7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature . Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81000S/L-10	-	480	mA	3, 4
		THM81000S/L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81000S/L-10	-	480	mA	3
		THM81000S/L-12	-	400		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM81000S/L-10	-	320	mA	3, 4
		THM81000S/L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81000S/L-10	-	480	mA	3
		THM81000S/L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81000S/L-10		THM81000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{PC}	Fast Page Mode Cycle Time	55		70		ns	
t_{RAC}	Access Time from $\overline{RAS}$		100		120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$		35		45	ns	8, 13
t_{AA}	Access Time from Column Address		50		60	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		50		65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		5		ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35		45		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35		45		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	20		25		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	10

ELECTRICAL CHARACTERISTIC AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81000S/L-10		THM81000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	10
t_{WCH}	Write Command Hold Time	20		25		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{WP}	Write Command Pulse Width	20		25		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		ns	
t_{DS}	Data Set-Up Time	0		0		ns	11
t_{DH}	Data Hold Time	20		25		ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{REF}	Refresh Period		8		8	ms	
t_{WCS}	Write Command Set-Up Time	0		0		ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30		30		ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50		60		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20		ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)		60	pF
C_{DQ}	I/O Capacitance (DQ0 ∿ DQ7)		15	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

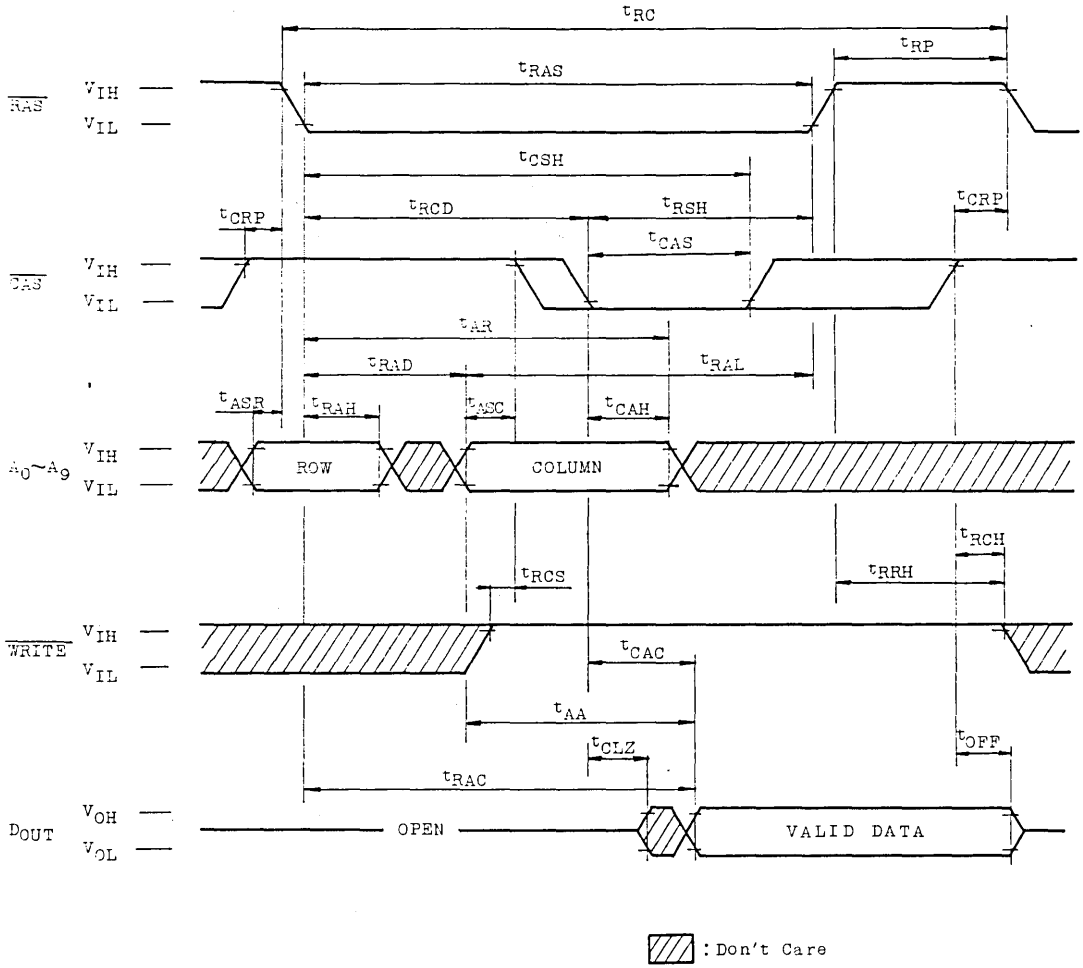
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

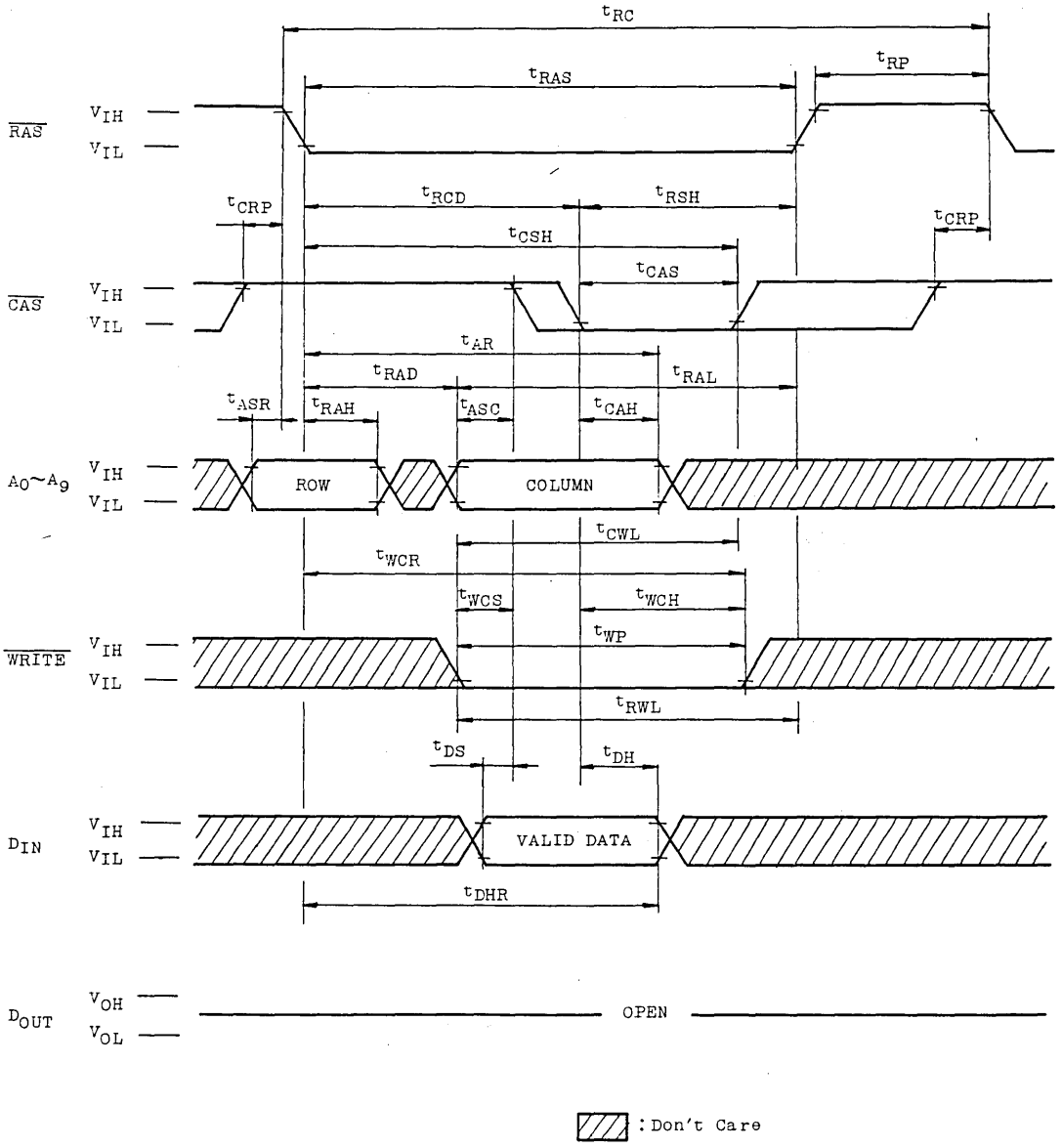
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

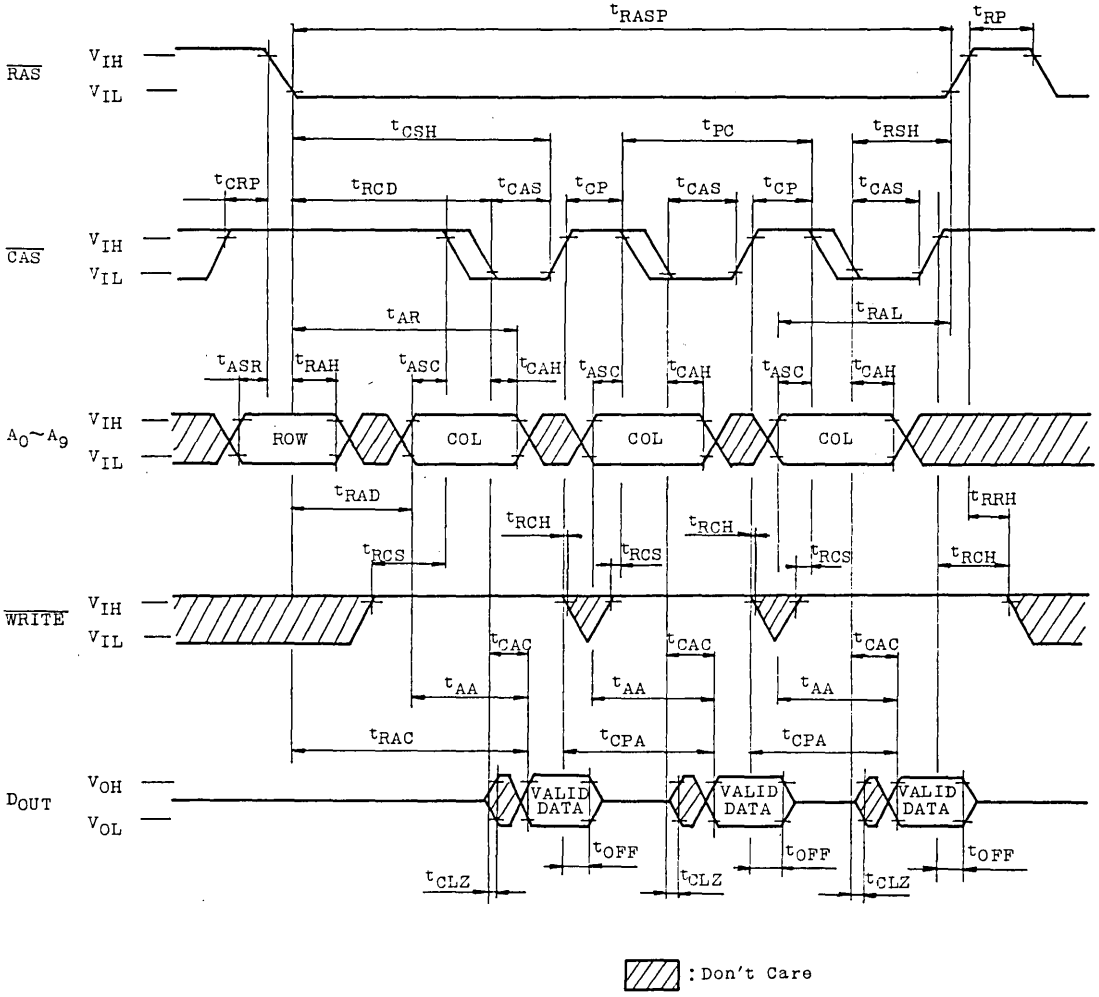
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: Don't Care

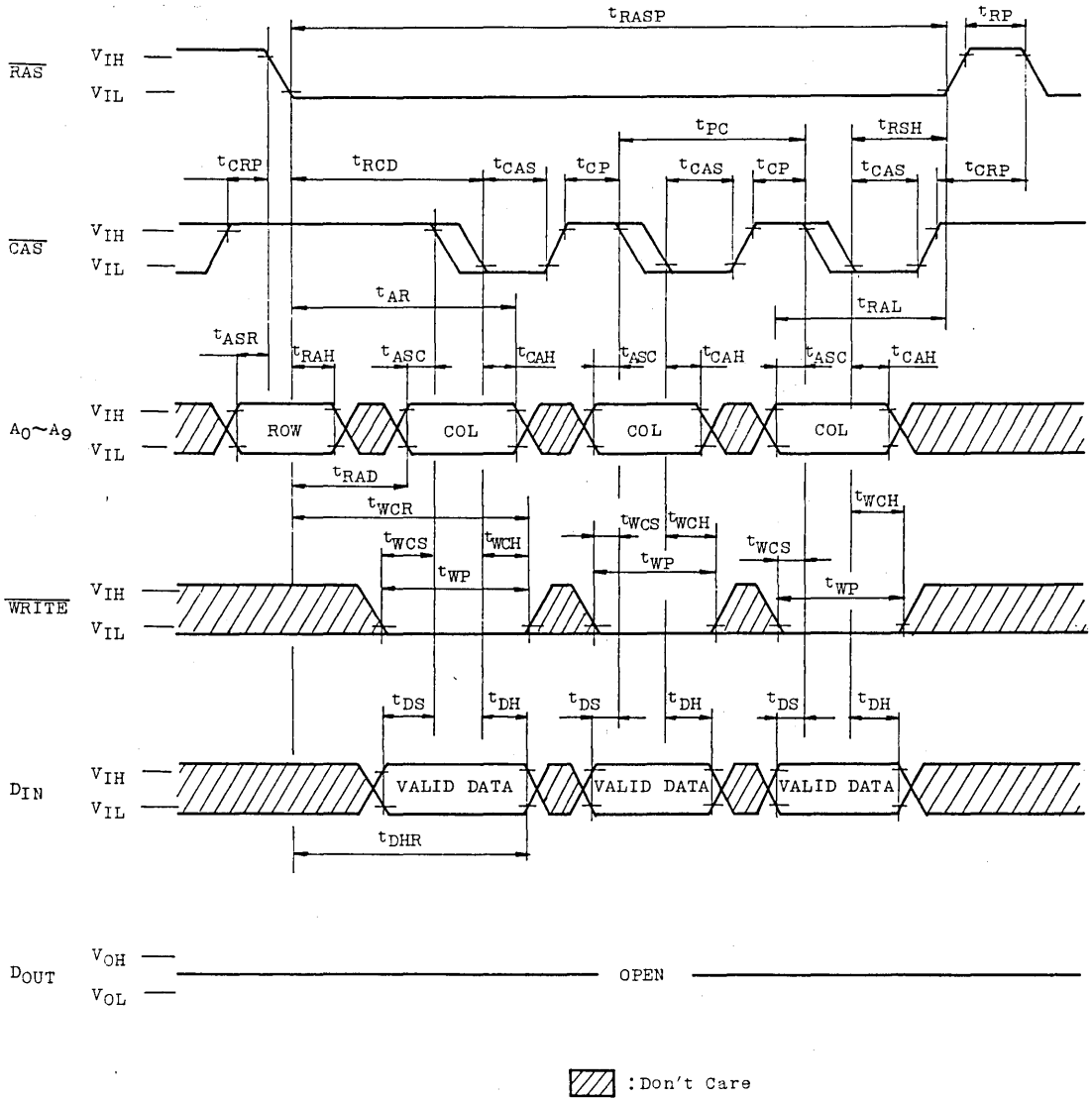
EARLY WRITE CYCLE



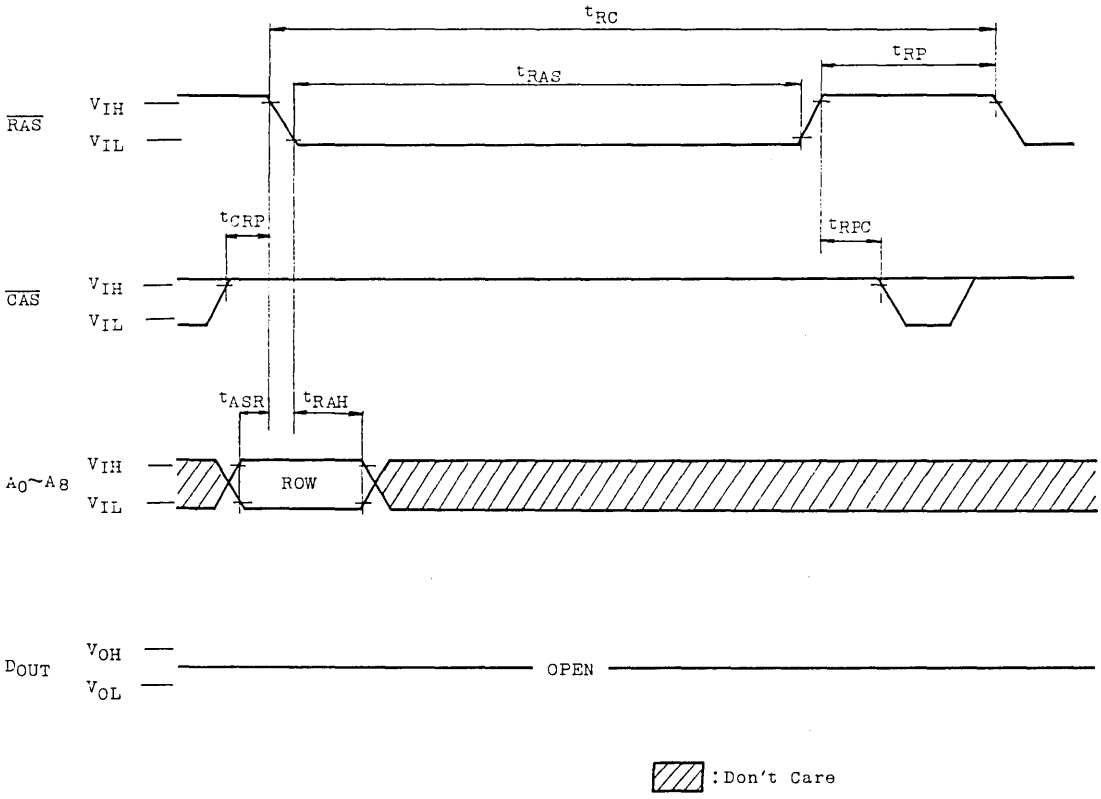
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

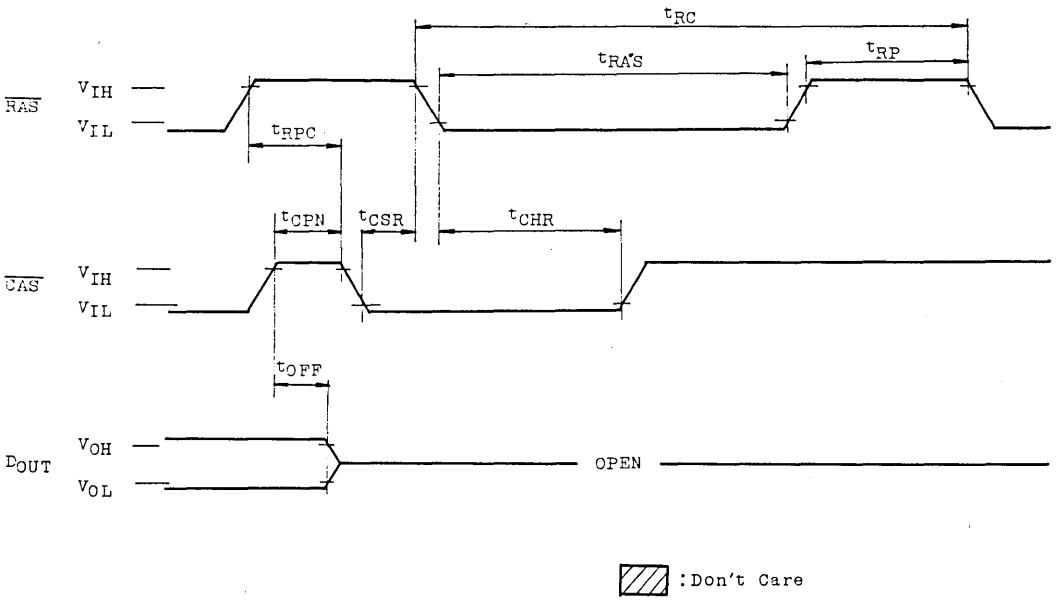


$\overline{RAS}$ ONLY REFRESH CYCLE



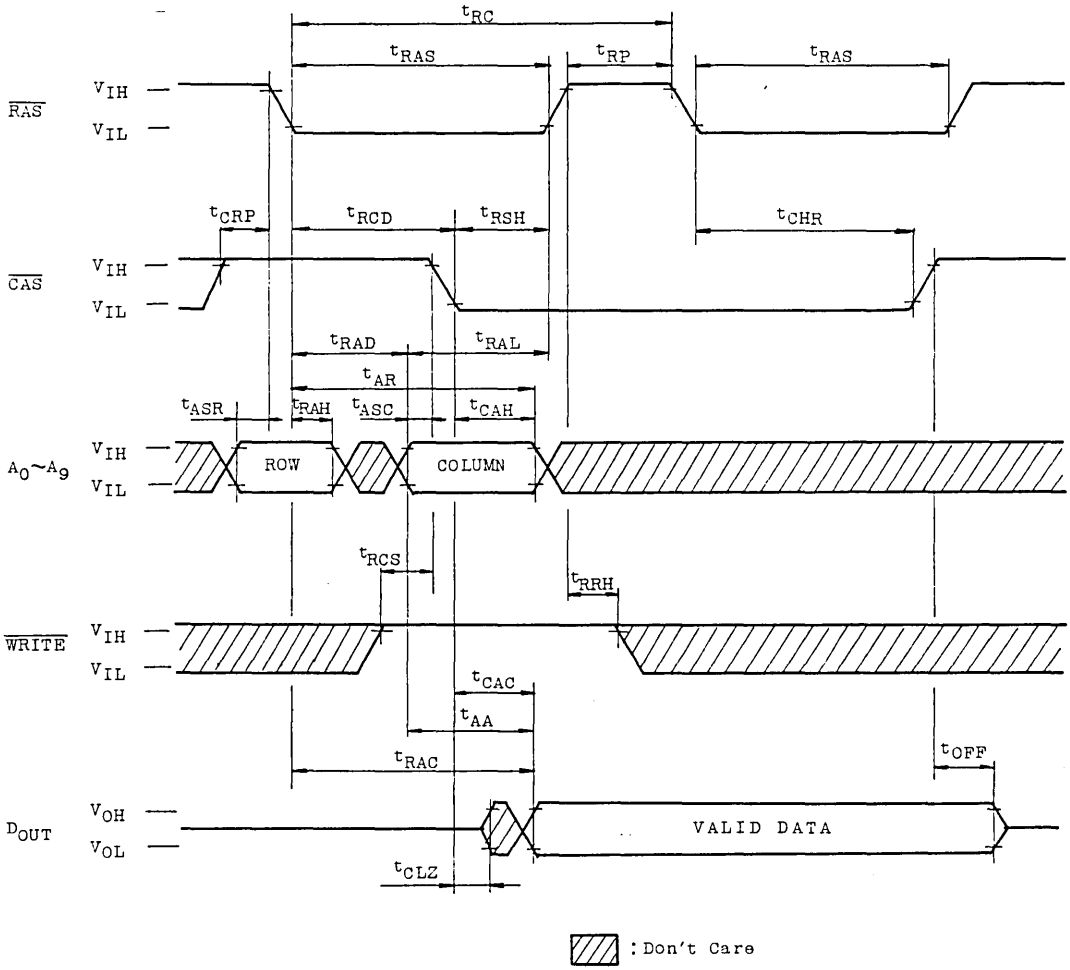
Note: $\overline{WRITE}$=Don't care, A9=Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

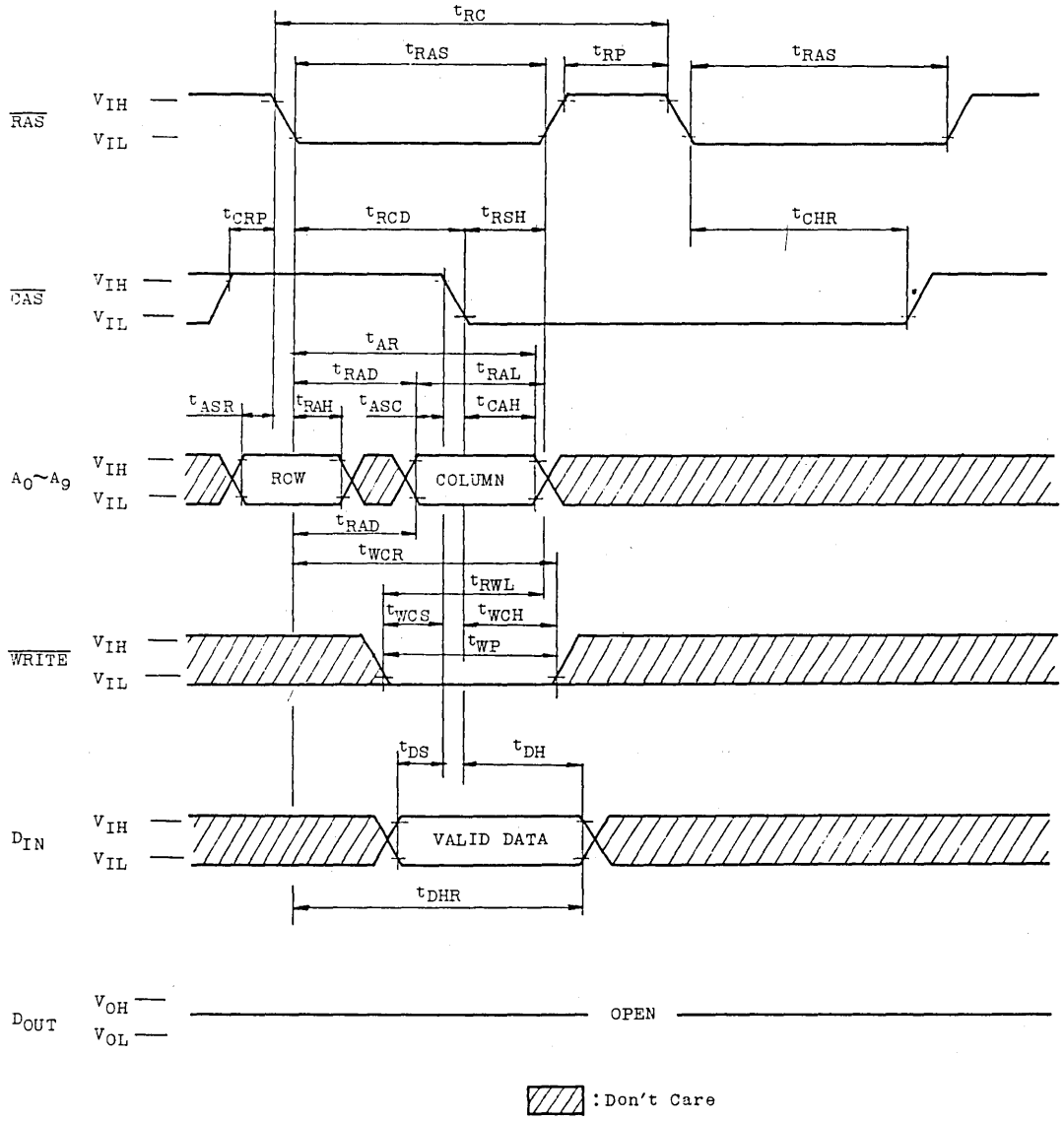


Note: $\overline{WRITE}$=Don't care, A0 ∿ A9=Don't care

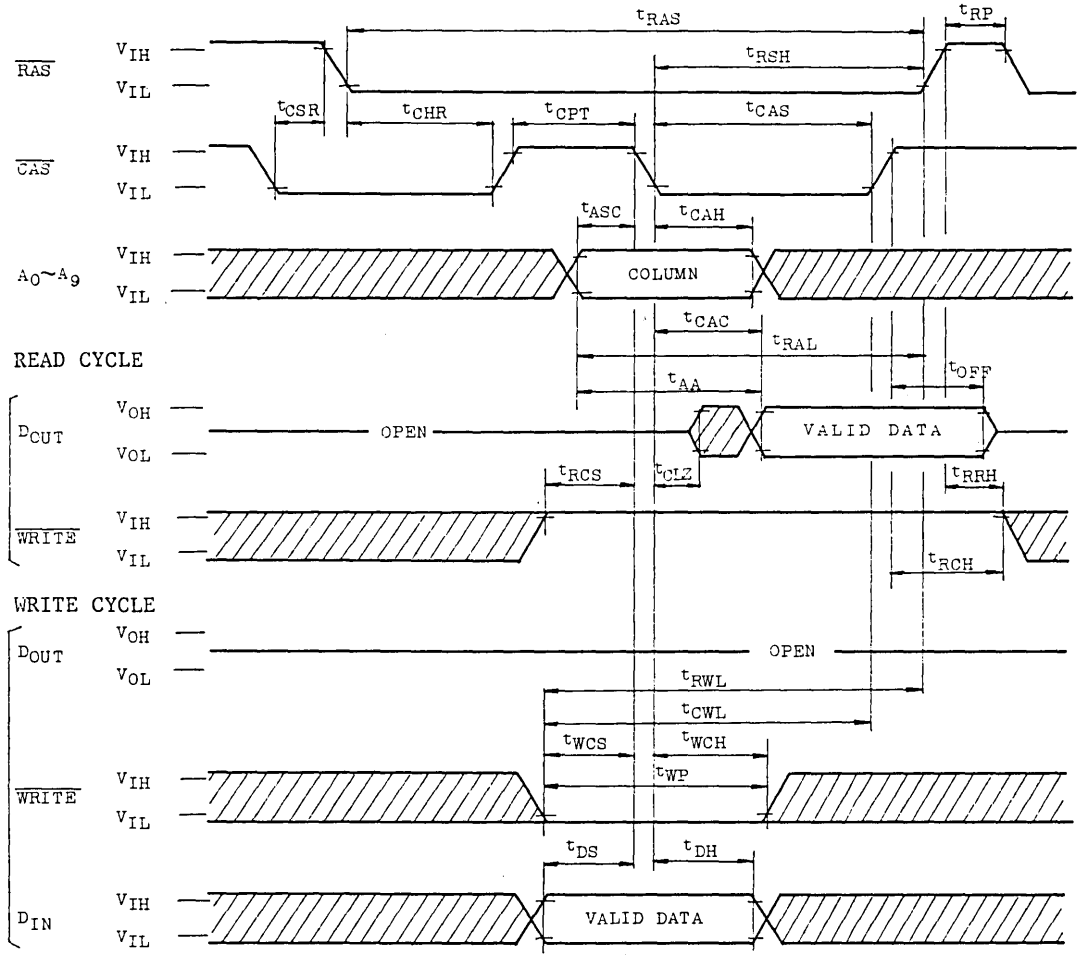
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



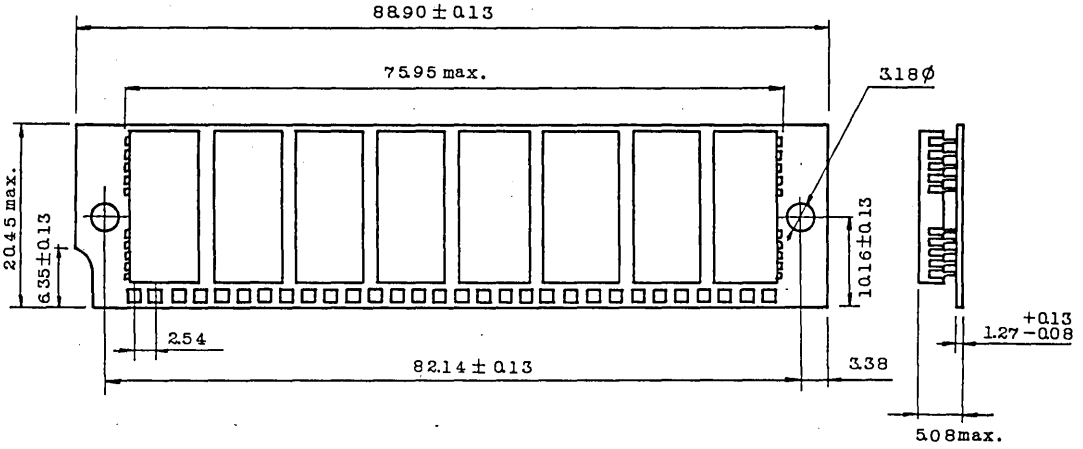
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

• THM81000S

Unit in mm



• THM81000L