4,194,304 WORDS×9 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM94000S/L is a 4,194,304 words by 9 bits dynamic RAM module which assembled 9 pcs of TC514100J on the printed circuit board.

The THM94000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

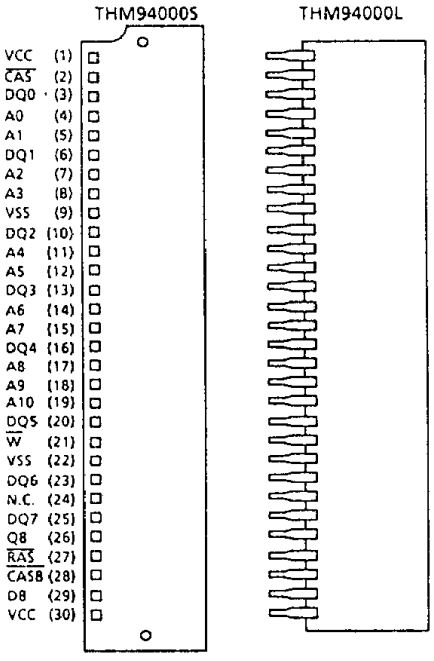
FEATURES

- 4,194,304 words by 9 bits organization
- Fast access time

		THM94000S/L-80	THM94000S/L-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power 4,950mW MAX. Operating (THM94000S/L-80)
  4,212mW MAX. Operating (THM94000S/L-10)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms

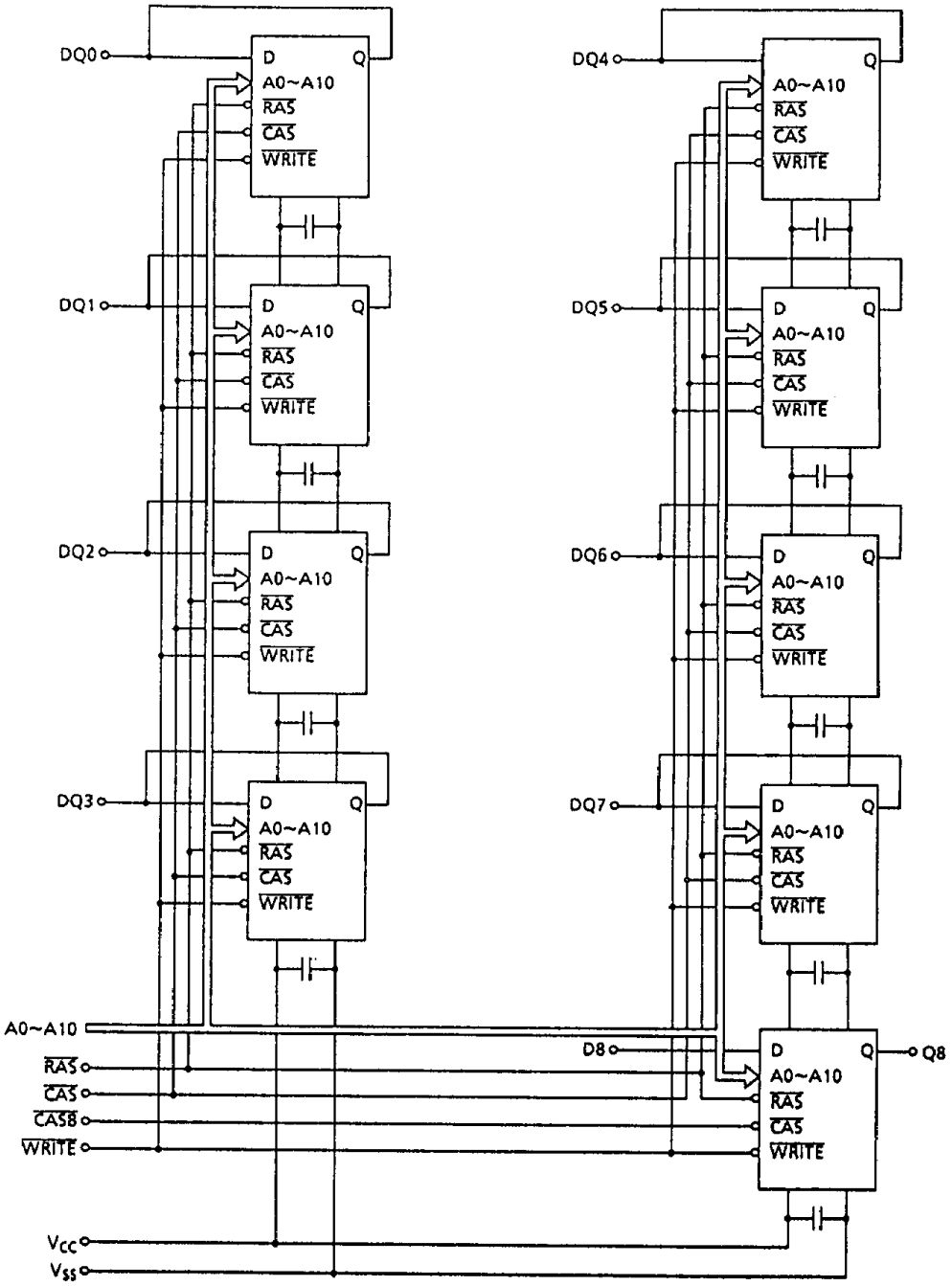
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A10	Address Inputs
DQ0~DQ7	Data Inputs/Outputs
D8	Data Inputs
Q8	Data Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM×××××−80	–	900	mA	3, 4
		THM×××××−10	–	765		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ V_{IH}: t_{RC} = t_{RC} MIN.)	THM×××××−80	–	900	mA	3
		THM×××××−10	–	765		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM×××××−80	–	540	mA	3, 4
		THM×××××−10	–	450		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		–	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM×××××−80	–	900	mA	3
		THM×××××−10	–	765		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		−90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		−20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = 5 − mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM94000S-80		THM94000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM94000S-80		THM94000S-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	11
t_{DH}	Data Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

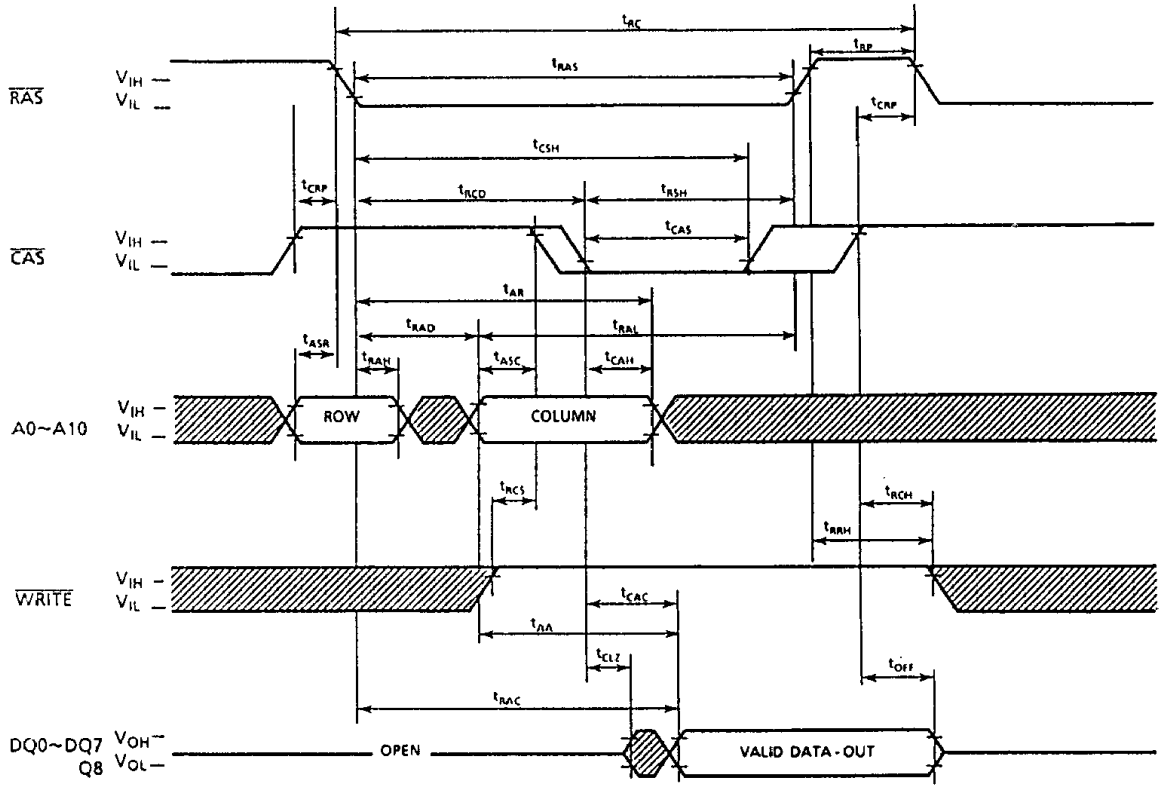
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	–	10	pF
C_{DQ}	I/O Capacitance (DQ0~DQ7)	–	15	pF
C_Q	Output Capacitance (Q8)	–	10	pF

NOTES:

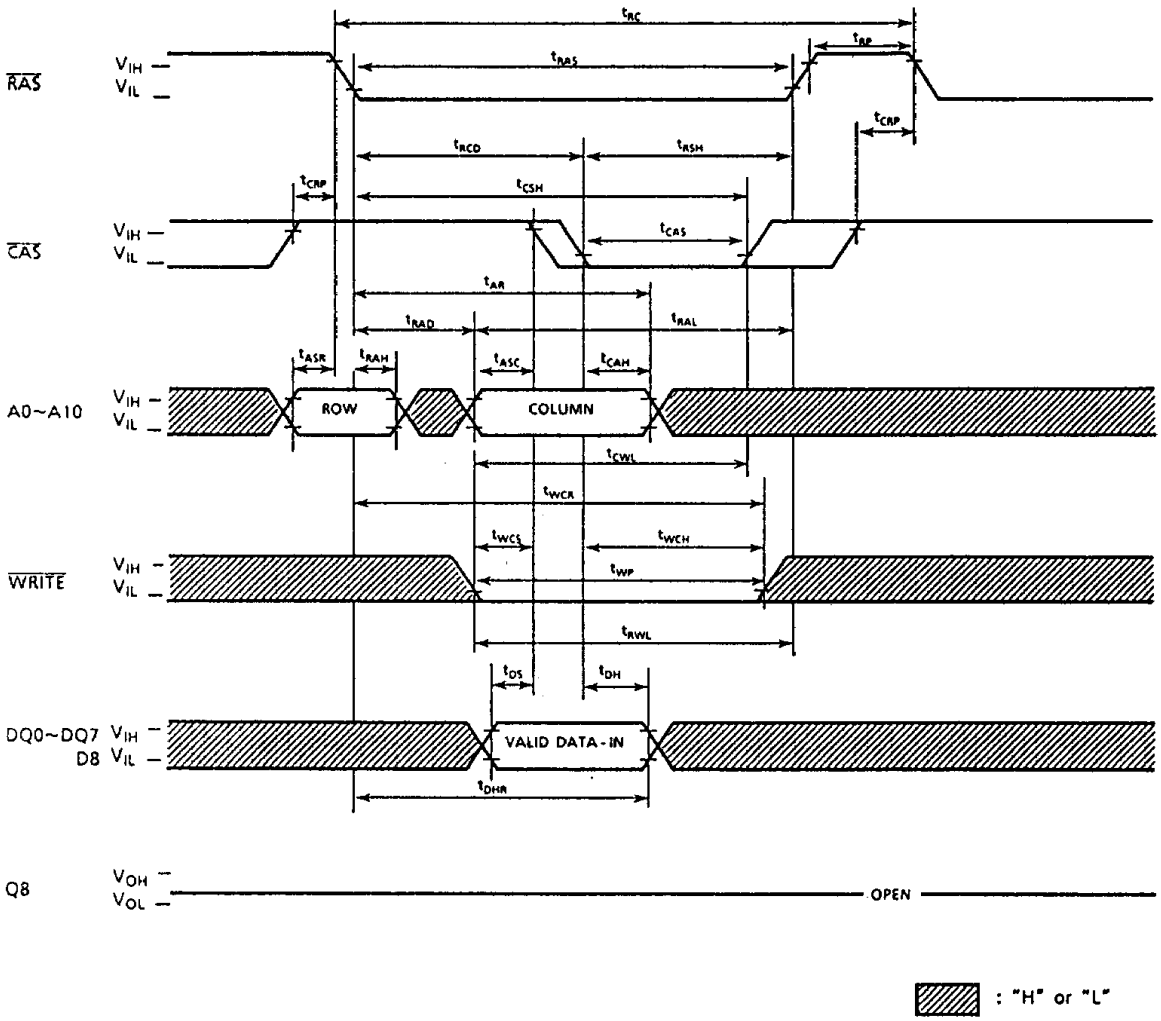
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

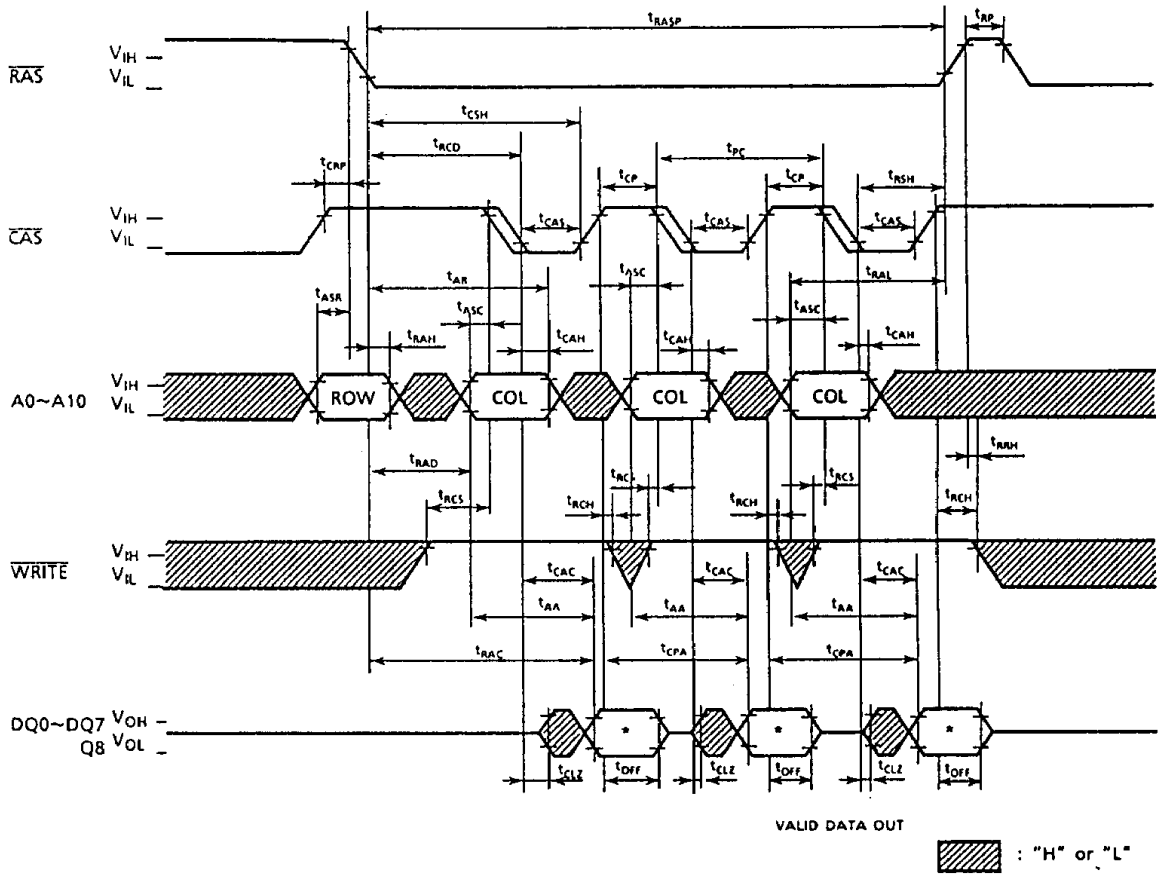


: "H" or "L"

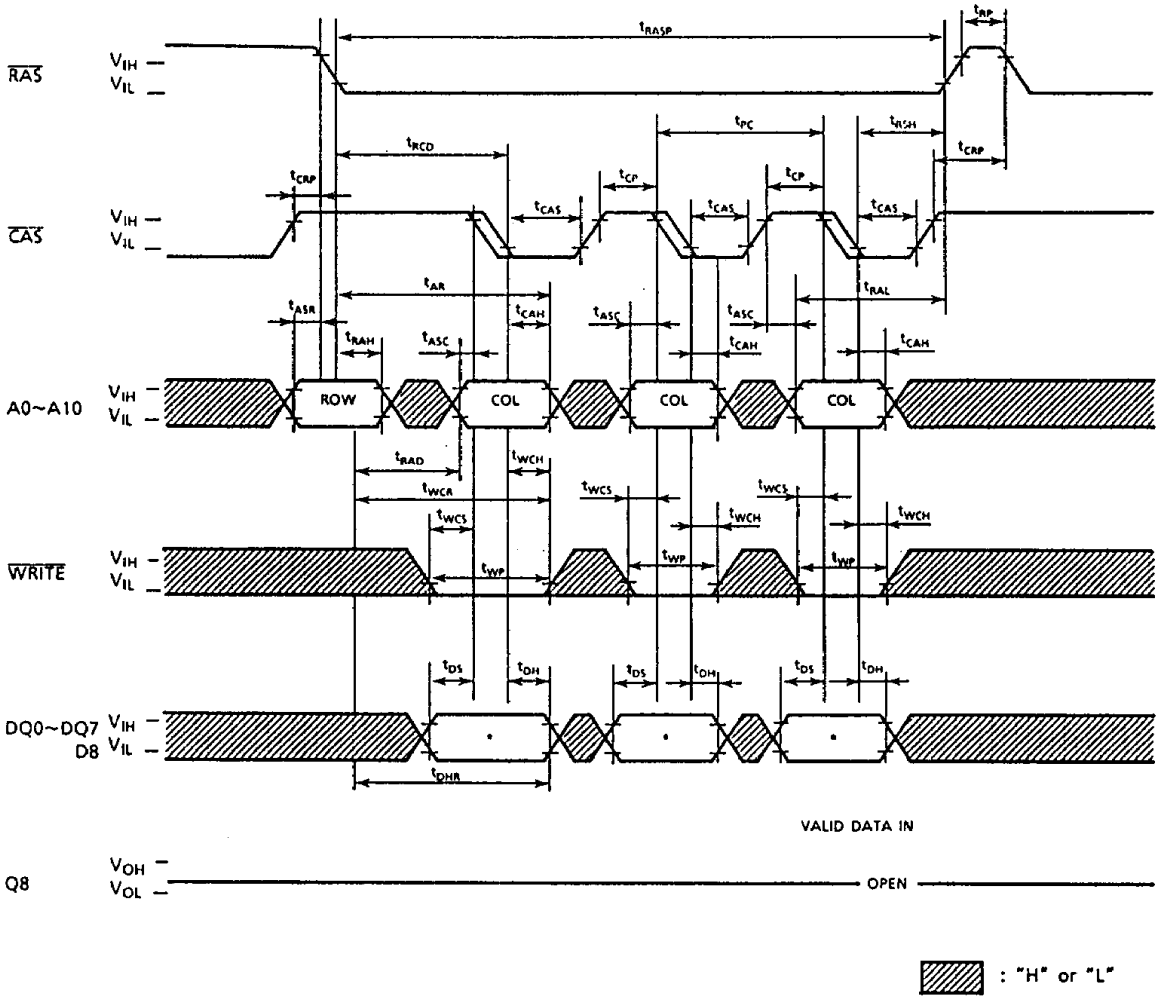
EARLY WRITE CYCLE



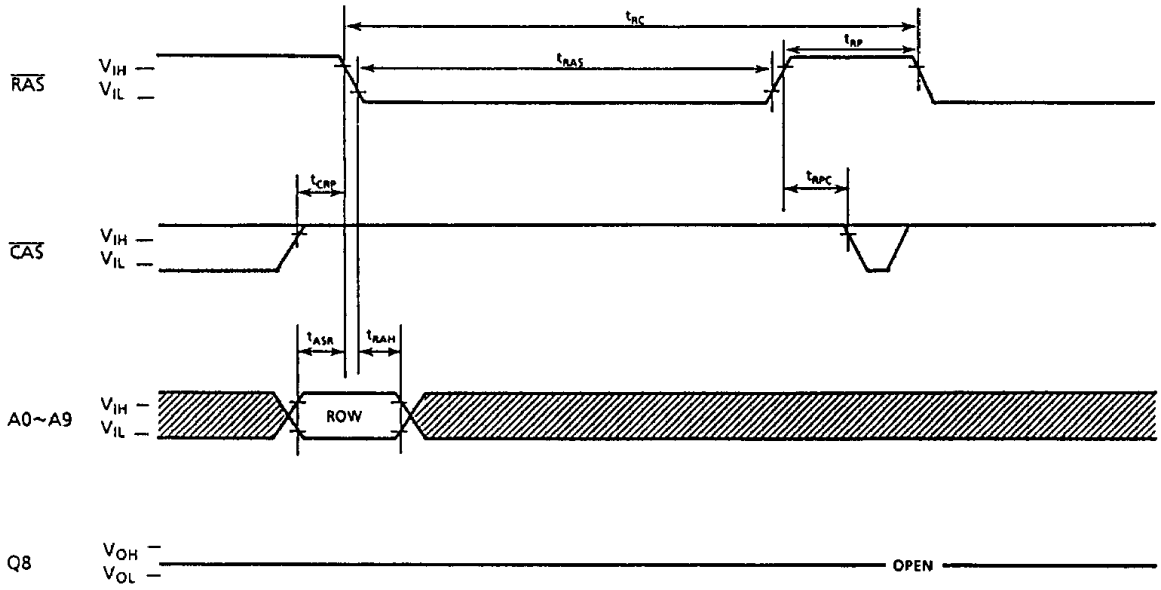
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



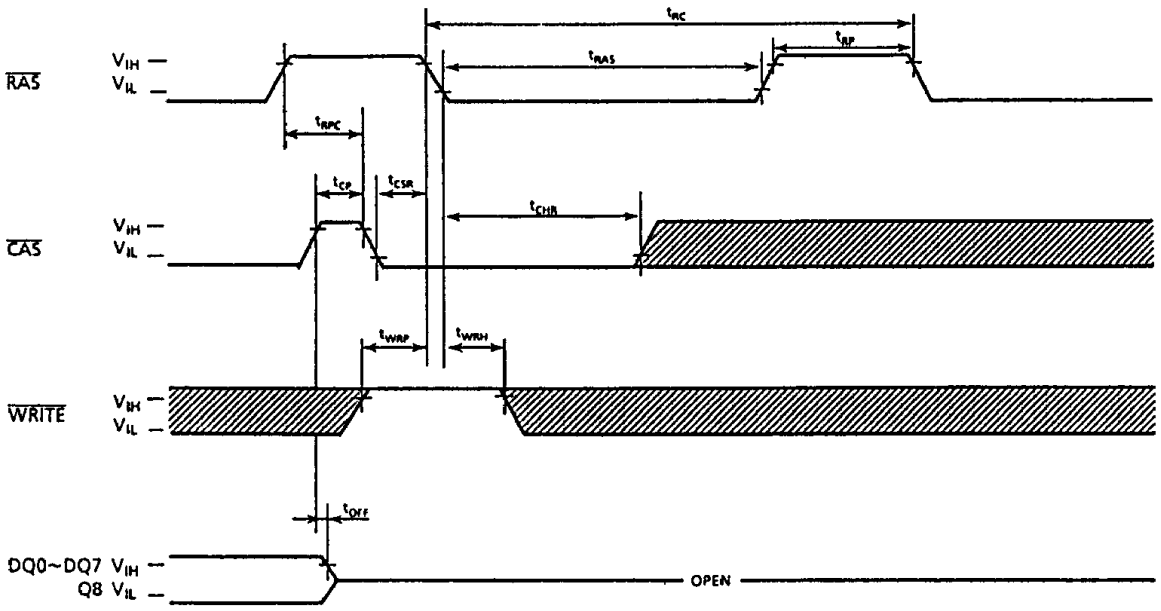
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, A10 = "H" or "L"

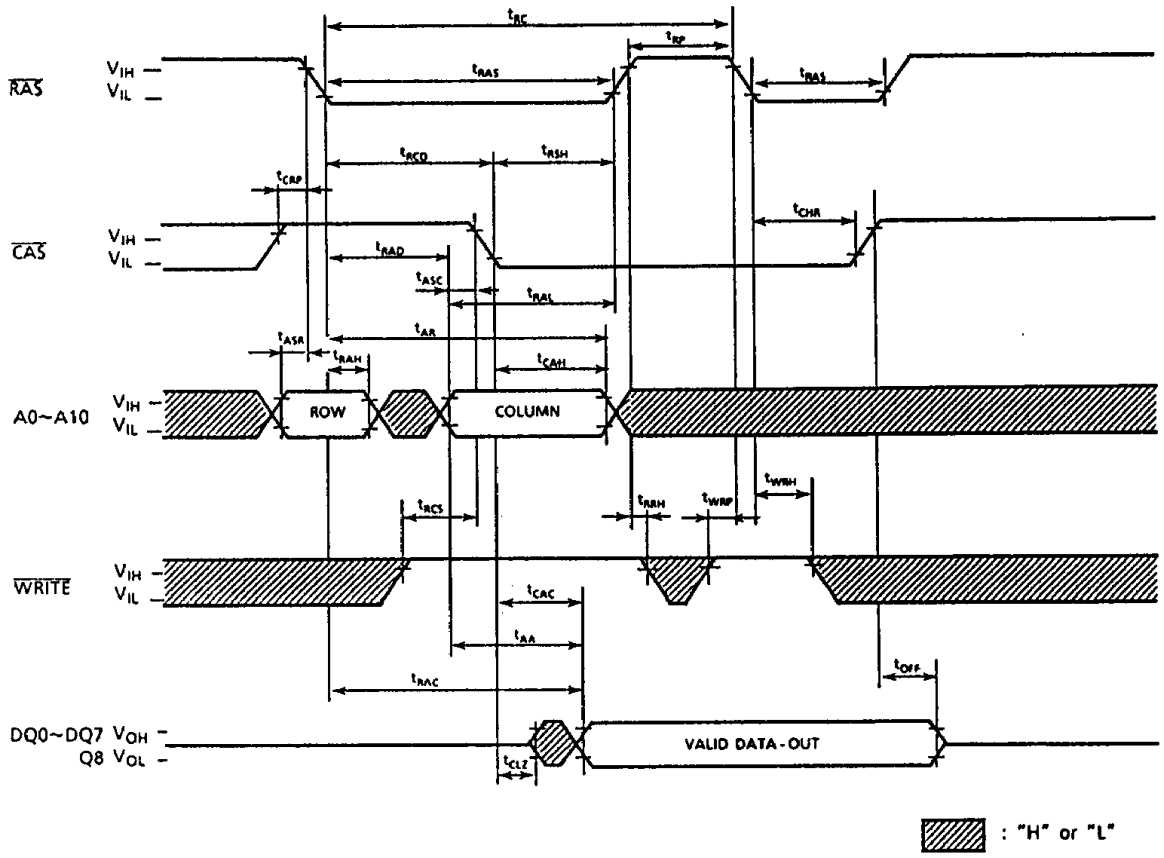
▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

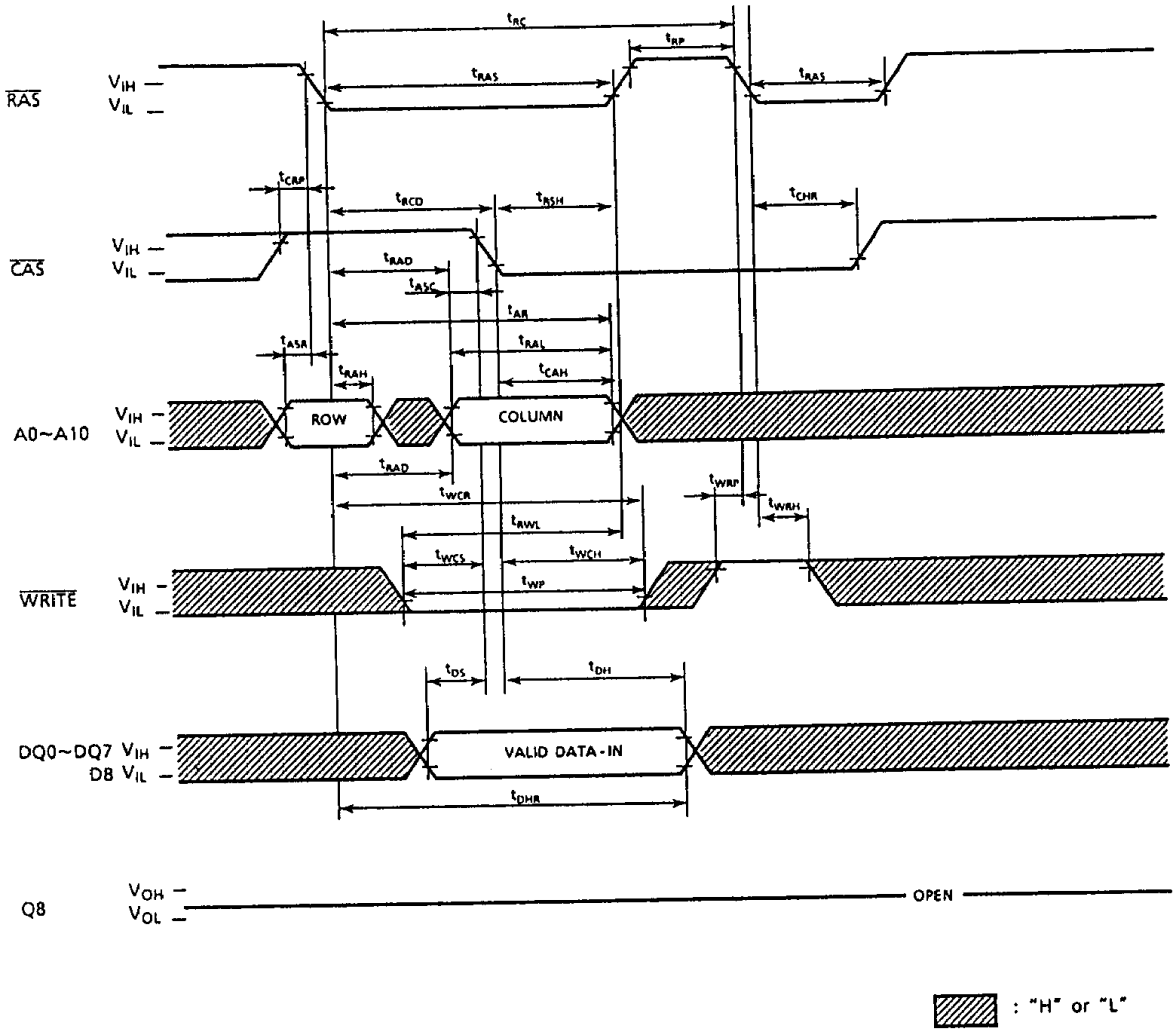


Note: A0~A10 = "H" or "L"

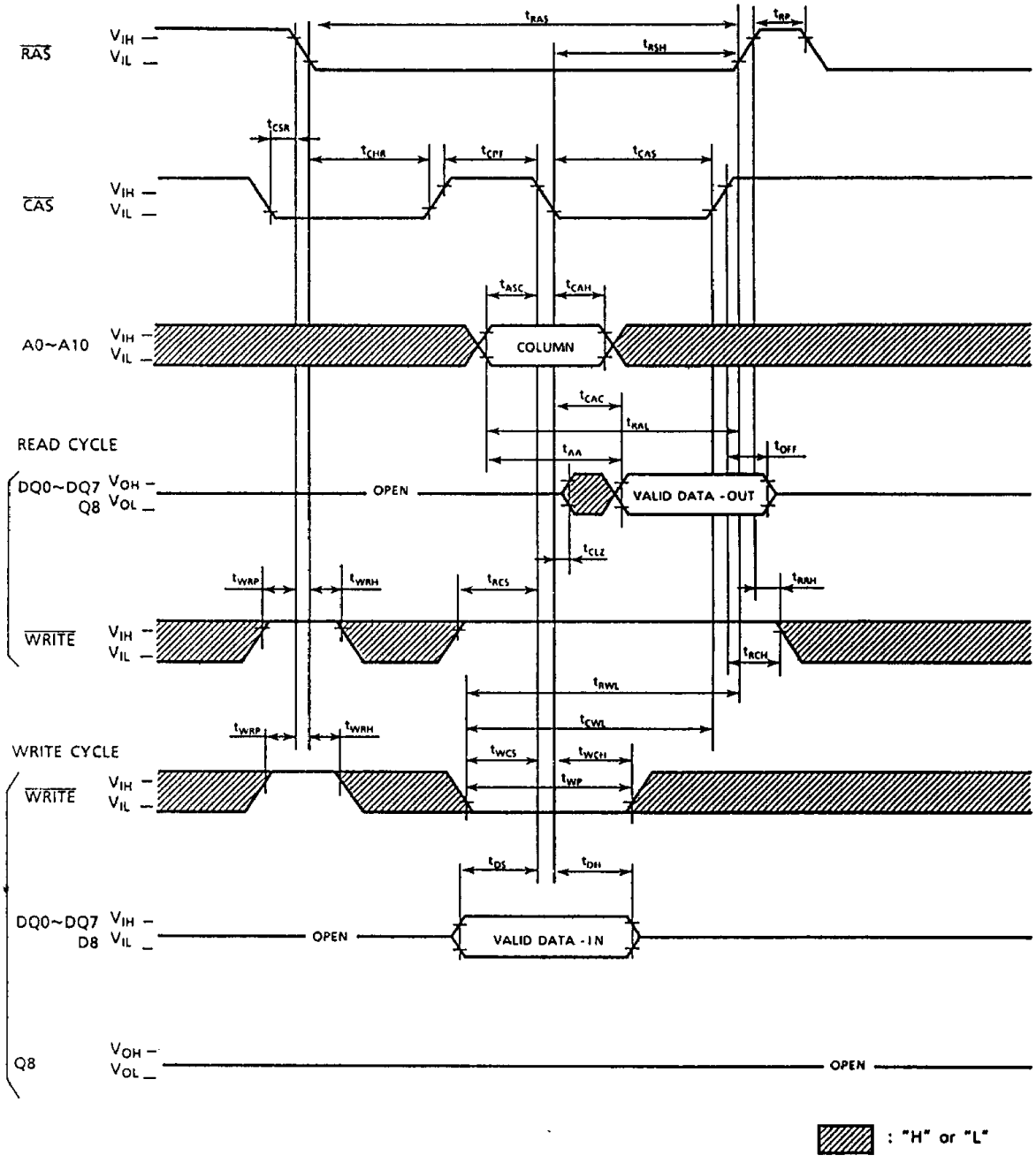
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



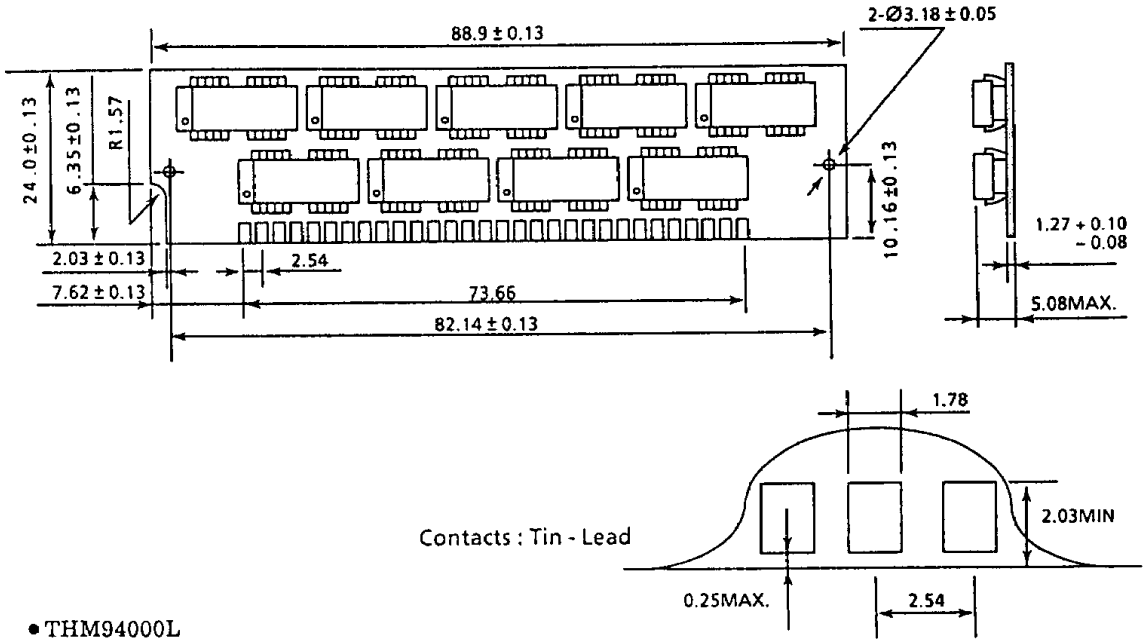
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

Unit in mm

• THM94000S



• THM94000L