SLOS387 − DECEMBER 2001

ADSL (ISDN) CENTRAL OFFICE LINE INTERFACE DRIVER/RECEIVER

FEATURES

- **15-V Single Supply Operation**
- **Low 1.1-W Total Power Consumption**
  - **0.9-W Transmit Drivers**
  - **0.2-W Receive Channel**
- **Active Termination Differential Line Drivers**
  - **No Line Matching Resistors Reduces Output Voltage and Power Consumption by up to 50%**
- **Integrated Differential Receivers**
- **Includes Analog Filters in Both Transmit and Received Channels**
- **Multiple Power Saving Modes**
  - **Bias Current Is Adjustable in 20% Increments to Allow Lower Power Modes for Short Line Lengths**

APPLICATIONS

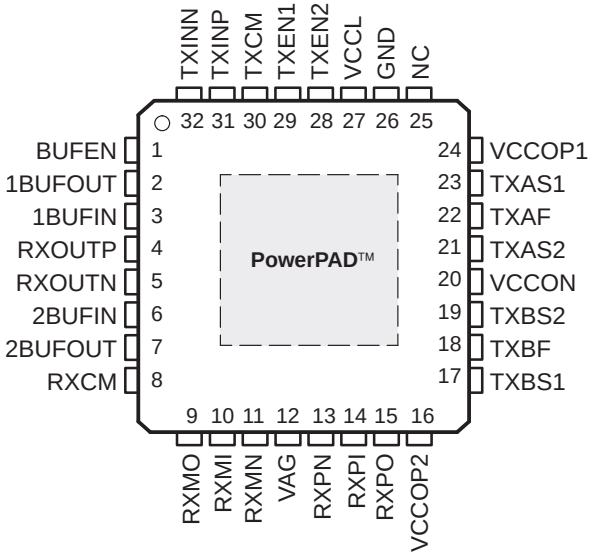
- **Full Rate ADSL Central Office Line Driver/Receiver for ISDN Applications**

DESCRIPTION

The THS7103 is a low power differential ADSL (ISDN) central office line interface driver/receiver. It features active termination drivers that eliminate the matching resistors required with traditional ADSL line drivers. Removal of the matching resistors allows the THS7103 to output nearly half the output voltage as compared with traditional drivers, resulting in power savings of up to 50%. The lower output voltage levels resulting from the active termination also allow the THS7103 to operate on a single 15-V supply, easing power supply requirements.

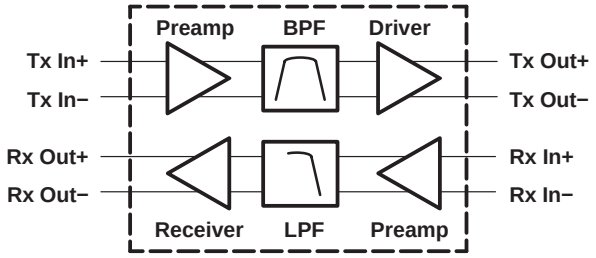
The THS7103 also features integrated differential receivers to reduce the component count on multichannel ADSL line cards. To reduce valuable PCB space further, the transmit path integrates a band-pass filter while the receive path integrates a low-pass filter. Four power-saving modes are featured on this device, allowing it to operate at lower power levels for shorter line lengths.

VFP PACKAGE
(TOP VIEW)



NC − No internal connection

SIMPLIFIED BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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THS7103 Features

Device	Application	Transmit Bandpass Filter†	Receiver Lowpass Filter
THS7103	ADSL (ISDN)	268 kHz to 1.3 MHz	238 kHz

† When used in conjunction with the appropriate input capacitor (see the functional block diagram information)

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PowerPAD (VFP)
0°C to 70°C	THS7103CVFP
−40°C to 85°C	THS7103IVFP

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, VCCL, VCCOP1, VCCOP2 (see Note 1) . . . . . 17 V
Input voltage, V_I . . . . . GND, VCCL, VCCOPx
Output current, I_O (see Note 2): Tx outputs . . . . . 400 mA
Rx outputs . . . . . 50 mA
BUF outputs . . . . . 50 mA
Differential input voltage, V_{ID} . . . . . ±3 V
ESD rating: HBM . . . . . 2 kV
CDM . . . . . 500 V
MM . . . . . 200 V
Total power dissipation at (or below) 25°C free-air temperature
(see Note 2) . . . . . See Dissipation Rating Table
Maximum junction temperature, T_J . . . . . 150°C
Operating free-air temperature, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . −40°C to 85°C
Storage temperature, T_{stg} . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 300°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

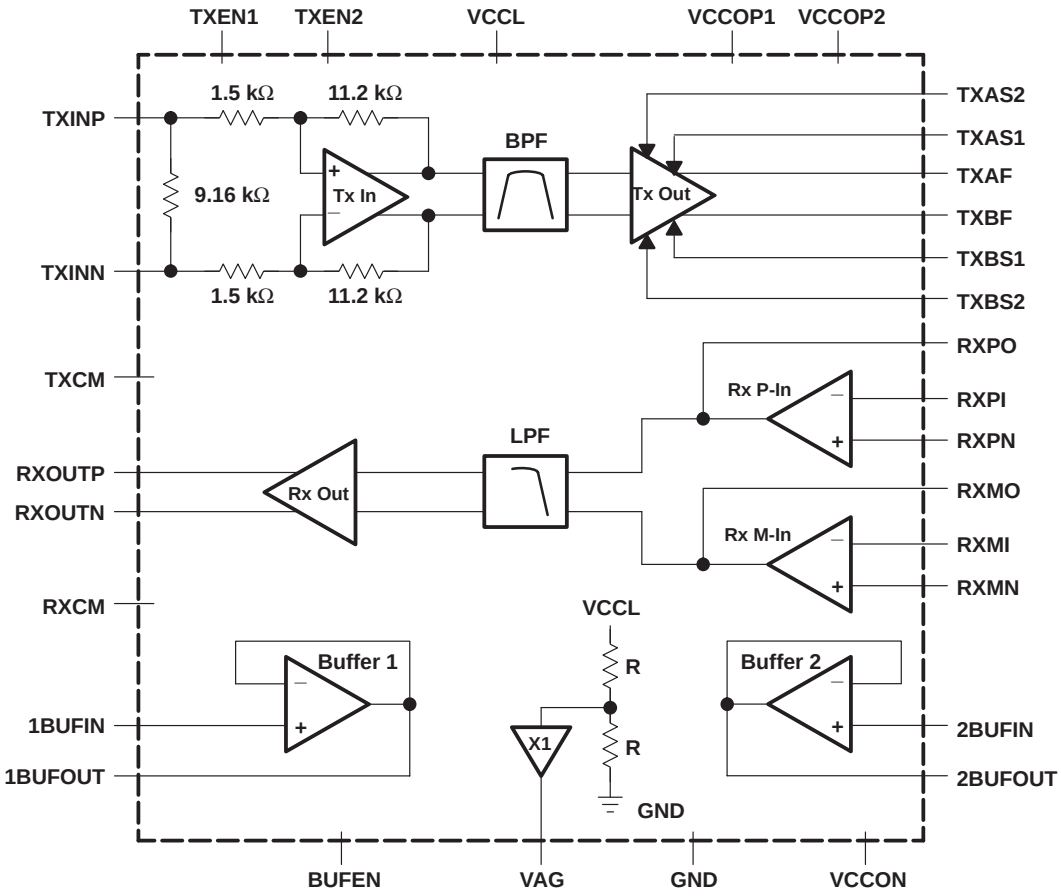
NOTES: 1. VCCL must always be equal to VCCOP1 and VCCOP2
2. The THS7103 incorporates a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device.

DISSIPATION RATING TABLE§

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C¶ POWER RATING	T_A = 70°C¶ POWER RATING	T_A = 85°C¶ POWER RATING
VFP	29.4	0.96	3.57 W	2.04 W	1.53 W

§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a JEDEC standard 4 layer 3 in × 3 in PCB.
¶ The power rating is determined with a junction temperature of 130°C. This is the junction temperature at which distortion begins to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 125°C for the best performance.

functional block diagram



The THS7103 is designed to implement ADSL signals over the same line as ISDN signals at the central office (CO). The THS7103 transmit BPF consists of a low-pass filter and a high-pass filter. The low-pass filter portion of the BPF is comprised of a third order Chebyshev filter with a 0.33-dB passband ripple and a breakpoint frequency of 1.3 MHz. The high-pass portion of the BPF is a 0.33-dB passband ripple Chebyshev with a breakpoint frequency at 268 kHz. This high-pass section requires that a 390-pF capacitor be used at each transmit input (TXINP and TXINN) for the appropriate Chebyshev response. Together the LPF and HPF form a bandpass filter with a passband ripple of about 0.6 dB. The THS7103 receive LPF is comprised of a fourth order Chebyshev filter with a 0.25-dB passband ripple and a breakpoint frequency of 238 kHz.

NOTE:

The definition of breakpoint frequency is the frequency at which the attenuation leaves the ripple band.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BUFEN	1	I	Buffer enable − enables buffers 1 and 2
1BUFOUT	2	O	Buffer 1 output
1BUFIN	3	I	Buffer 1 input
2BUFIN	6	I	Buffer 2 input
2BUFOUT	7	O	Buffer 2 output
GND	26	I	Ground
NC	25		No connect
RXCM	8	O	Receive channel common-mode voltage decoupling node
RXMO	9	O	Negative receiver preamp output
RXMI	10	I	Negative receiver preamp inverting input
RXMN	11	I	Negative receiver preamp noninverting input
RXOUTP	4	O	Receive channel positive output
RXOUTN	5	O	Receive channel negative output
RXPI	14	I	Positive receiver preamp inverting input
RXPN	13	I	Positive receiver preamp noninverting input
RXPO	15	O	Positive receiver preamp output
TXAF	22	O	Driver A output
TXBF	18	O	Driver B output
TXAS1	23	I	Driver A sense point 1
TXAS2	21	I	Driver A sense point 2
TXBS1	17	I	Driver B sense point 1
TXBS2	19	I	Driver B sense point 2
TXCM	30	O	Transmit channel common mode decoupling node
TXEN1	29	I	Transmit enable 1
TXEN2	28	I	Transmit enable 2
TXINN	32	I	Transmit channel negative input
TXINP	31	I	Transmit channel positive input
VAG	12	O	Virtual analog ground − is at VCCL/2
VCCL	27	I	V_{CC} to low level circuitry
VCCON	20	I	Output stage negative supply − tie to ground
VCCOPx	24, 16	I	Output stage positive V_{CC} supply

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	VCCL, VCCOP1, VCCOP2	7.5	15	16	V
Operating free-air temperature, T_A	I−suffix	−40		85	°C
	C−suffix	0		70	

driver characteristics, VCCL = VCCOPx = 15 V, VCCON = GND, R_S = 1.35 Ω, N = 1, R_L = 27 Ω†, C_i = 0.1 μF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{IN}−Tx	Input resistance (single-ended)		1.13	1.16	1.19	kΩ
V_A	Output voltage	f = 1 MHz, THD ≤ −31 dBc	23.8	24.4		V_{pp}
V_A/V_{IN}	Gain (see Note 3 and Figure 1)	f = 1 MHz	19.0	19.5	19.8	dB
		f ≅ 270 kHz (Peak frequency)	22.2	22.5	22.8	
V_B/V_{IN}		f = 1 MHz	18.2	18.7	19	dB
		f ≅ 270 kHz (Peak frequency)	21.4	21.7	22	
	Differential output noise	200 kHz		85		nV/√Hz
Z_o	Output impedance‡	f = 20 kHz to 1.1 MHz		†		Ω
	Filter corner frequency	HPF, C_i = 0.1 μF	178	190	202	kHz
		LPF	1.15	1.4	1.65	MHz
	Out of band rejection (relative to the input signal)	V_O at f = 40 kHz, C_i = 0.1 μF	−10	−14		dB
		V_O at f = 6 MHz	−17.5	−20.5		
	Channel-to-channel mismatch	f = 200 kHz to 800 kHz	−0.15	0	0.35	dB
		f = 900 kHz to 1.1 MHz	−0.15	0.2	0.5	
I_{CCL}	Supply current	Off, TXEN1 = 0, TXEN2 = 0	0.7	1	1.3	mA
		Low, TXEN1 = 1, TXEN2 = 0	13.1	14.6	16.1	
		Med., TXEN1 = 1, TXEN2 = 1	13.3	14.8	16.3	
		High, TXEN1 = 0, TXEN2 = 1	13.5	15	16.5	
I_{CCOP}	Supply current	Off, TXEN1 = 0, TXEN2 = 0	0	0.6	1.1	mA
		Low, TXEN1 = 1, TXEN2 = 0	1.7	2.7	3.7	
		Med., TXEN1 = 1, TXEN2 = 1	6	7.5	9	
		High, TXEN1 = 0, TXEN2 = 1	11	13	15	

† The test circuit of R_S = 1.35 Ω, N = 1, and R_L = 27 Ω is equivalent to a standard ADSL circuit with R_S = 1.35 Ω, N = 1.9, and R_L = 100 Ω.
‡ Output impedance is given by $Z_o = 10 \times R_S$.
NOTES: 3. Due to the gain of the transmit path, the maximum input voltage should not exceed 3 V_{pp} or clipping and distortion occurs.

receiver characteristics, VCCL = VCCOPx = 15 V, VCCON = GND, R_S = 1.35 Ω, N = 1, R_L = 3.9 kΩ, R_F = 5 kΩ, Gain = 26 dB, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	V_I = 1 V_{pp}, f = 200 kHz	19	20		V_{pp}
	Output noise	At f = 200 kHz		73		nV/√Hz
V_n	Noise voltage (preamp input noise)	f = 20 kHz		2.3		nV/√Hz
I_n	Noise current (preamp input noise)	f = 20 kHz		1.0		pA/√Hz
	Filter corner frequency	V_I = 0.5 V_{pp}	223.7	238	252.3	kHz
	Out of band rejection (relative to input point A) See Figure 1	V_O at f = 400 kHz		−6		dB
	In-band ripple	V_O at f = 55 kHz and 103.5 kHz		0.2	0.5	dB
	Channel-to-channel mismatch	f = 10 kHz to 145 kHz	−0.15	0	0.15	dB

transmit enable characteristics (TXEN1, TXEN2), VCCL = VCCOPx = 15 V, VCCON = GND, R_S = 1.35 Ω, N = 1, T_A = 25°C

BUFEN	TXEN1	TXEN2	FUNCTION	DESCRIPTION
X	0	0	Tx OFF	Device completely powered down
X	0	1	Tx ON − 100% bias	Full power
X	1	1	Tx ON − Medium bias	Medium power
X	1	0	Tx ON − Low bias	Low power
0	X	X	Buffers off	Conserves power when buffers are not required
1	X	X	Buffers enabled	Useful for extra RX filtering

NOTE: The default state shall be a logic one (1).

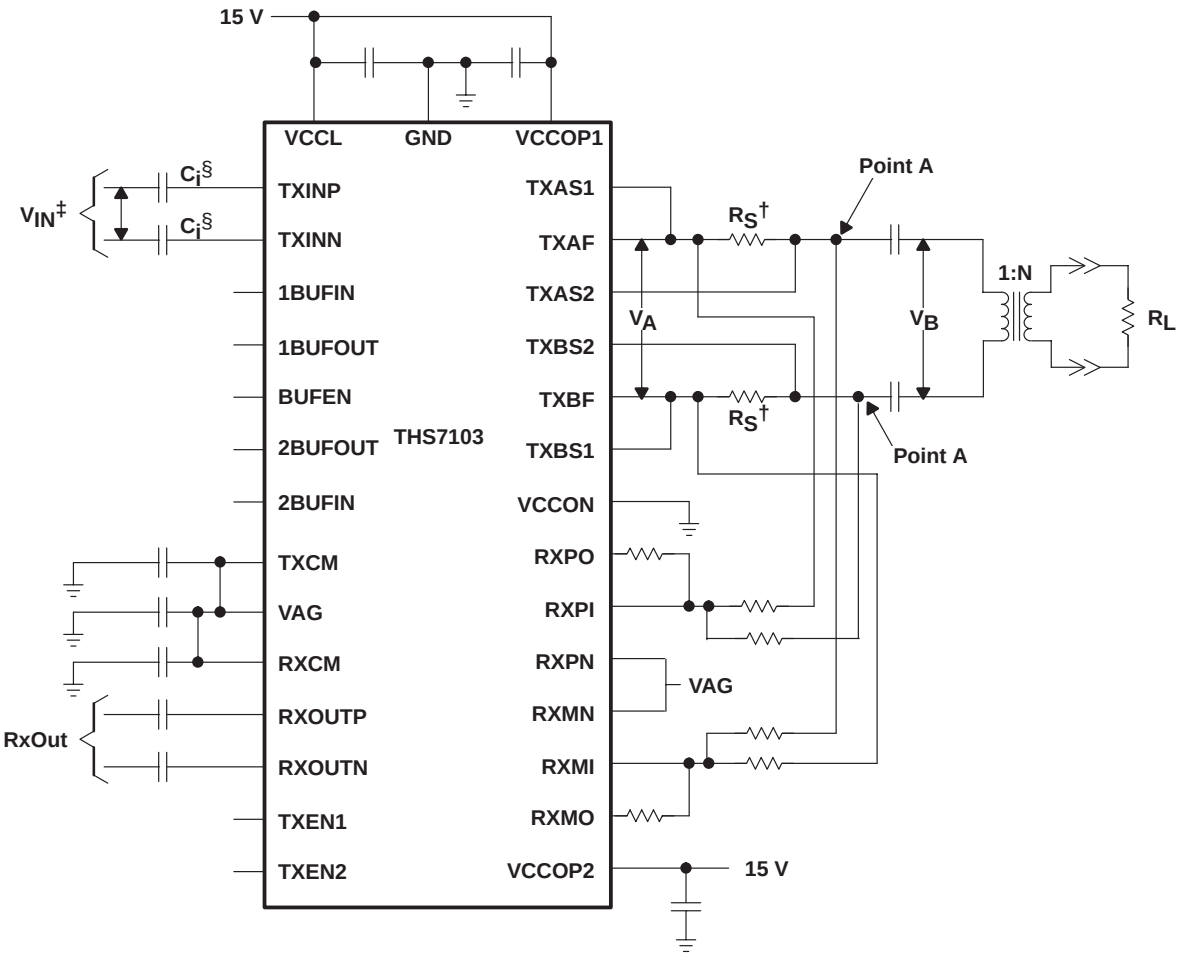
logic control characteristics, VCCL = VCCOPx = 15 V, VCCON = GND, R_S = 1.35 Ω, N = 1, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	TXEN1	V_{TXEN1} = 5 V	−5	0	5	µA
	TXEN2	V_{TXEN2} = 5 V	−5	0	5	
	BUFEN	V_{BUFEN} = 5 V	−5	0	5	
I_{IL}	TXEN1	V_{TXEN1} = 0 V	−70	−50	−30	µA
	TXEN2	V_{TXEN2} = 0 V	−70	−55	−30	
	BUFEN	V_{BUFEN} = 0 V	−70	−50	−30	
V_{IH}	All logic control pins			≥2.3		V
V_{IL}	All logic control pins			≤0.8		V

miscellaneous characteristics, VCCL = VCCOPx = 15 V, VCCON = GND, R_S = 1.35 Ω, N = 1, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, VAG		7.4	7.5	7.6	V
V_O	Output voltage, buffer	V_I = 7.5 V	7.0	7.5	8.0	V

APPLICATION INFORMATION

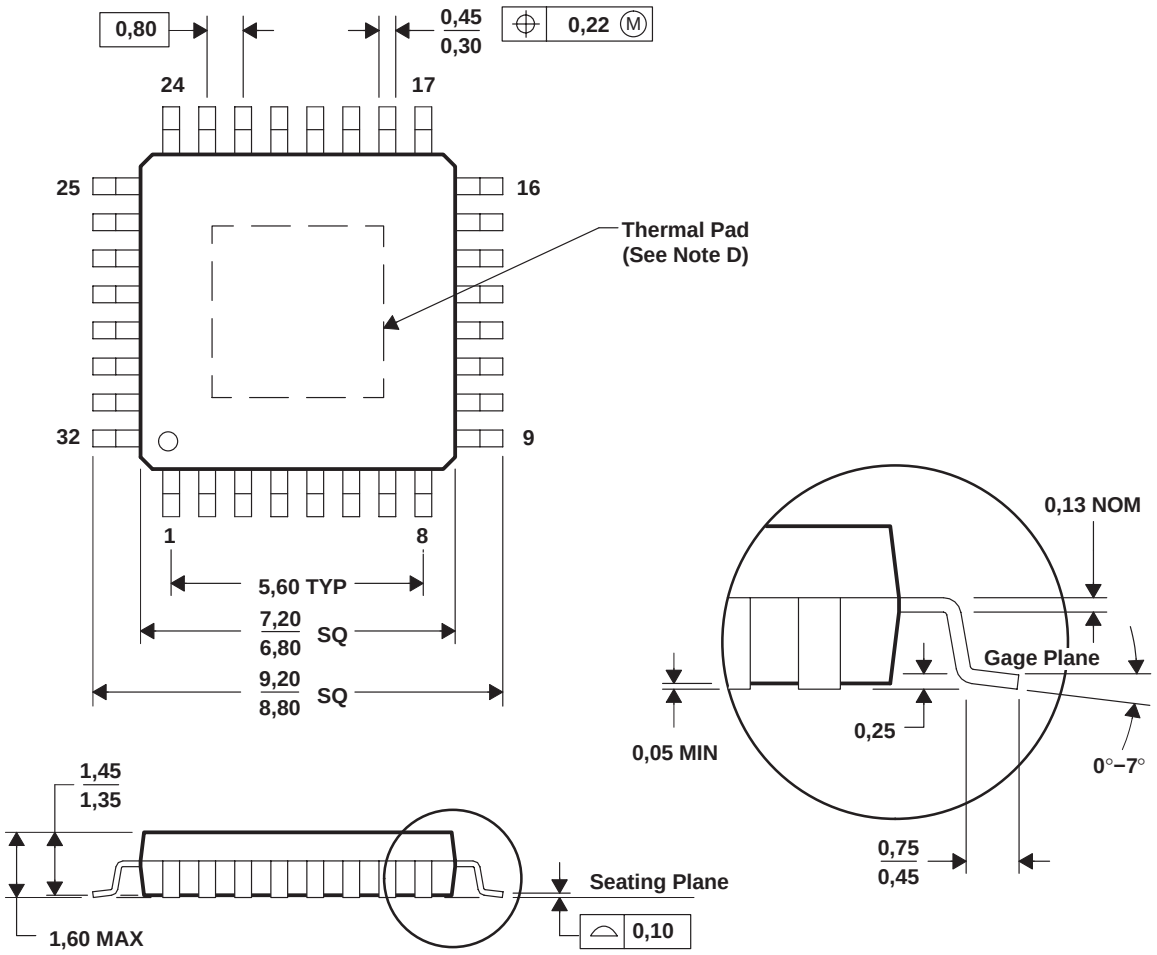


† Output impedance of transmit driver at point A = 10 × R_S
‡ Maximum input of V_{IN} = 3 V_{pp}.
§ In ADSL systems, it is recommended to use C_i = 390 pF for the THS7103. For testing purposes, use C_i = 0.1 μF.

Figure 1. Typical THS7103 Circuit Configuration

MECHANICAL DATA

VFP (S-PQFP-G32) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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