THVD8000 RS-485 Transceiver with OOK Modulation for Power Line Communication

1 Features

- 3-V – 5.5-V supply voltage
- Half-duplex communication
  - Up to 500 kbps data rate with f_0 / bps = 10
  - Higher data rates are possible with f_0 / bps < 10
- RS-485 electrical signaling with on-off keying (OOK) modulation
- Pin selectable carrier frequency: 125 kHz – 5 MHz
- Spread spectrum clocking for excellent EMI performance
- Polarity free
- TX timeout to avoid stuck bus conditions
- Operational common-mode range: –7 V to 12 V
- Bus I/O protection
  - ± 18-V DC fault protection
  - ± 16 kV HBM ESD
  - ± 8 kV IEC 61000-4-2 contact discharge
  - ± 15 kV IEC 61000-4-2 air gap discharge
  - ± 4 kV IEC 61000-4-4 fast transient burst
- Extended temperature range: -40°C to 125°C
- 8-Pin SOT-23 package for space constrained applications

2 Applications

- HVAC systems
- Building automation
- Factory automation & control
- Appliances
- Lighting
- Grid infrastructure
- Power delivery

3 Description

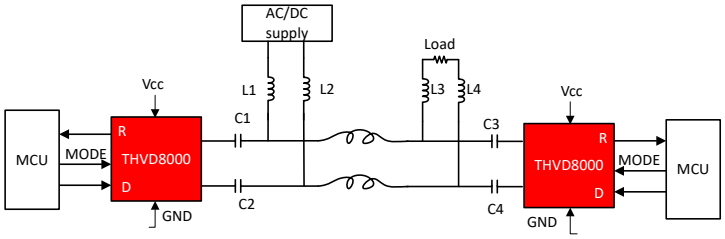
THVD8000 is an RS-485 transceiver with on-off keying (OOK) modulation and demodulation built in for power line communication. Modulating data onto existing power lines allows power delivery and data communication to share a common pair of wires, resulting in a significant reduction of the system cost.

A pin programmable interface simplifies the system design. The carrier frequency can be adjusted by changing an external resistor on the F_SET pin. A broad range of carrier frequencies gives the system designer the flexibility to choose the external inductors and capacitors. In addition, OOK modulation operates with immunity to data polarity for ease of system installations.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
THVD8000	SOT-23 (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2020) to Revision A (March 2021)	Page
• Changed the data sheet status From: *Advanced Information* To: *Production* data	1

5 Pin Configuration and Functions

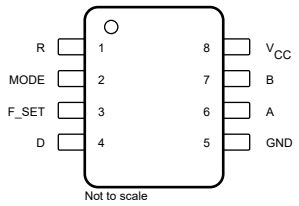


Figure 5-1. DRL Package, 8-Pin SOT-23, Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	Digital output	Receive data output
MODE	2	Digital input	Transmit/receive mode selection. Low = receive mode; High = transmit mode. 2-MΩ pull-down to GND
F_SET	3	Analog input	Carrier frequency selection. Use a resistor to GND to select a frequency.
D	4	Digital input	Driver data input, 2-MΩ pull-up to V_{CC}
GND	5	Ground	Device ground
A	6	Bus input/output	Bus I/O port A (complementary to B)
B	7	Bus input/output	Bus I/O port B (complementary to A)
V_{CC}	8	Power	3.3-V to 5-V device supply

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_L	Input voltage at any logic pin (D, MODE or F_SET)	–0.3	5.7	V
V_A, V_B	Voltage at A or B inputs (differential or with respect to GND)	–18	18	V
I_O	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.4* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A and B pins to GND	±16,000	V
			All pins	±4,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1,500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD contact discharge, A and B pins to GND	±8,000	V
		IEC 61000-4-2 ESD air gap discharge, A and B pins to GND	±15,000	
		IEC 61000-4-4 electrical fast transient, A and B pins to GND	±4,000	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{ID}	Input differential voltage (A and B pins)		–7		12	V
V_{CM}	Operational common mode voltage (A and B pins)		–7		12	V
V_{IH}	High-level input voltage (D and MODE pins)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D and MODE pins)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–4		4	
R_{F_SET}	Carrier frequency selection resistor		1.5		80	kΩ
ΔR_{F_SET}	Carrier frequency selection resistor tolerance		–2		2	%
$1/t_{UI}$	Data rate	Modulation mode(1)			f_0 / 10	bps
C_{F_SET}	Recommended load capacitance on F_SET pin				100	pF
T_A	Operating ambient temperature		–40		125	°C

(1) f_0 is the carrier frequency (in Hz) set by the external resistor between F_SET and GND pins.

6.5 Thermal Information

THERMAL METRIC[1]		THVD8000 DDF (SOT-23) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.5	°C/W
ψ_{JB}	Junction-to-top characterization parameter	29.5	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and ICPackage Thermal Metrics application report.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted). All typical values are measured at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V, Measured at 2nd pulse	See Figure 7-1	1.5	3.5		V
		R_L = 100 Ω, C_L = 50 pF, Measured at 2nd pulse	See Figure 7-1	2	4		
		R_L = 54 Ω, C_L = 50 pF, Measured at 2nd pulse	See Figure 7-1	1.5	3.5		
V_{OC}	Steady state common-mode output voltage	R_L = 60 Ω, C_L = 50 pF	See Figure 7-2	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage	R_L = 60 Ω, C_L = 50 pF	See Figure 7-2	-160		160	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	R_L = 60 Ω, C_L = 50 pF, V_{CC} = 3.3 V and V_{CC} = 5V	See Figure 7-2		425		mV
I_{OS}	Driver short-circuit output current	MODE = V_{CC}, –7 V ≤ [V_A or V_B] ≤ 12 V		–250		250	mA
f_0	Minimum carrier frequency[1]	R_{F_SET} = 77 kΩ	See Figure 7-3		125		kHz
	Maximum carrier frequency[1]	R_{F_SET} = 1.5 kΩ			5		MHz
DCD_{f0}	Carrier frequency duty cycle distortion	Measured over the full range of f_0		–2		2	%
Δf_0	Carrier frequency tolerance	Measured with a ±2% tolerant R_{F_SET}		–25		25	%
Δf_{SSC}	Variation of the carrier frequency for spread spectrum clocking	Measured across the full carrier frequency range			±5		%
f_{SSC}	Spread spectrum clock rate				30		kHz

Over operating free-air temperature range (unless otherwise noted). All typical values are measured at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Receiver							
I_I	Bus input current in receive mode	MODE = GND, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	125	µA
			V_I = –7 V	–97	–70		
V_{MAG_ZERO}	OOK signal differential swing (magnitude) to detect a zero at the R output	MODE = GND, over full common mode range	125 kHz			225	mV
			1 MHz			150	
			5 MHz			115	
V_{MAG_ONE}	OOK signal differential swing (magnitude) to detect a one at the R output		125 kHz	20			mV
			1 MHz	10			
			5 MHz	10			
V_{MAG_HYS}	Receiver differential input voltage threshold hysteresis		125 kHz	40			mV
			1 MHz	20			
			5 MHz	20			
Logic / Control Pins							
I_{IN}	Input current (D, MODE)	V_O = 0 V or V_{CC}		–5		5	µA
I_{IN}	Input current (F_SET)	V_O = V_{CC}				55	µA
V_O	Output voltage (F_SET)	I_O = 0 mA			1.4		V
		1.5 kΩ ≤ R_{PD} ≤ 78 kΩ			785		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –4 mA		V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 4 mA			0.2	0.4	V
I_{OZ}	Receiver high-impedance output current	V_O = 0 V or V_{CC}, MODE = 0		–1		1	µA
Device							
I_{CC}	Supply current (quiescent)	Transmit mode	D = V_{CC}, MODE = V_{CC}, resistor between F_SET and GND, no load		3.1	5	mA
		Receive mode	D = V_{CC}, MODE = GND, resistor between F_SET and GND, no load		4	6	
T_{SD}	Thermal shutdown temperature			160	170	185	℃
T_{HYS}	Thermal shutdown hysteresis				11	15	℃

(1) See OOK modulation section for the complete carrier frequency range

6.7 Power Dissipation Characteristics

Over operating free-air temperature range (unless otherwise noted). All typical values are measured at 25°C and supply voltage of V_{CC} = 5 V.

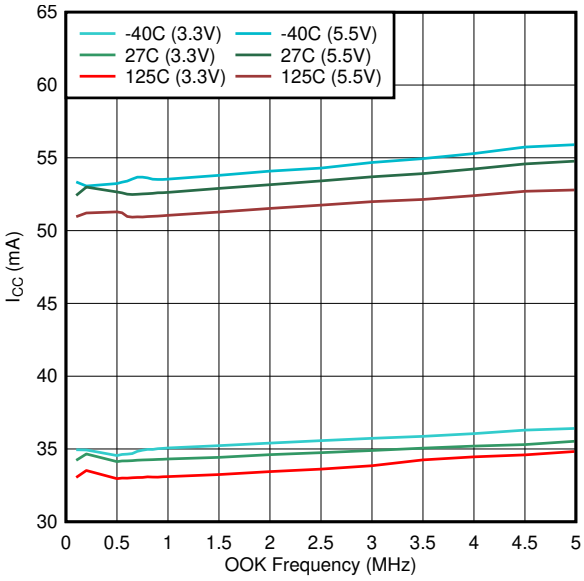
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PD_{OOK}	Chip power dissipation	MODE = V_{CC}, R_L = 60 Ω, no C_L, see Figure 2	f_0 = 125 kHz, 12.5 kHz (25 kbps) clock pattern as data		60	80	mW
			f_0 = 5 MHz, 500 kHz (1Mbps) clock pattern as data		90	125	mW

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). All typical values are measured at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Driver differential output rise and fall times		R_L = 60 Ω, C_L = 50 pF, See Figure 7-4		10	30	ns
t_{PHL}, t_{PLH}	Driver propagation delay				1.2	2.5	Clocks
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				0.3	2.5	Clocks
Receiver							
t_r, t_f	Receiver output rise and fall times		C_L = 15 pF, See Figure 7-5		1.5	16	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				4	6.5	Clocks
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				1.1	3	
Device							
$t_{TX\text{-}RX\_OOK}$	Transmit to receive mode change delay, OOK mode	For all R_{FSET}	Worst case of $t_{TX\text{-}RX\_OOK\_ZERO}$ and $t_{TX\text{-}RX\_OOK\_ONE}$. See Figure 7-6 and Figure 7-7			14	clocks
$t_{RX\text{-}TX\_OOK}$	Receive to transmit mode change delay, OOK mode	For all R_{FSET}	See Figure 7-8			12	clocks
$t_{TX\_TIMEOUT}$	Transmit timeout delay			60	110		s

6.9 Typical Characteristics



R_L = 60Ω Data rate = f_0/10 TX Enabled

Figure 6-1. ICC vs OOK Frequency

7 Parameter Measurement Information

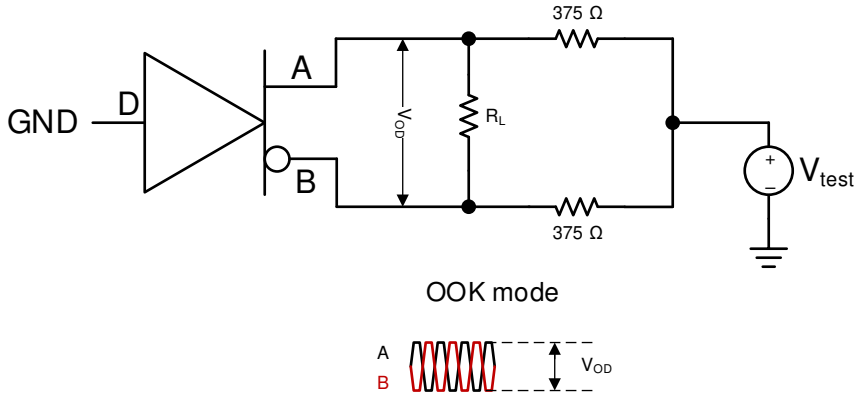


Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

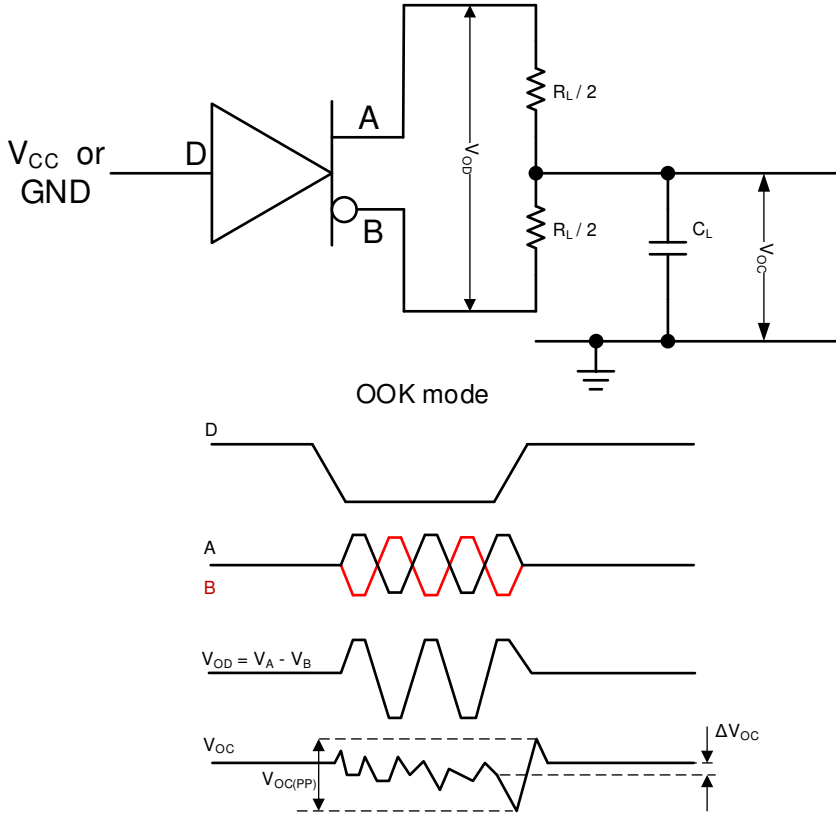


Figure 7-2. Measurement of Driver Differential and Common-Mode Outputs

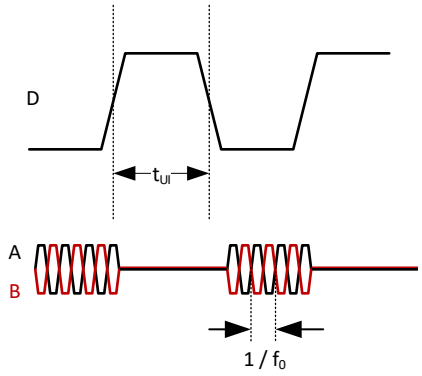


Figure 7-3. Measurement of Carrier Frequency

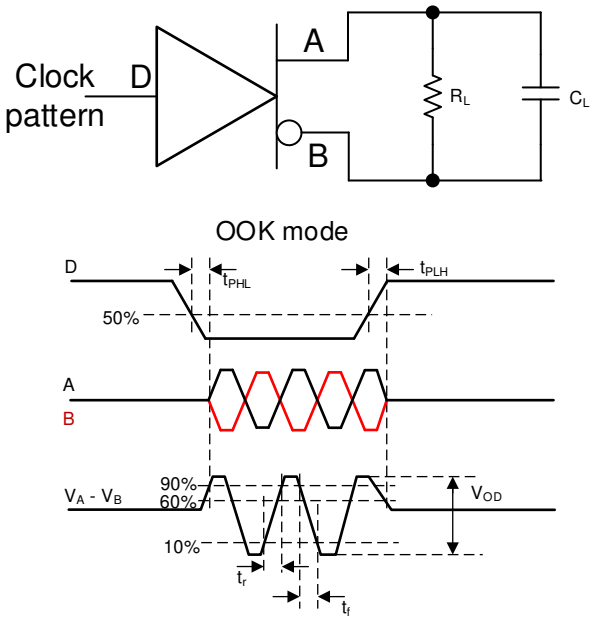


Figure 7-4. Measurement of Driver Switching Characteristics

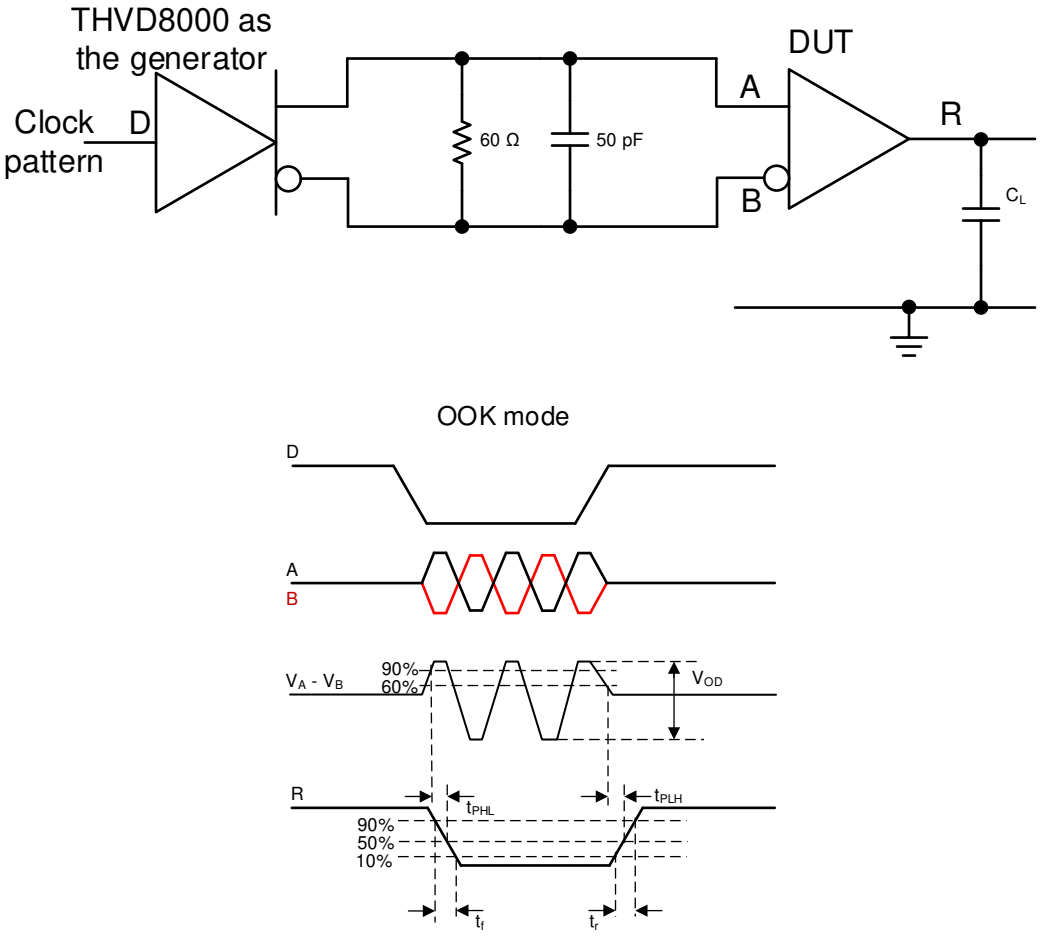


Figure 7-5. Measurement of Receiver Characteristics

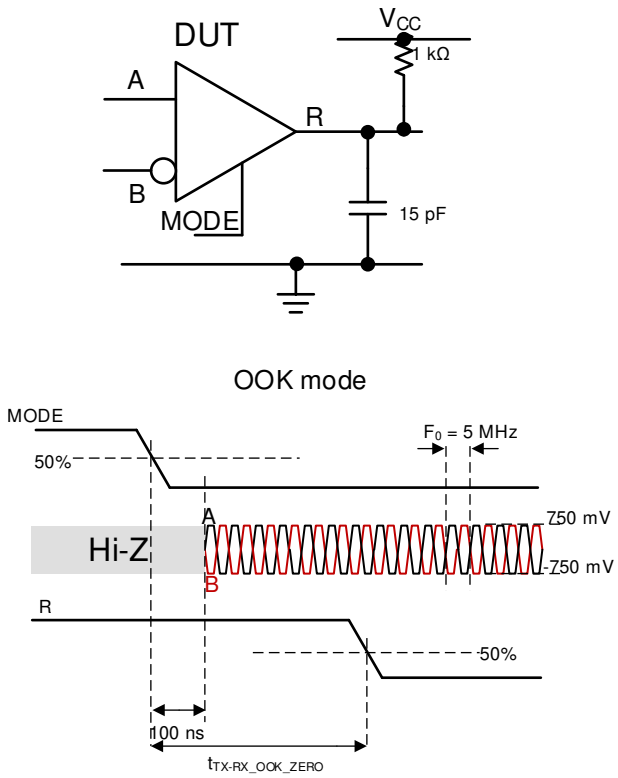


Figure 7-6. Transmit to Receive Mode Change with Low Output

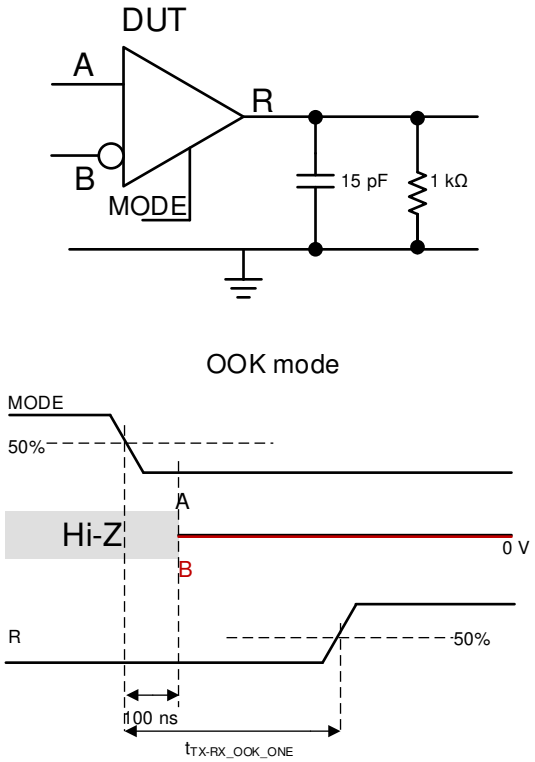


Figure 7-7. Transmit to Receive Mode Change with High Output

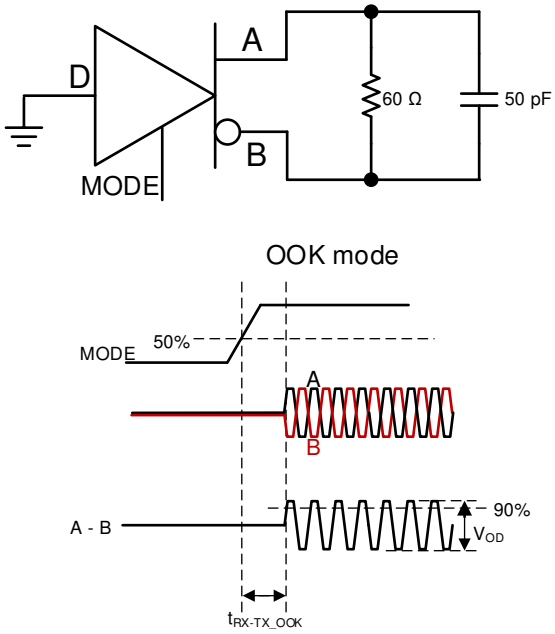


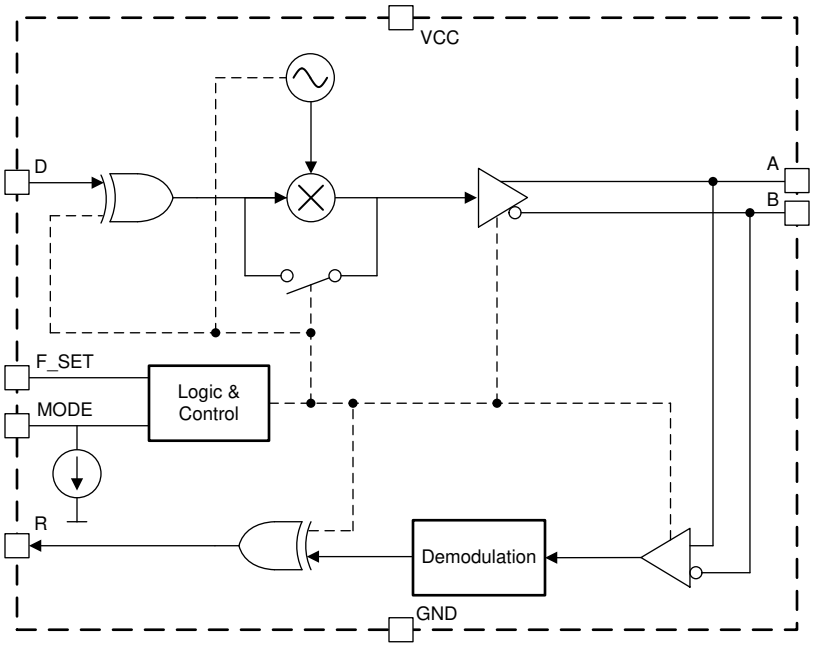
Figure 7-8. Receive to Transmit Mode Change

8 Detailed Description

8.1 Overview

THVD8000 enables power line communication using RS-485 physical layer signaling. An integrated OOK modulator enables RS-485 data to be directly coupled onto existing power cables via series capacitors without any updates to the MCU or the controller. The THVD8000 receiver extracts the data from the power cables through series capacitors by using a precise bandpass filter and a demodulator.

8.2 Functional Block Diagrams



8.3 Feature Description

8.3.1 OOK Modulation with F_SET pin

Data at the D input is modulated with the carrier frequency (f_0) via the F_SET pin. Figure 8-1 illustrates the modulation scheme. A high level at the D input is driven to the mid-level with zero differential voltage (V_{OD}). A low level at the D input is modulated at the carrier frequency. It is recommended to use a carrier frequency that is 10x higher than the data rate. Higher data rates are possible at the expense of increased pulse width distortion with the use of lower ratios.

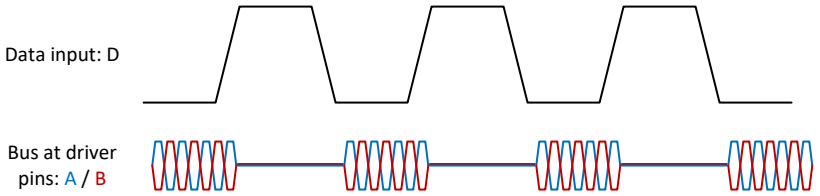


Figure 8-1. OOK Modulation Scheme

f_0 is programmable by changing the external resistor (R_{F_SET}) value connected to ground. Table 8-1 shows the carrier frequency for the each recommended resistor value.

Table 8-1. OOK f_0 versus R_{F_SET}

R_{F_SET} (kΩ)	OOK f_0 (kHz)
77	125
50	187.5
19	500

Table 8-1. OOK f_0 versus R_{F_SET} (continued)

R_{F_SET} (kΩ)	OOK f_0 (kHz)
12.5	750
9.3	1000
4.4	2000
1.5	5000

The oscillator used to generate the carrier frequency features spread spectrum clocking to reduce emissions.

8.3.2 OOK Demodulation

The OOK signal received at the A and B inputs go through a bandpass filter and a peak detector to regenerate the original data stream. Figure 8-2 shows the OOK input and the R output waveforms. The bandpass filter characteristics will adapt to optimal settings automatically based on the carrier frequency, set via R_{F_SET}.

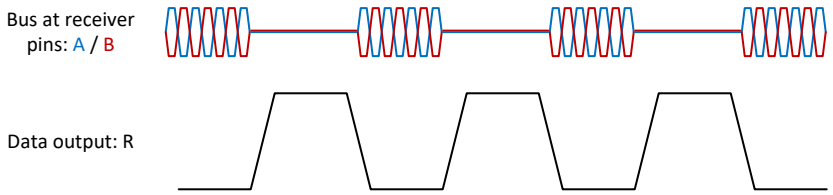


Figure 8-2. OOK Demodulation

8.3.3 Transmitter Timeout

The driver path incorporates a timeout feature to prevent a faulty node from occupying the bus indefinitely in a multi-drop application.

The driver stops transmitting and the outputs will go high impedance if the D input doesn't detect an edge (either rising or falling) for longer than $t_{TX\_TIMEOUT}$. One of the following events brings the device back to normal operation.

- Any edge at D input
- Toggle MODE pin

The transmit path resumes operation within t_{MODE}.

8.3.4 Polarity Free Operation

THVD8000 is immune to A and B polarity at the receiver input in OOK mode. The receiver data comparator only checks for the receive input signal magnitude, ignoring the polarity, to determine its logic level. Note that reversing the polarity does result in degraded pulse width distortion.

8.3.5 Glitch Free Mode Change

The device incorporates a delay of up to t_{MODE} when changing the state of the MODE pin. This feature ensures that there are no glitches at the A, B and R outputs when transitioning between transmit and receive modes.

8.3.6 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±8 kV contact and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. This integrated protection eliminates the need of external components reducing the system BOM.

8.4 Device Functional Modes

Table 8-2. THVD8000 Functional Modes

F_SET Configuration	Device Functional Mode
R_{F_SET} between F_SET and GND	OOK mode, f_0 set by the R_{F_SET} value
F_SET at high impedance	Invalid, not recommended for normal operation
F_SET at V_{CC}	
F_SET short to GND	

8.4.1 OOK Mode

Data at the D input is modulated with the carrier frequency set by the R_{F_SET} value when the device is transmitting (MODE = V_{CC}). See Section 8.3.1 section for more details. In receiving (MODE = GND), the device expects an OOK modulated signal at the A and B inputs. The data is demodulated and sent out via R pin. See Section 8.3.2 section for more details.

Table 8-3. Driver function table for OOK mode

INPUTS			OUTPUTS		FUNCTION
F_SET	MODE	D	A	B	
R_{F_SET} (See Table 8-1)	H	H or Z	Bias to V_{CM}	Bias to V_{CM}	Driver is actively biased to V_{CM} on the bus
	H	L	Oscillating	Oscillating	Bus actively driven at carrier frequency
	L or Z	X	Z	Z	Driver disabled, device in receive mode

Table 8-4. Receiver function table for OOK mode

INPUTS			OUTPUT	FUNCTION
F_SET	MODE	Input	R	
R_{F_SET} (See Table 8-1)	L or Z	Oscillating at F_SET and $V_{ID} > V_{MAG\_ZERO}$	L	Receive valid bus low
	L or Z	Oscillating at F_SET and $V_{MAG\_ONE} < V_{ID} < V_{MAG\_ZERO}$	?	Receive invalid bus, output indeterminate
	L or Z	Oscillating at F_SET and $V_{ID} < V_{MAG\_ONE}$	H	Receive valid bus high
	L or Z	Z / not oscillating	H	Receive valid bus high
	L or Z	OPEN, SHORT, IDLE (V_{ID} = 0 V)	H	Failsafe high output
	H	X	Z	Receiver disabled, device in transmit mode

8.4.2 Thermal shutdown (TSD)

The THVD8000 has a protection feature called thermal shutdown. When the junction temperature reaches T_{SD}, the device enters thermal shutdown protection mode. This mode disables the driver and receiver outputs, which will halt all communication through the device. Normal operation resume once the junction temperature drops out of thermal shutdown, which is typically T_{SD} - T_{HYS}.

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application information

The THVD8000 is able to transmit data over an AC coupled power line pair using On-Off Keying (OOK).

9.2 Typical application (OOK mode)

In order to combine data and power over a single pair of wires, capacitors and inductors are used in a bias-tee configuration. High-frequency differential data is AC-coupled onto the bus lines via series capacitances while power is DC-coupled via series inductances. The values of these components will depend on the carrier frequency, number of nodes on the bus, and the power delivery requirements (i.e., voltage and total current sourced or consumed by a given node).

The transmitted differential communication signal is AC-coupled onto the power bus as shown below. This configuration provides the advantage that the power transmitted on the bus has little impact on the differential data, allowing for a wide range of voltage and current scenarios. Typical applications are realized with the THVD8000 transmitting over a power bus of 24VDC or 24VAC with currents from 100mA to 1A, but due to the AC-coupling the THVD8000 does not directly see these voltages. For more information, please refer for the THVD8000 design guide.

In Figure 9-1, there is an optional rectifier network pictured on the bus lines. This network of diodes can ensure that the node is receives power correctly from the bus wires, even if the lines get swapped.

A termination resistance, R_T, is not required for device functionality but can be useful in improving signal integrity in some applications by reducing reflections that can occur at cable ends.

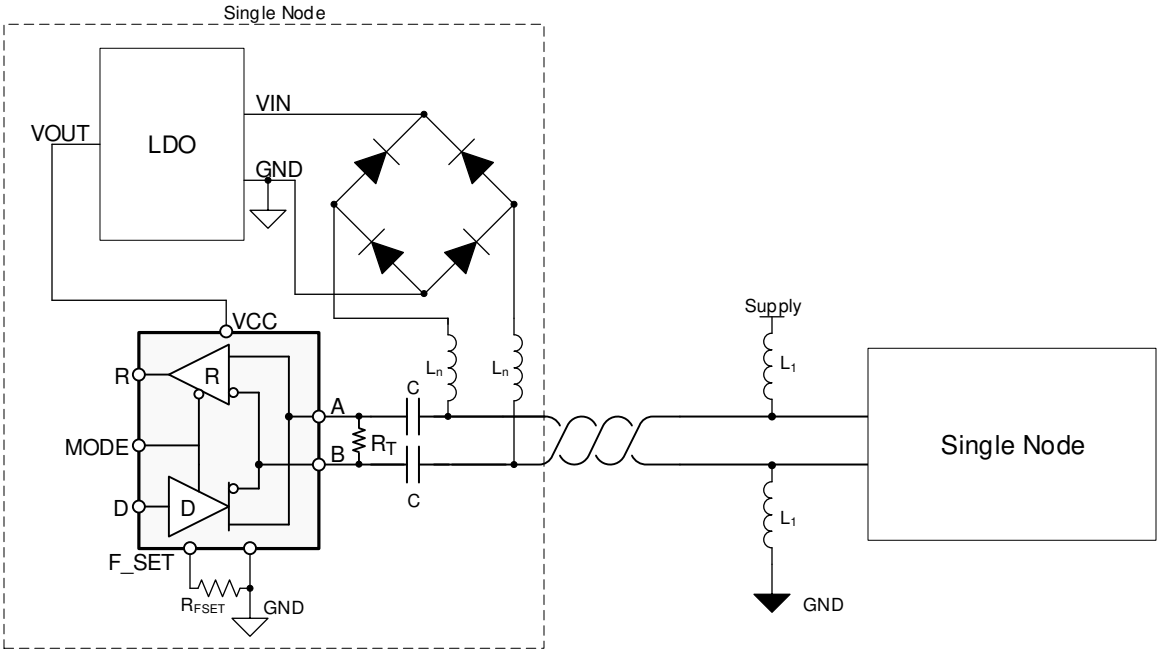


Figure 9-1. Typical power line network with 2 nodes

9.2.1 Design requirements

The main requirements are the values of the bus capacitors and the power inductors. Both of these values are dependant upon the carrier frequency selected.

9.2.1.1 Carrier frequency

This device uses on-off-keying to transmit binary data on the bus. Please read Section 8.3.1 for detailed information. The modulation and demodulation of the data can result in pulse width distortion due to asymmetries in low-to-high and high-to-low transition times. These asymmetries are due to factors like synchronization of the data to the internal carrier oscillator in the transmit path and the response time of the band-pass filter in the receive path. The impact of these factors can be minimized by choosing a carrier frequency much higher than the data rate required. A frequency ratio of at least 10:1 is recommended.

9.2.2 Detailed design procedure

9.2.2.1 Inductor value selection

It is important to note that the inductor selected must also take power consumption into consideration. The inductor should be sized to handle the maximum anticipated current in addition to the inductance value.

The parallel aggregate impedance should be selected so that the total equivalent impedance at the carrier frequency is Z ≥ 375 Ω. This assumes RS-485 loading with 60 Ω termination. If no termination is used in the application, then the total equivalent impedance at the carrier frequency could be reduced to Z ≥ 60 Ω. These examples assume that termination is used. Equation 1 shows the parallel aggregate impedance equation for inductors L_1 to L_n. Since the inductance value for each node should be the same, it's simple to determine that each node's impedance should be n times the total equivalent impedance. For example, if there are 4 nodes connected to the bus and the equivalent impedance is 375 Ω, then each node impedance should be 1,500 Ω.

$$Z = Z_1 \,||Z_2\,||\,..||\,Z_n \tag{1}$$

To determine the suggested inductance value, Equation 2 can be rearranged to determine L_n, as shown in Equation 3.

$$Z_n = 2\pi f_0 L_n \tag{2}$$

$$L_n = \frac{Z_n}{2\pi f_0} \tag{3}$$

f_0 is the carrier frequency (OOK frequency) used. If the previous 1.5 kΩ impedance per node is assumed with a carrier frequency of 1 MHz, the resulting inductance limit is ~240 µH per node. Be aware that this is the minimum suggested value per node. Refer to Figure 9-2 as a quick reference on the minimum inductance value to achieve 375 Ω of total aggregate impedance. This value can be multiplied by the number of nodes on the bus to get the minimum inductance per node. Referring to the previous example, if there are 4 nodes and a carrier frequency of 1 MHz, then the minimum aggregate inductance is about 60 µH, which is 240 µH when multiplied by 4.

9.2.2.2 Capacitor value selection

Capacitor selection is easier than inductor selection, primarily because capacitance impedance is important to allow higher frequency signals through. However, the capacitor ratings for voltage must be carefully selected to meet the application requirements. Special considerations for hot plug nodes should be made to ensure that voltage transients during hot plugging do not exceed the absolute maximum values. See Section 6.1.

The number of nodes on the bus does not play into the capacitance calculation. The impedance of a capacitor is shown in Equation 4.

$$Z = \frac{1}{2\pi f_0 C} \tag{4}$$

Maintaining Z ≤ 5 Ω keeps the impedance low enough at the carrier frequency to allow data to pass through. If the equation is rearranged to calculate C, the result is shown in Equation 5.

$$C = \frac{1}{2\pi f_0 Z} \tag{5}$$

If the previous example of a 1 MHz carrier frequency is used, then a minimum capacitance value of about 32 nF. For a quick reference, refer to Figure 9-3.

9.2.3 Application Curves

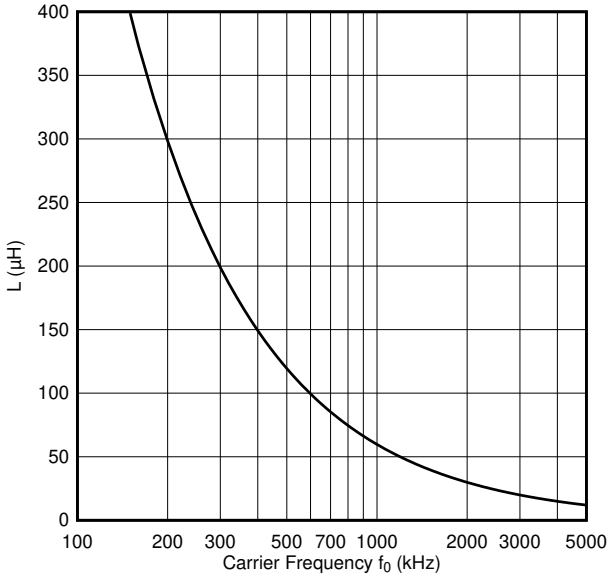


Figure 9-2. Inductor selection (select values above the line)

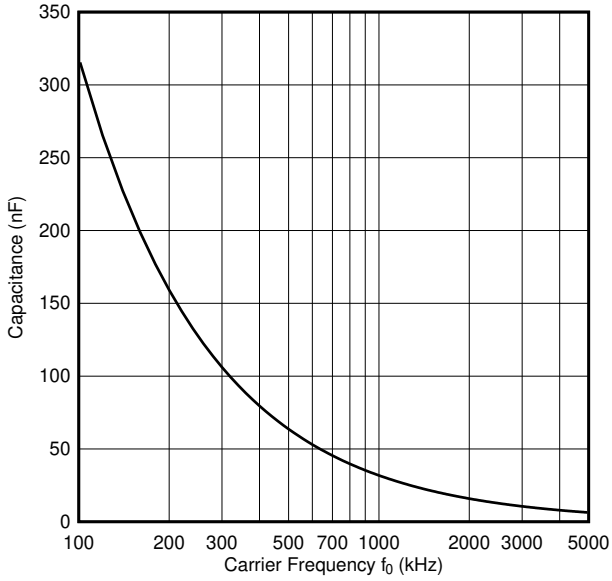


Figure 9-3. Capacitor selection (select values above the line)

10 Power supply recommendations

To ensure reliable operation at all data rates and supply voltages, the supply should be decoupled with a 100 nF to 220 nF ceramic capacitor and a 1 µF capacitor (for ESD sensitive designs) located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Place F_SET components near the pin to keep capacitance load below recommended value
4. Use a pull up or down resistor on mode to set a default state
5. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
6. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
7. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in theses lines during transient events.
8. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
9. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

11.2 Layout Example

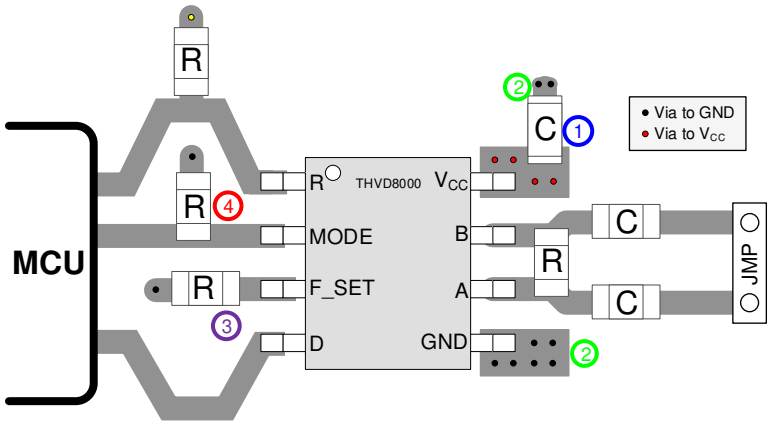


Figure 11-1. Layout Example (OOK)

12 Device and Documentation Support

12.1 Device Support

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD8000DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	8000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

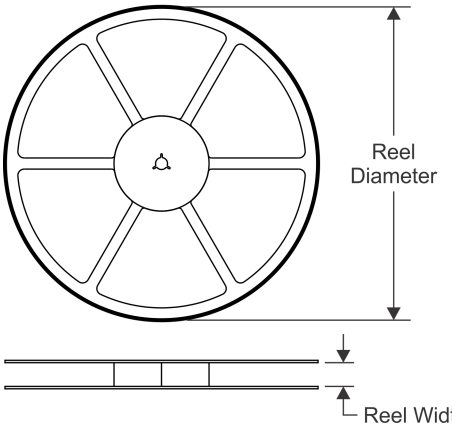
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

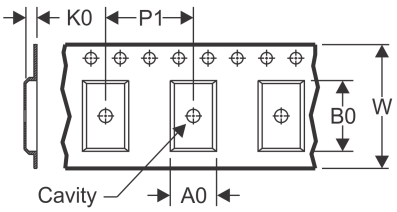
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

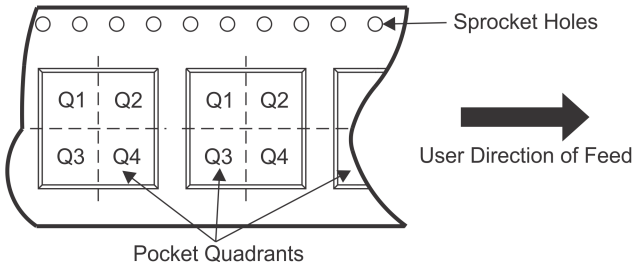


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

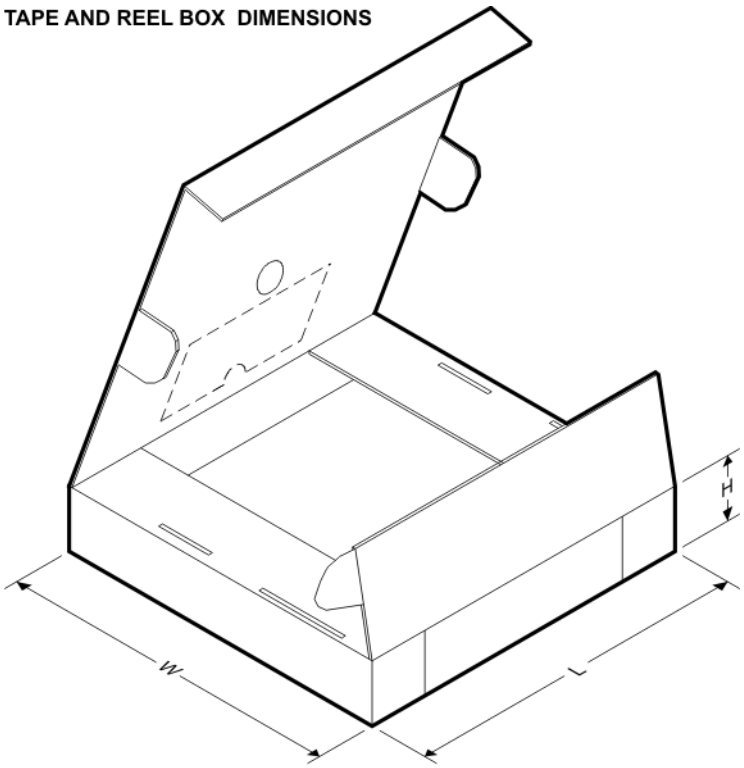
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD8000DDFR	SOT-23-THIN	DDF	8	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

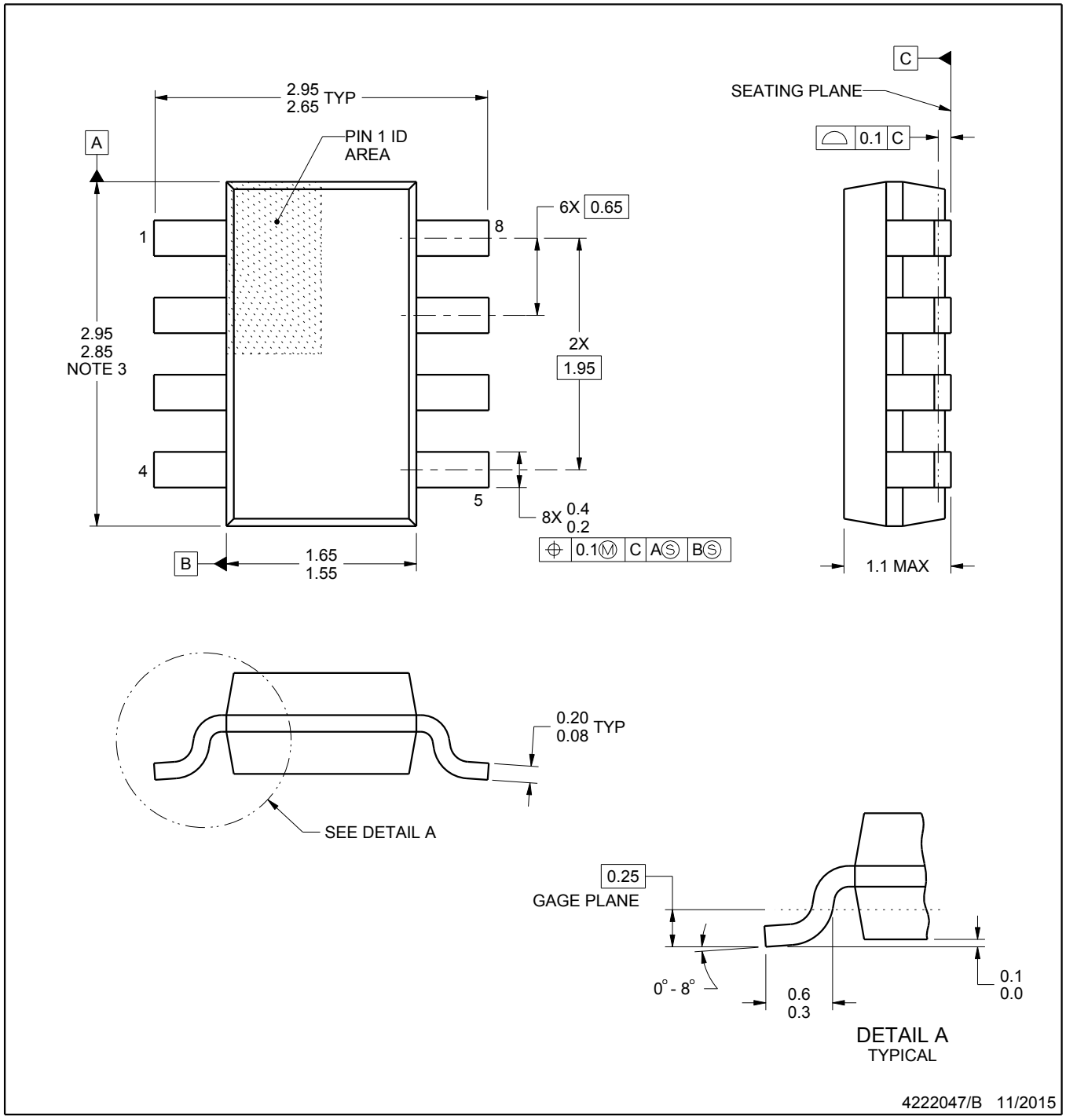
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD8000DDFR	SOT-23-THIN	DDF	8	3000	184.0	184.0	19.0

PACKAGE OUTLINE

DDF0008A

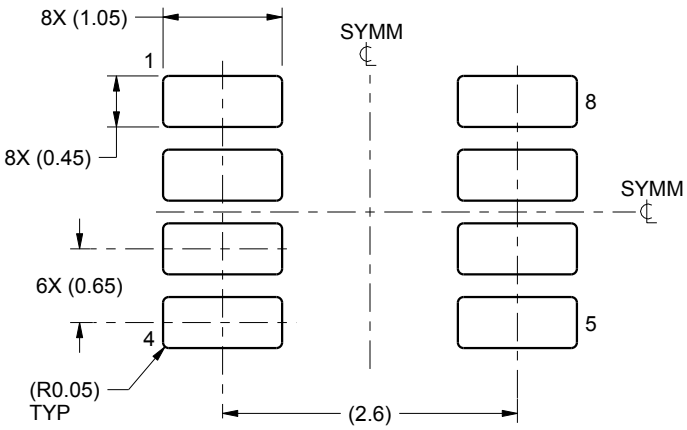
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

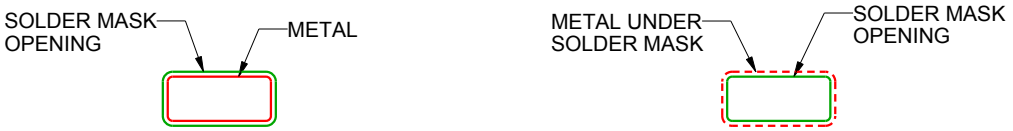


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

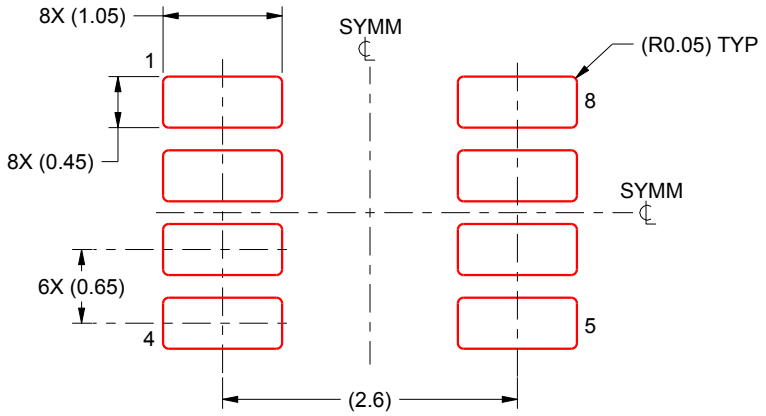
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265