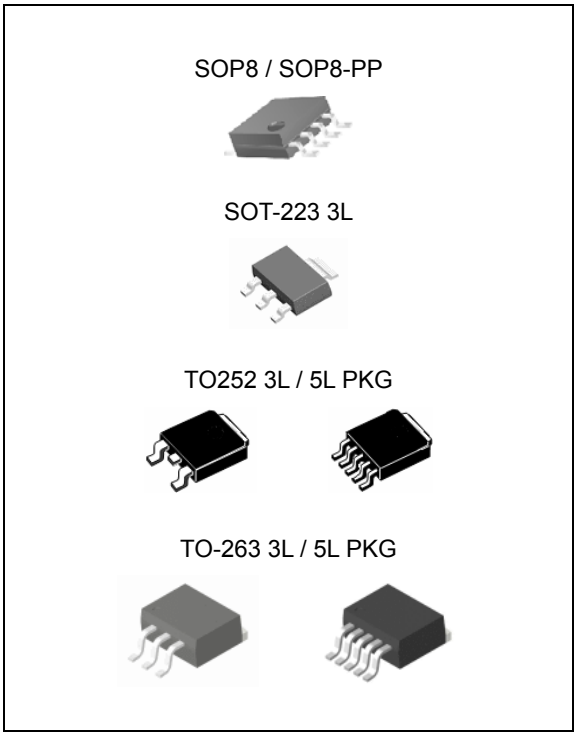
2A Ultra Low Dropout Linear Regulator TJ4220

FEATURES

- Ultra Low Dropout Voltage
- Compatible with low ESR MLCC as Input/Output Capacitor
- Good Line and Load Regulation
- Guaranteed Output Current of 2A
- Available in SOP8, SOP8-PP, SOT-223 and TO-252 and TO-263 Packages
- Fixed Output Voltages : 1.0V, 1.2V, 1.8V, 2.5V, and 3.3V
- SENSE Option Improves Load Regulation
- Over-Temperature/Over-Current Protection
- -40 ºC to 125 ºC Junction Temperature Range



APPLICATION

- LCD TVs and SETTOP Boxes
- Battery Powered Equipments
- Motherboards and Graphic Cards
- Microprocessor Power Supplies
- Peripheral Cards
- High Efficiency Linear Regulators
- Battery Chargers

DESCRIPTION

The TJ4220 series of high performance ultra-low dropout linear regulators operates from 2.5V to 6V input supply and provides ultra-low dropout voltage, high output current with low ground current. Wide range of preset output voltage options are available. These ultra-low dropout linear regulators respond fast to step changes in load which makes them suitable for low voltage micro-processor applications. The TJ4220 is developed on a CMOS process technology which allows low quiescent current operation independent of output load current. This CMOS process also allows the TJ4220 to operate under extremely low dropout conditions.

ORDERING INFORMATION

Device	Package
TJ4220GD-ADJ	SOP8
TJ4220GD-X.X	
TJ4220GDP-ADJ	SOP8-PP
TJ4220GDP-X.X	
TJ4220xS-ADJ	SOT-223 3L/5L
TJ4220xS-X.X	
TJ4220GRS-ADJ	TO-252 3L/5L
TJ4220GRS-X.X	
TJ4220GR-ADJ	TO-263 3L/5L
TJ4220GR-X.X	

X.X = Output Voltage = 1.0, 1.2, 1.8, 2.5, and 3.3

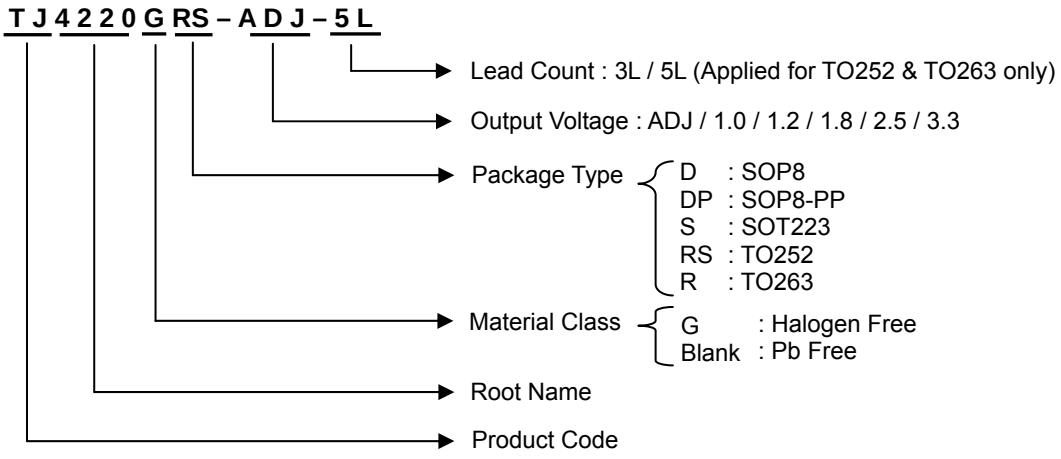
Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Input Supply Voltage (Survival)	V_{IN}	-	6.5	V
Enable Input Voltage (Survival)	V_{EN}	-	6.5	V
Maximum Output Current	I_{MAX}	-	2	A
Lead Temperature (Soldering, 5 sec)	T_{SOL}		260	ºC
Storage Temperature Range	T_{STG}	-65	150	ºC
Operating Junction Temperature Range	T_{JOPR}	-40	125	ºC
Package Thermal Resistance *	$\Theta_{JA\text{-}SOP8\text{-}PP}$	68		ºC/W

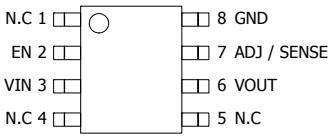
* Calculated from package in still air, mounted to 2.6mm X 3.5mm(minimum foot print) 2 layer PCB without thermal vias per JESD51 standards.

Ordering Information

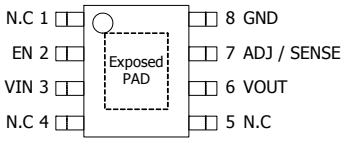
V_{OUT}	Package	Order No.	Description	Package Marking	Status
ADJ	SOP8	TJ4220GD-ADJ	2A, Adjustable, Enable	TJ4220G-ADJ	Contact Us
	SOP8-PP	TJ4220GDP-ADJ	2A, Adjustable, Enable	TJ4220G-ADJ	Active
	TO-252 5L	TJ4220GRS-ADJ-5L	2A, Adjustable, Enable	TJ4220G-ADJ	Contact Us
	TO-263 5L	TJ4220GR-ADJ-5L	2A, Adjustable, Enable	TJ4220G-ADJ	Contact Us
1.0V	SOP8	TJ4220GD-1.0	2A, Enable, SENSE	TJ4220G-1.0	Contact Us
	SOP8-PP	TJ4220GDP-1.0	2A, Enable, SENSE	TJ4220G-1.0	Contact Us
	SOT-223 3L	TJ4220S-1.0	2A	4220-1.0	Contact Us
	TO-252 3L	TJ4220GRS-1.0-3L	2A	TJ4220G-1.0	Contact Us
	TO-252 5L	TJ4220GRS-1.0-5L	2A, Enable, SENSE	TJ4220G-1.0	Contact Us
	TO-263 3L	TJ4220GR-1.0-3L	2A	TJ4220G-1.0	Contact Us
	TO-263 5L	TJ4220GR-1.0-5L	2A ,Enable, SENSE	TJ4220G-1.0	Contact Us
1.2V	SOP8	TJ4220GD-1.2	2A, Enable, SENSE	TJ4220G-1.2	Contact Us
	SOP8-PP	TJ4220GDP-1.2	2A, Enable, SENSE	TJ4220G-1.2	Contact Us
	SOT-223 3L	TJ4220S-1.2	2A	4220-1.2	Contact Us
	TO-252 3L	TJ4220GRS-1.2-3L	2A	TJ4220G-1.2	Contact Us
	TO-252 5L	TJ4220GRS-1.2-5L	2A, Enable, SENSE	TJ4220G-1.2	Contact Us
	TO-263 3L	TJ4220GR-1.2-3L	2A	TJ4220G-1.2	Contact Us
	TO-263 5L	TJ4220GR-1.2-5L	2A ,Enable, SENSE	TJ4220G-1.2	Contact Us
1.8V	SOP8	TJ4220GD-1.8	2A, Enable, SENSE	TJ4220G-1.8	Contact Us
	SOP8-PP	TJ4220GDP-1.8	2A, Enable, SENSE	TJ4220G-1.8	Contact Us
	SOT-223 3L	TJ4220S-1.8	2A	4220-1.8	Contact Us
	TO-252 3L	TJ4220GRS-1.8-3L	2A	TJ4220G-1.8	Contact Us
	TO-252 5L	TJ4220GRS-1.8-5L	2A, Enable, SENSE	TJ4220G-1.8	Contact Us
	TO-263 3L	TJ4220GR-1.8-3L	2A	TJ4220G-1.8	Contact Us
	TO-263 5L	TJ4220GR-1.8-5L	2A ,Enable, SENSE	TJ4220G-1.8	Contact Us
2.5V	SOP8	TJ4220GD-2.5	2A, Enable, SENSE	TJ4220G-2.5	Contact Us
	SOP8-PP	TJ4220GDP-2.5	2A, Enable, SENSE	TJ4220G-2.5	Contact Us
	SOT-223 3L	TJ4220S-2.5	2A	4220-2.5	Contact Us
	TO-252 3L	TJ4220GRS-2.5-3L	2A	TJ4220G-2.5	Contact Us
	TO-252 5L	TJ4220GRS-2.5-5L	2A, Enable, SENSE	TJ4220G-2.5	Contact Us
	TO-263 3L	TJ4220GR-2.5-3L	2A	TJ4220G-2.5	Contact Us
	TO-263 5L	TJ4220GR-2.5-5L	2A ,Enable, SENSE	TJ4220G-2.5	Contact Us
3.3V	SOP8	TJ4220GD-3.3	2A, Enable, SENSE	TJ4220G-3.3	Contact Us
	SOP8-PP	TJ4220GDP-3.3	2A, Enable, SENSE	TJ4220G-3.3	Contact Us
	SOT-223 3L	TJ4220S-3.3	2A	4220-3.3	Contact Us
	TO-252 3L	TJ4220GRS-3.3-3L	2A	TJ4220G-3.3	Contact Us
	TO-252 5L	TJ4220GRS-3.3-5L	2A, Enable, SENSE	TJ4220G-3.3	Contact Us
	TO-263 3L	TJ4220GR-3.3-3L	2A	TJ4220G-3.3	Contact Us
	TO-263 5L	TJ4220GR-3.3-5L	2A ,Enable, SENSE	TJ4220G-3.3	Contact Us



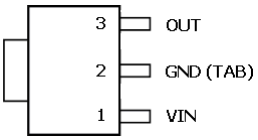
PIN CONFIGURATION



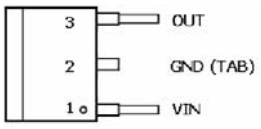
SOP8



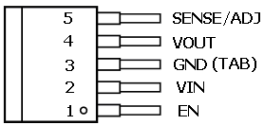
SOP8-PP



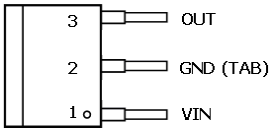
SOT223-3L



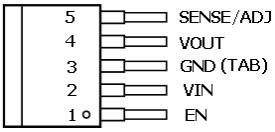
TO252-3L



TO252-5L



TO263-3L



TO263-5L

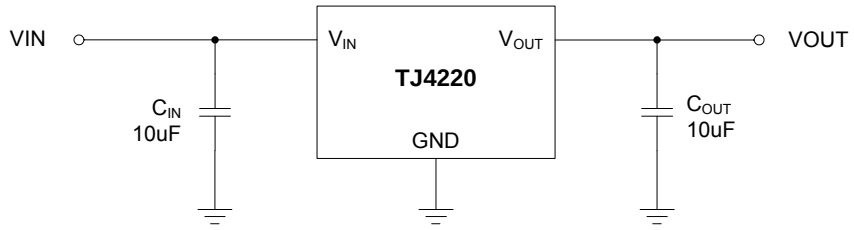
PIN DESCRIPTION

Pin No.	SOT223/TO252/TO263 3 LEAD		TO252 / TO263 5 LEAD		SOP8/SOP8-PP	
	Name	Function	Name	Function	Name	Function
1	V_{IN}	Input Supply	EN	Chip Enable	-	N.C.
2	GND	Ground	V_{IN}	Input Supply	EN	Chip Enable
3	V_{OUT}	Output Voltage	GND	Ground	V_{IN}	Input Supply
4	-	-	V_{OUT}	Output Voltage	-	N.C.
5	-	-	SENSE/ADJ	Remote Sense or Output Adjust	-	N.C.
6	-	-	-	-	V_{OUT}	Output Voltage
7	-	-	-	-	SENSE/ADJ	Remote Sense or Output Adjust
8	-	-	-	-	GND	Ground

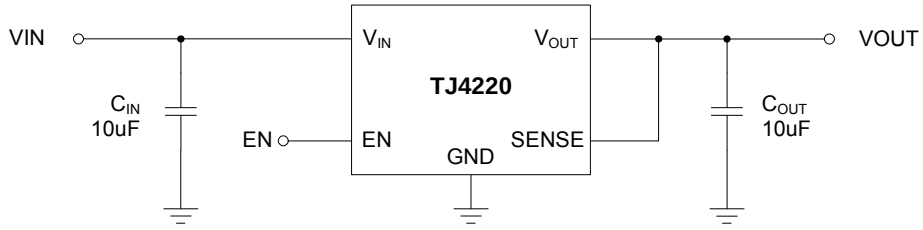
* Exposed Pad of SOP8-PP package should be externally connected to GND.

BASIC APPLICATION

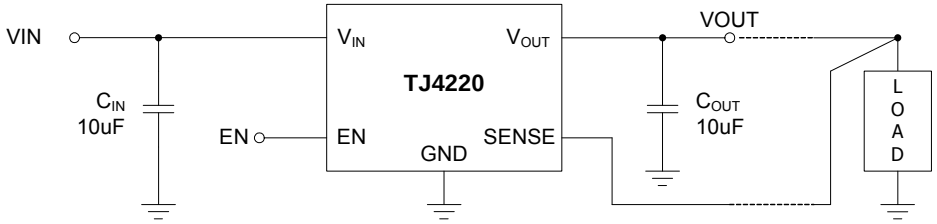
Typical 3 Pin Application



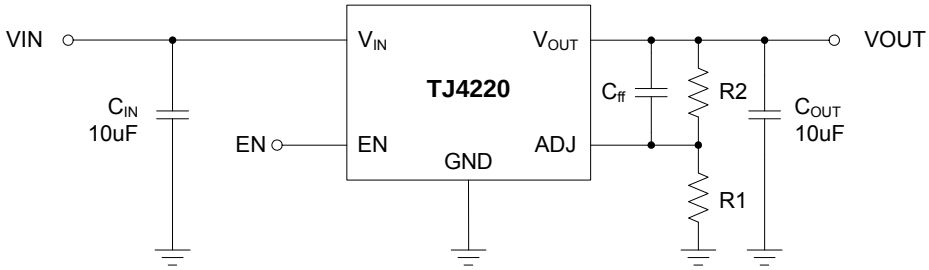
Typical 5 / 8 Pin Application



5 / 8 Pin Remote Load Sense Application



Typical Adjustable Version Application



* TJ4220 can deliver a continuous current of 2A over the full operating temperature. However, the output current is limited by the restriction of power dissipation which differs from packages. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of application. With respect to the applied package, the maximum output current of 2A may be still undeliverable.

* See Application Information.

ELECTRICAL CHARACTERISTICS(Note 1)

Limits in standard typeface are for TJ=25ºC, and limits in **boldface type** apply over the **full operating temperature range**.
Unless otherwise specified: V_{IN}(Note 2) = $V_{O(NOM)}$ + 1 V, I_L = 10 mA, C_{IN} = 10 uF, C_{OUT} = 10 uF, V_{EN} = V_{IN} - 0.3 V

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage Tolerance		V_O	V_{OUT}+1 V < V_{IN} < 5.5 V	-2 **-3**	0	2 **3**	%
Adjustable Pin Voltage (ADJ version)		V_{ADJ}	2.5 V < V_{IN} < 5.5 V	0.784 **0.776**	0.8	0.816 **0.824**	V
Line Regulation(Note 3)		ΔV_{LINE}	V_{OUT}+1 V < V_{IN} < 5.5 V	-	0.15	- **0.40**	%/V
Load Regulation(Note 3, 4)		ΔV_{LOAD}	10 mA < I_L < 2 A	-	0.20	0.50 **0.60**	%
Dropout Voltage(Note 5)		V_{DROP}	I_L = 200 mA	-	45	55 **65**	mV
			I_L = 2 A	-	400	500 **600**	
Ground Pin Current(Note 6)		I_{GND}	I_L = 200 mA	-	0.40	0.6 **1.0**	mA
			I_L = 2 A	-	0.40	0.6 **1.0**	
Ground Pin Current(Note 7)		I_{GND_OFF}	V_{EN} < 0.2 V	-	0.5	1 **2**	uA
Power Supply Rejection Ratio		PSRR	f = 1kHz	-	55	-	dB
			f = 1kHz, C_{FF} = 1uF	-	65	-	
Current Limit		I_{LIMIT}	-	-	5	-	A
Thermal Shutdown Temperature		T_{SD}	-	-	165	-	ºC
Enable threshold	Logic Low	V_{IL}	Output = Low	-	-	0.4	V
	Logic High	V_{IH}	Output = High	2.0	-	-	V
Enable Input Current		I_{EN}	V_{EN} = V_{IN}	-	0.1	- **1**	uA

Note 1. Stresses listed as the absolute maximum ratings may cause permanent damage to the device. These are for stress ratings. Functional operating of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibly to affect device reliability.

Note 2. The minimum operating value for input voltage is equal to either ($V_{OUT,NOM}$ + V_{DROP}) or 2.5V, whichever is greater.

Note 3. Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current.

Note 4. Regulation is measured at constant junction temperature by using a 10ms current pulse. Devices are tested for load regulation in the load range from 10mA to 2A.

Note 5. Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the dropout voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V

Note 6. Ground current, or quiescent current, is the difference between input and output currents. It's defined by I_{GND1} = I_{IN} - I_{OUT} under the given loading condition. The total current drawn from the supply is the sum of the load current plus the ground pin current.

Note 7. Ground current, or standby current, is the input current drawn by a regulator when the output voltage is disabled by an enable signal.

APPLICATION INFORMATION

Introduction

TJ4220 is intended for applications where high current capability and very low dropout voltage are required. It provides a simple, low cost solution that occupies very little PCB estate. Additional features include an enable pin to allow for a very low power consumption standby mode, an adjustable pin to provide a fully adjustable output voltage, and SENSE pin to provide better remote load regulation characteristics.

Component Selection

Input Capacitor :
A large bulk capacitance over than 10uF/A(Output Load) should be closely placed to the input supply pin of the TJ4220 to ensure that the input supply voltage does not sag. Also a minimum of 10uF ceramic capacitor is recommended to be placed directly next to the V_{IN} Pin. It allows for the device being some distance from any bulk capacitor on the rail. Additionally, input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.(See Fig.1)

Output Capacitor :
A minimum ceramic capacitor over than 10uF/A(Output Load) should be very closely placed to the output voltage pin of the TJ4220. Increasing capacitance will improve the overall transient response and stability.

Decoupling (Bypass) Capacitor :
In very electrically noisy environments, it is recommended that additional ceramic capacitors be placed from VIN to GND. The use of multiple lower value ceramic capacitors in parallel with output capacitor also allows to achieve better transient performance and stability if required by the application.(See Fig.1)

Feed-Forward Capacitor
To get the higher PSRR than the inherent performance of TJ4220, it is recommended that additional ceramic feed-forward capacitor be placed from VOUT pin to ADJ pin. The capacitance of feed-forward capacitor with range of 10pF to 1uF allows to achieve better PSRR performance when required by the application.(See Fig.2)

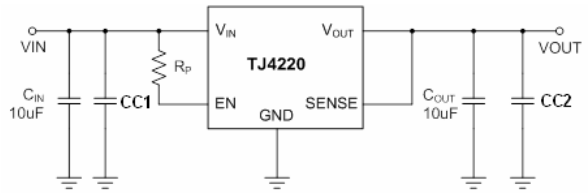


Fig. 1. Application with Decoupling Capacitor, CC1 & CC2

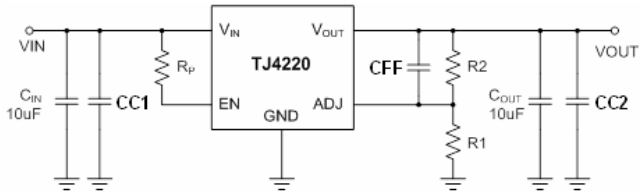


Fig. 2. Application with Feed-Forward Capacitor, CFF

Delayed Start-Up
When power sequence control is required or rising time of input supply voltage is over than 100usec, it is recommended to apply delayed start-up by using Cdelay as shown in Fig. 3. It can adjust proper delay by Rp-Cdelay time constant. And also it can prevent any unexpected transient characteristics at output voltage when the rising time of input supply voltage is as long as 100usec or longer.

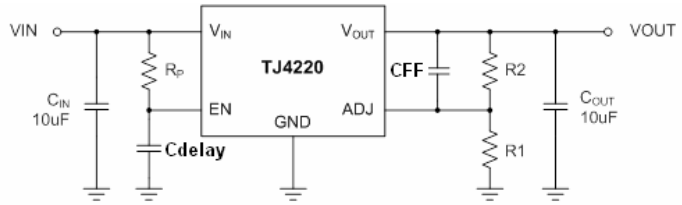
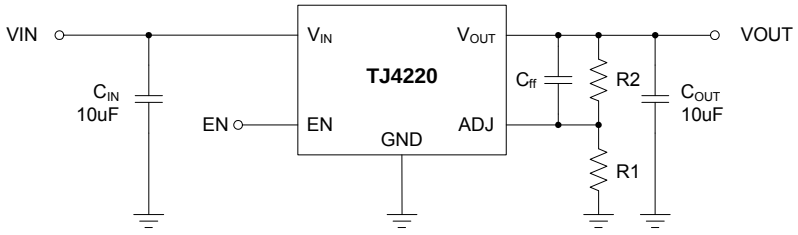


Fig. 3. Application with Delayed Start-Up

Output Adjustment (Adjustable Version)

An adjustable output device has output voltage range of 0.8V to 5.0V. The operating condition of V_{IN} and the operating characteristics of V_{OUT} depend on the dropout voltage performance in accordance with output load current presented at Fig. 7. To obtain a desired output voltage, the following equation can be used with R1 resistor range of 100Ω to 50kΩ.



$$R2 = R1\left(\frac{V_{OUT}}{0.8} - 1\right)$$

Fig. 4. Application for Adjustable Output Voltage

To enhance output stability, a feed-forward capacitor of 10nF to 1uF can be placed in series with V_{OUT} and ADJ.(Refer to "Component Selection" Section)

SENSE Pin

In applications where the regulator output is not very close to the load, the TJ4220 can provide better remote load regulation characteristics using the SENSE pin. TJ4220 regulates the voltage at the output pin. Hence, the voltage at the remote load will be lower than the voltage at the output pin as a value of the voltage drop across the trace series resistance. If the sense option pin is not required, the sense pin must be connected to the V_{OUT} pin. Connecting the sense pin to the remote load will provide regulation at the remote load because the TJ4220 regulates the voltage at the sense pin when the sense option pin is used.

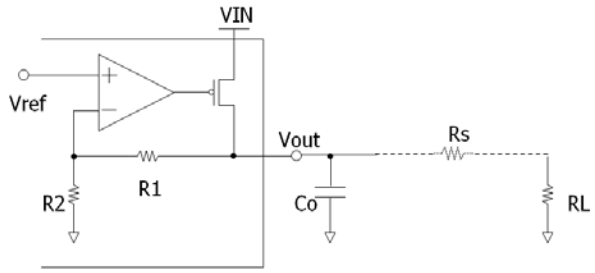


Fig. 5. Conventional Linear Regulator Application

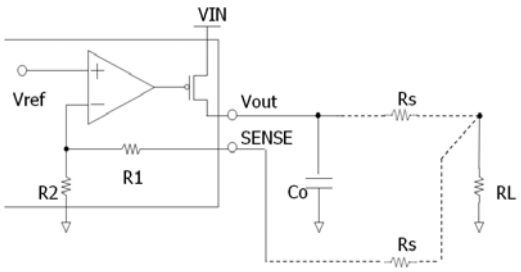


Fig.6. Remote Load Sense Application

Maximum Output Current Capability

The TJ4220 can deliver a continuous current of 2A over the full operating junction temperature range. However, the output current is limited by the restriction of power dissipation which differs from packages. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of application. With respect to the applied package, the maximum output current of 2A may be still undeliverable due to the restriction of the power dissipation of TJ4220. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.
The temperatures over the device are given by:

$T_C = T_A + P_D \times \theta_{CA}$
$T_J = T_C + P_D \times \theta_{JC}$
$T_J = T_A + P_D \times \theta_{JA}$

where T_J is the junction temperature, T_C is the case temperature, T_A is the ambient temperature, P_D is the total power dissipation of the device, θ_{CA} is the thermal resistance of case-to-ambient, θ_{JC} is the thermal

resistance of junction-to-case, and θ_{JA} is the thermal resistance of junction to ambient.
The total power dissipation of the device is given by:

$$P_D = P_{IN} - P_{OUT} = (V_{IN} \times I_{IN}) - (V_{OUT} \times I_{OUT})$$
$$= (V_{IN} \times (I_{OUT} + I_{GND})) - (V_{OUT} \times I_{OUT}) = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

where I_{GND} is the operating ground current of the device which is specified at the Electrical Characteristics. The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

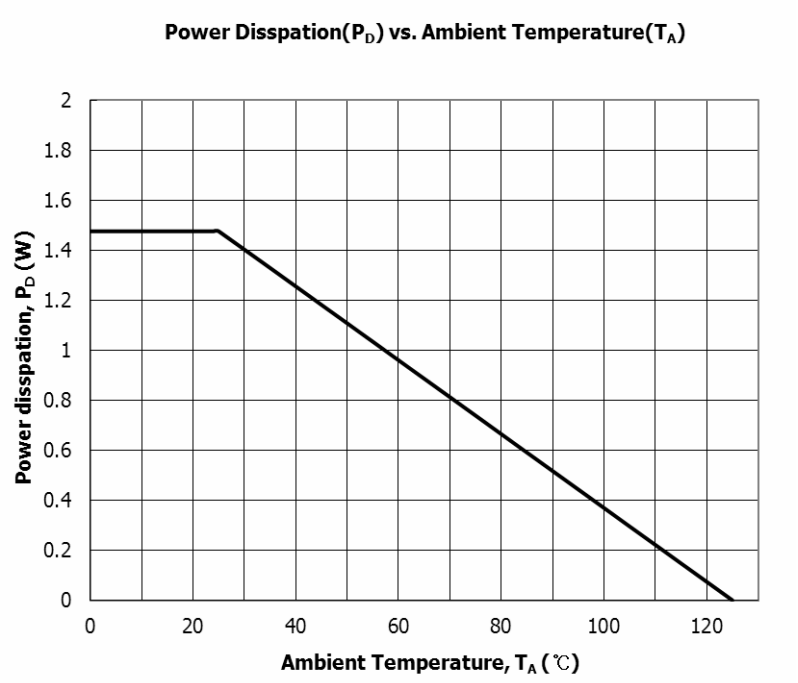
$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D$$

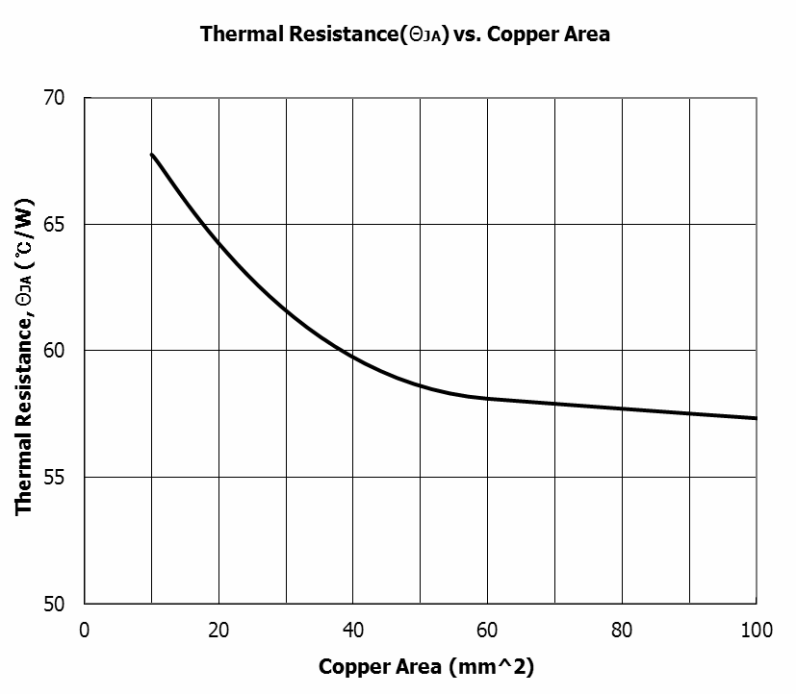
TJ4220 is available in SOT223, SOP8-PP, TO252 and TO263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow.

If proper cooling solution such as heat sink, copper plane area, or air flow is applied, the maximum allowable power dissipation could be increased. However, if the ambient temperature is increased, the allowable power dissipation would be decreased.



The graph above is valid for the thermal impedance specified in the Absolute Maximum Ratings section on page 1.

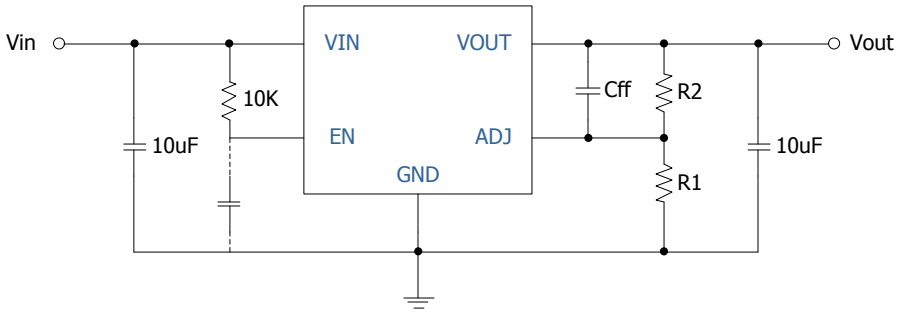
The θ_{JA} could be decreased with respect to the copper plane area. So, the specification of maximum power dissipation for an application is fixed, the proper plane area could be estimated by following graphs. Wider copper plane area leads lower θ_{JA}.



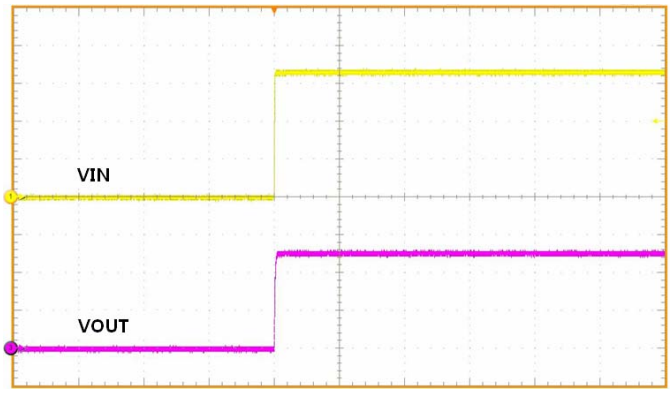
The maximum allowable power dissipation is also influenced by the ambient temperature. With the θ_{JA}-Copper plane area relationship, the maximum allowable power dissipation could be evaluated with respect to the ambient temperature. As shown in graph, the higher copper plane area leads θ_{JA}. And the higher ambient temperature leads lower maximum allowable power dissipation.

TYPICAL OPERATING CHARACTERISTICS

Test Circuit



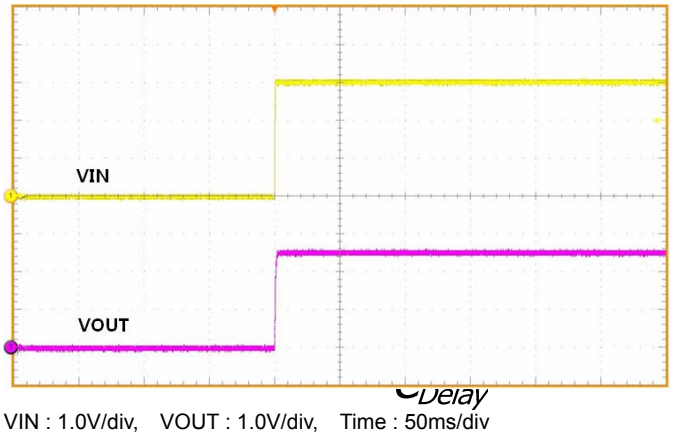
Case 1 (VIN = 3.3V, VOUT = 2.5V)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=0A

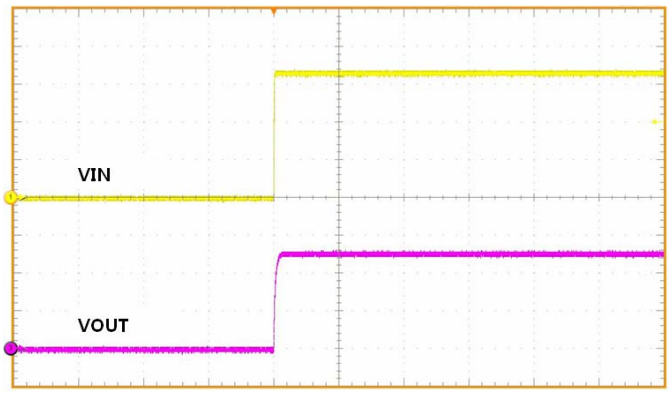
(Cff=10nF, R2=51KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=2A

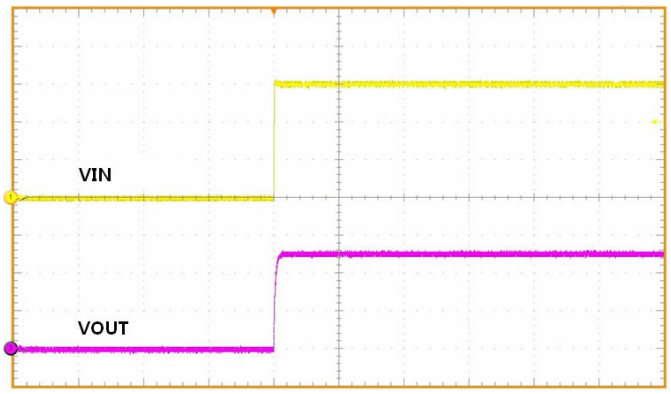
(Cff=10nF, R2=51KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=0A

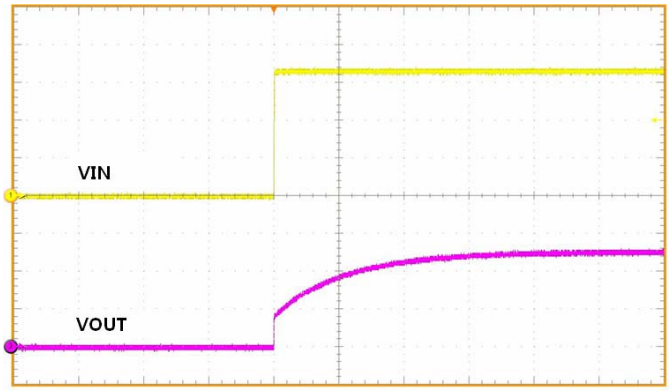
(Cff=10nF, R2=120KΩ, R1=56KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=2A

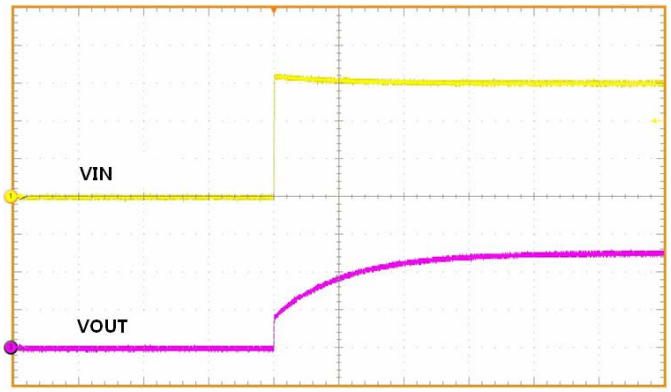
(Cff=10nF, R2=120KΩ, R1=56KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=0A

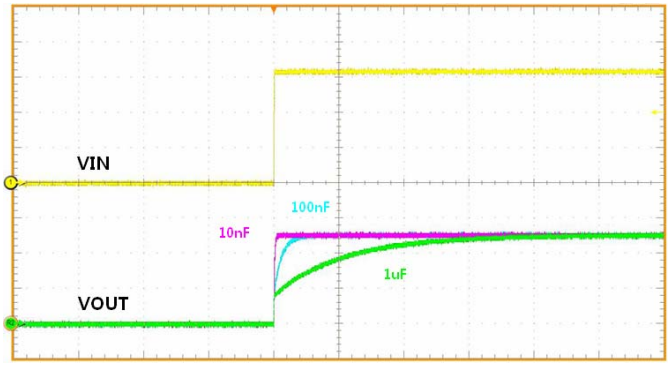
(Cff=1uF, R2=51KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=2A

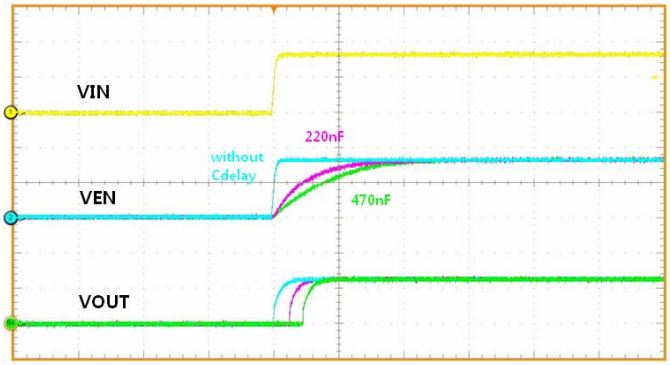
(Cff=1uF, R2=51KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 50ms/div

Start Up @ Iout=1A

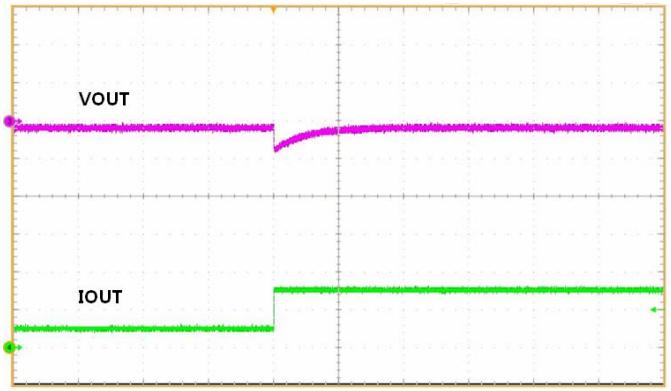
(Cff is varied, R2=51KΩ, R1=24KΩ)



VIN : 2.0V/div, VEN : 2.0V/div, VOUT : 2.0V/div, Time : 5ms/div

Start Up with Cdelay @ Iout=10mA

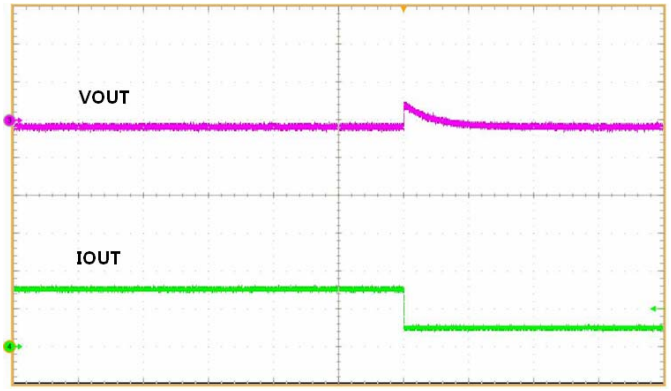
(Cdelay is varied, Cff=10nF, R2=51KΩ, R1=24KΩ)



IOUT : 1.0A/div, VOUT : 20mV/div, Time : 500ms/div

Load Transient Response

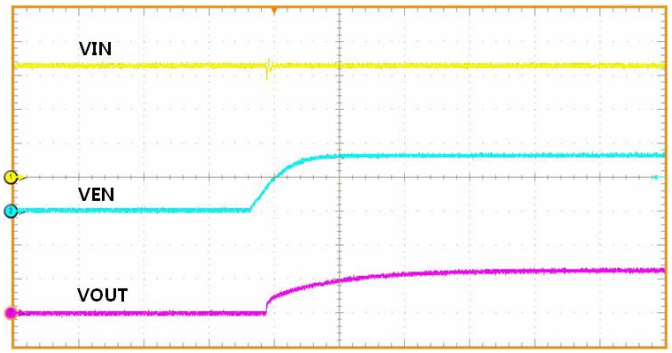
(Cff=10nF, R2=51KΩ, R1=24KΩ)



IOUT : 1.0A/div, VOUT : 20mV/div, Time : 500ms/div

Load Transient Response

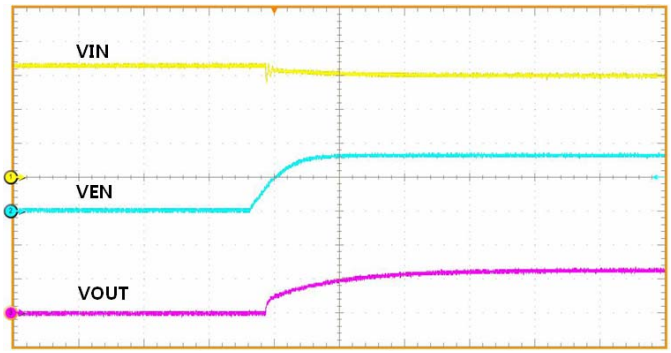
(Cff=10nF, R2=51KΩ, R1=24KΩ)



VIN : 1.0V/div, VEN : 2.0V, VOUT : 2.0V/div, Time : 500us/div

Start Up by external VEN @ Iout=0A

(Cff=10nF, R2=51KΩ, R1=24KΩ)

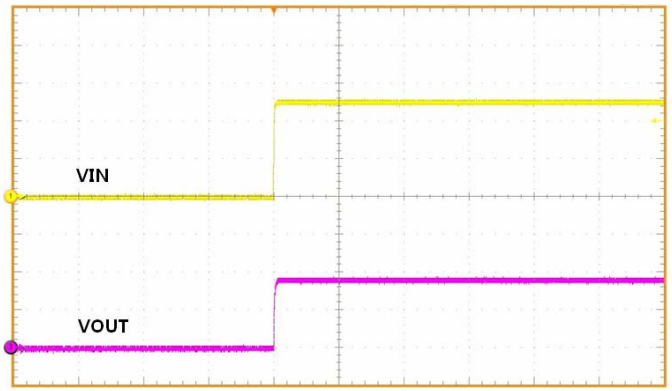


VIN : 1.0V/div, VEN : 2.0V, VOUT : 2.0V/div, Time : 500us/div

Start Up by external VEN @ Iout=2A

(Cff=10nF, R2=51KΩ, R1=24KΩ)

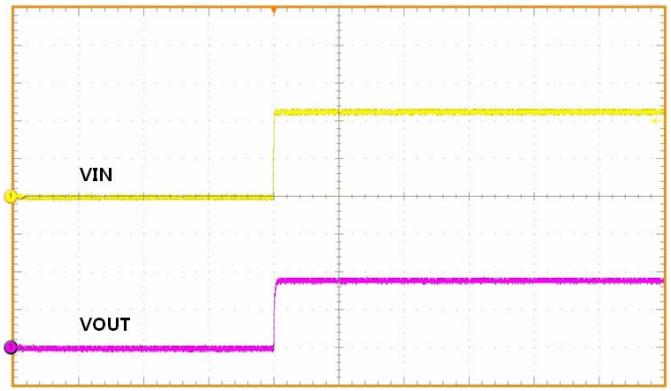
Case 2 (VIN = 2.5V, VOUT = 1.8V)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=0A

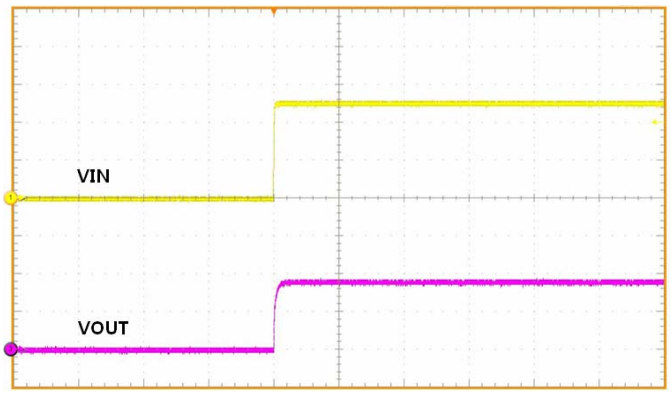
(Cff=10nF, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=2A

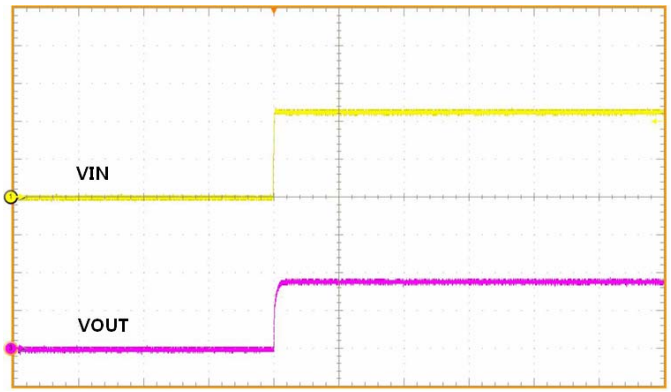
(Cff=10nF, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=0A

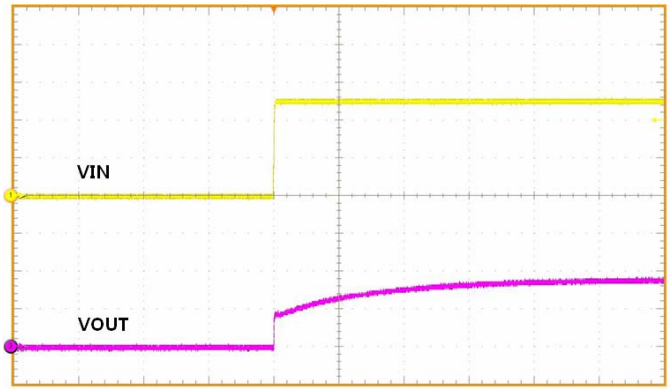
(Cff=10nF, R2=70KΩ, R1=56KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=2A

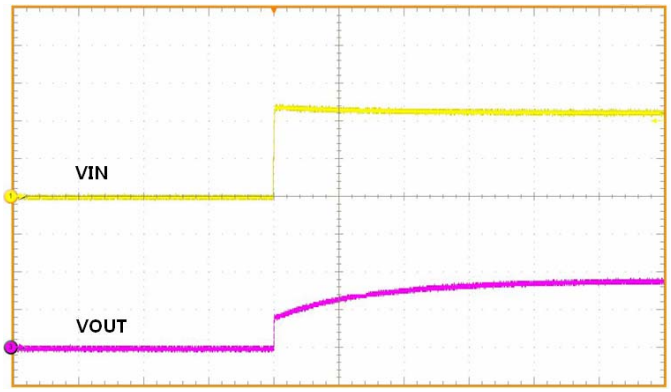
(Cff=10nF, R2=70KΩ, R1=56KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=0A

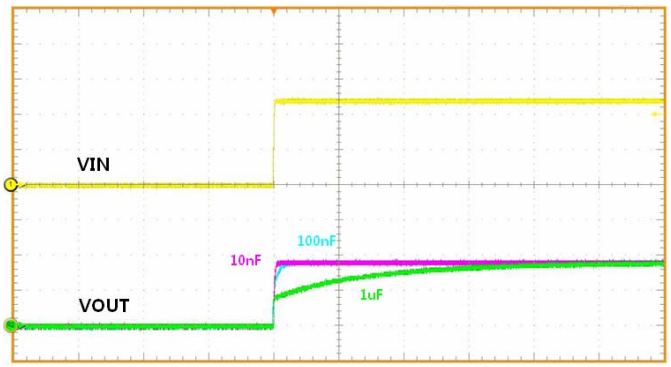
(Cff=1uF, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=2A

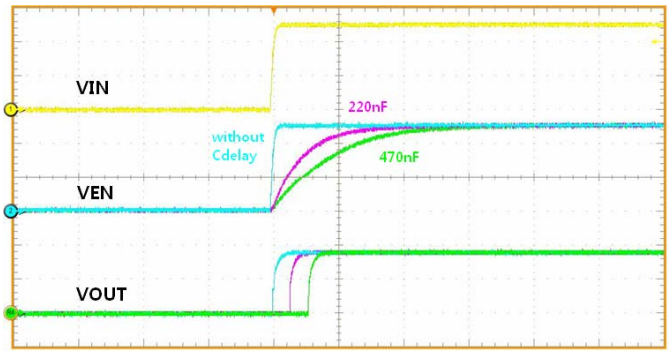
(Cff=1uF, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VOUT : 1.0V/div, Time : 20ms/div

Start Up @ Iout=1A

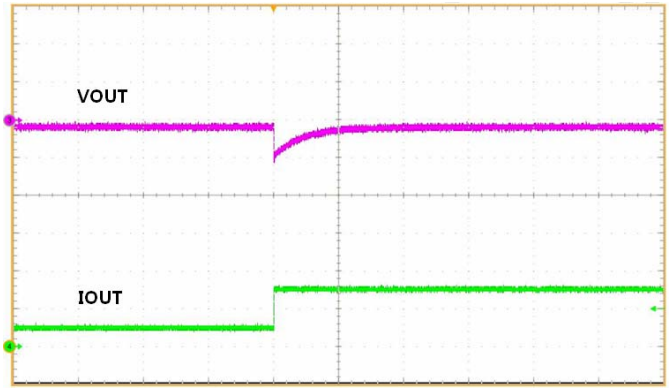
(Cff is varied, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VEN : 1.0V/div, VOUT : 1.0V/div, Time : 5ms/div

Start Up with Cdelay @ Iout=10mA

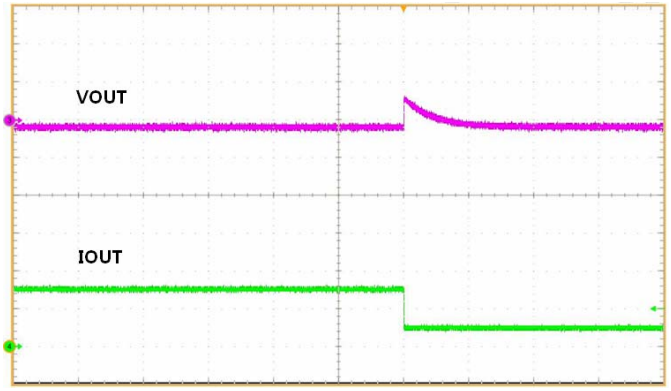
(Cdelay is varied, Cff=10nF, R2=30KΩ, R1=24KΩ)



IOUT : 1.0A/div, VOUT : 20mV/div, Time : 500ms/div

Load Transient Response

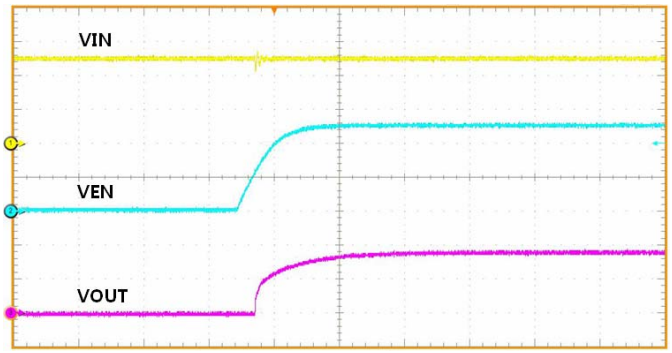
(Cff=10nF, R2=30KΩ, R1=24KΩ)



IOUT : 1.0A/div, VOUT : 20mV/div, Time : 500ms/div

Load Transient Response

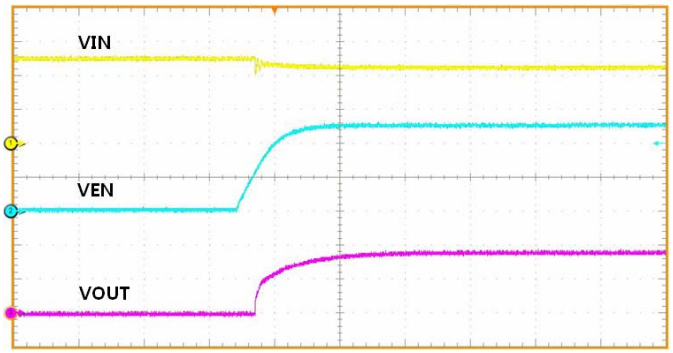
(Cff=10nF, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VEN : 1.0V, VOUT : 1.0V/div, Time : 500us/div

Start Up by external VEN @ Iout=0A

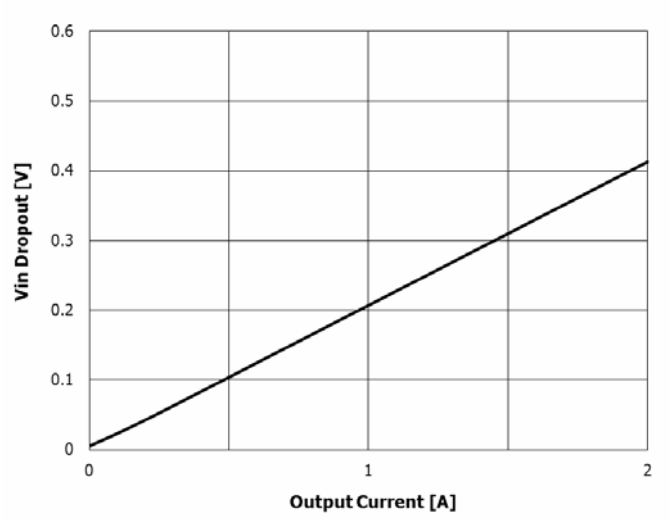
(Cff=10nF, R2=30KΩ, R1=24KΩ)



VIN : 1.0V/div, VEN : 1.0V, VOUT : 1.0V/div, Time : 500us/div

Start Up by external VEN @ Iout=2A

(Cff=10nF, R2=30KΩ, R1=24KΩ)



Dropout Voltage @ Vout=2.5V