# TJA1022

## Dual LIN 2.2A/SAE J2602 transceiver

Rev. 3 — 24 May 2018 Product data sheet

## 1. General description

The TJA1022 is a dual LIN transceiver that provides the interface between a Local Interconnect Network (LIN) master/slave protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602. The TJA1022T and TJA1022TK (SO14/HVSON14 packages) are pin compatible with the TJA1020, TJA1021, TJA1027 and TJA1029; the TJA1022HG (DHVQFN24 package) is pin compatible with the TJA1024 (see Section 18). The TJA1022, TJA1024, TJA1027 and TJA1029 are software compatible.

The transmit data streams generated by the protocol controller are converted by the TJA1022 into optimized bus signals shaped to minimize ElectroMagnetic Emissions (EME). The LIN bus output pins are pulled HIGH via internal termination resistors. For a master application, an external resistor in series with a diode should be connected between pin $V_{BAT}$ and each of the LIN pins. The receivers detect receive data streams on the LIN bus input pins and transfer them via pins RXD1 and RXD2 to the microcontroller.

Power consumption is very low when both transceivers are in Sleep mode. However, the TJA1022 can still be woken up via pins LIN1/LIN2 and SLP1_N/SLP2_N.

## 2. Features and benefits

### 2.1 General

- Two LIN transceivers in a single package
- LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602 compliant
- Baud rate up to 20 kBd
- Very low ElectroMagnetic Emissions (EME)
- Very low current consumption in Sleep mode with remote LIN wake-up
- Input levels compatible with 3.3 V and 5 V devices
- Integrated termination resistors for LIN slave applications
- Passive behavior in unpowered state
- Operational during cranking pulse: full operation from 5 V upwards
- Undervoltage detection
- K-line compatible
- Available in SO14, HVSON14 and DHVQFN24 packages
- Leadless HVSON14 (3.0 mm × 4.5 mm) and DHVQFN24 (3.5 mm × 5.5 mm) packages with improved Automated Optical Inspection (AOI) capability

- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- 14-pin variants pin-compatible with TJA1020, TJA1021, TJA1027 and TJA1029
- 24-pin variant pin-compatible subset of the TJA1024
- Software-compatible with the TJA1024, TJA1027 and TJA1029.

### 2.2 Protection

- Very high ElectroMagnetic Immunity (EMI)
- Very high ESD robustness: ±8 kV according to IEC 61000-4-2 for pins LIN1, LIN2 and $V_{BAT}$
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- Thermally protected
- Initial TXD dominant check when switching to Normal mode
- TXD dominant time-out function

## 3. Quick reference data

**Table 1. Quick reference data**

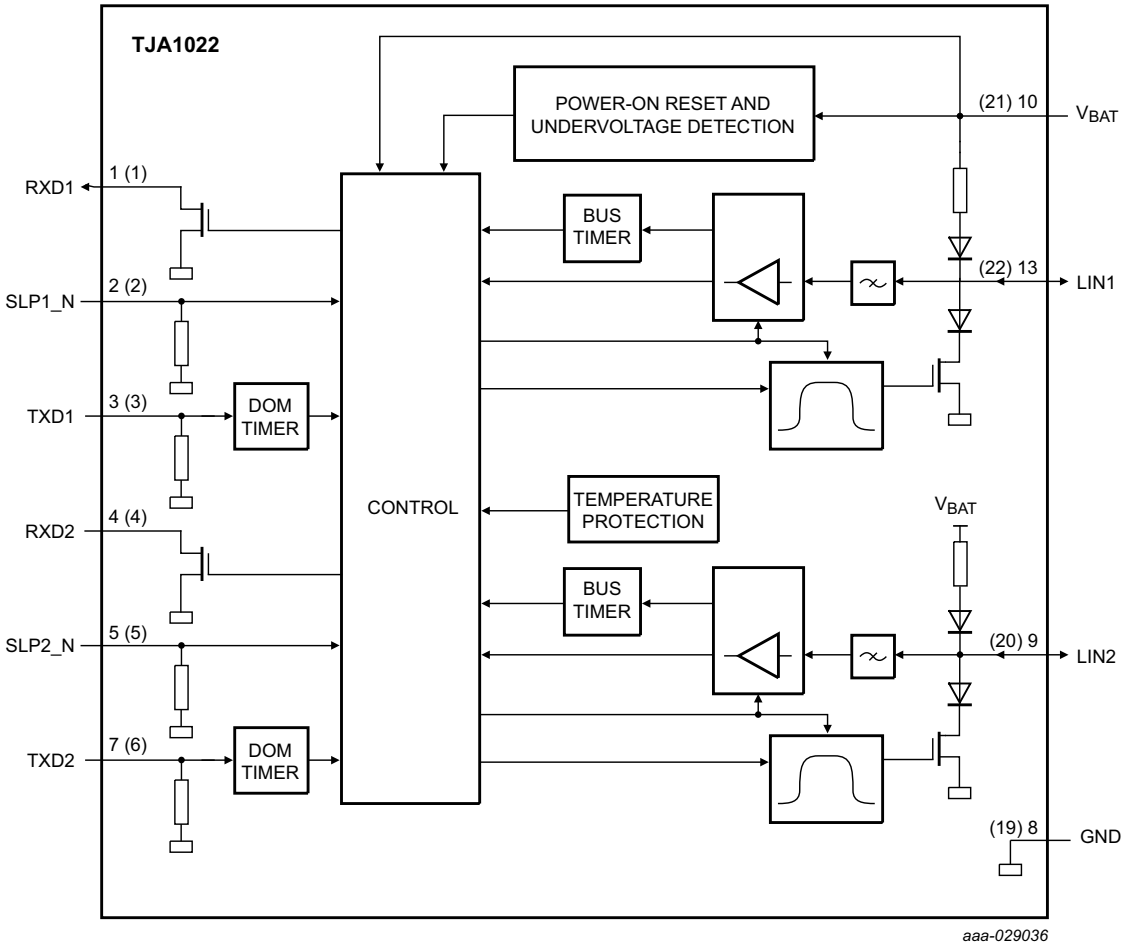
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | battery supply voltage | limiting values | −0.3 | - | +42 | V |
| | | operating range | 5 | - | 18 | V |
| $I_{BAT}$ | battery supply current | Sleep mode (both channels); bus recessive (both channels); $V_{LINx} = V_{BAT}$; $V_{SLPx\_N} = 0$ V | 2.5 | 7 | 10 | µA |
| | | Standby mode (both channels); bus recessive (both channels); $V_{LINx} = V_{BAT}$; $V_{SLPx\_N} = 0$ V | 2.5 | 7 | 10 | µA |
| | | Normal mode (both channels); bus recessive (both channels); $V_{TXDx} = 5$ V; $V_{LINx} = V_{BAT}$; $V_{SLPx\_N} = 5$ V | 300 | 1600 | 3200 | µA |
| $V_{LIN}$ | voltage on pin LIN | pins LIN1 and LIN2; limiting value; with respect to GND and $V_{BAT}$ | −42 | - | +42 | V |
| $V_{ESD}$ | electrostatic discharge voltage | on pins LIN1, LIN2 and $V_{BAT}$; according to IEC 61000-4-2 | −8 | - | +8 | kV |
| $T_{vj}$ | virtual junction temperature | | −40 | - | +150 | °C |

## 4. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TJA1022T | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| TJA1022TK | HVSON14 | plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm | SOT1086-2 |
| TJA1022HG | DHVQFN24 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm | SOT815-1 |

## 5. Block diagram

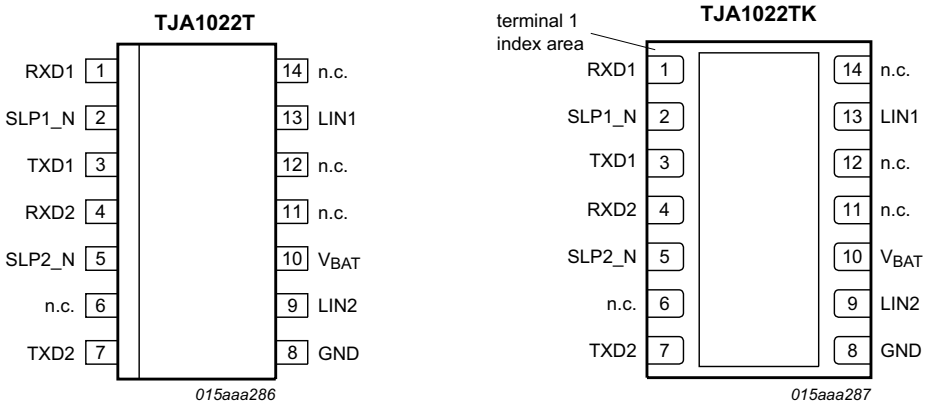



Pin numbers for the DHVQFN24 package are shown in brackets.

**Fig 1. Block diagram**

# 6. Pinning information

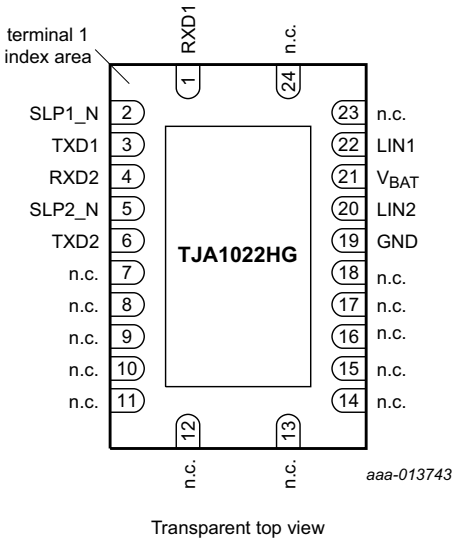
## 6.1 Pinning




TJA1022T: SO14 package

TJA1022TK: HVSON14 package

**Fig 2. Pin configuration diagrams: 14-pin**




Transparent top view

TJA1022HG: DHVQFN24

**Fig 3. Pin configuration diagram: 24-pin**

## 6.2 Pin description

**Table 3. Pin description: SO14 and HVSON14 packages**

| Symbol | Pin | Description |
|---|---|---|
| RXD1 | 1 | receive data output 1 (open-drain); active LOW after a wake-up event |
| SLP1_N | 2 | sleep control input 1 (active LOW); resets wake-up request on RXD1 |
| TXD1 | 3 | transmit data input 1 |

**Table 3. Pin description: SO14 and HVSON14 packages** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| RXD2 | 4 | receive data output 2 (open-drain); active LOW after a wake-up event |
| SLP2_N | 5 | sleep control input 2 (active LOW); resets wake-up request on RXD2 |
| n.c. | 6 | not connected |
| TXD2 | 7 | transmit data input 2 |
| GND | 8[1] | ground |
| LIN2 | 9 | LIN bus line 2 input/output |
| $V_{BAT}$ | 10 | battery supply |
| n.c. | 11 | not connected |
| n.c. | 12 | not connected |
| LIN1 | 13 | LIN bus line 1 input/output |
| n.c. | 14 | not connected |

[1] For enhanced thermal and electrical performance, the exposed center pad of the HVSON14 package should be soldered to board ground.

**Table 4. Pin description: DHVQFN24 package**

| Symbol | Pin | Description |
|---|---|---|
| RXD1 | 1 | receive data output 1 (open-drain); active LOW after a wake-up event |
| SLP1_N | 2 | sleep control input 1 (active LOW); resets wake-up request on RXD1 |
| TXD1 | 3 | transmit data input 1 |
| RXD2 | 4 | receive data output 2 (open-drain); active LOW after a wake-up event |
| SLP2_N | 5 | sleep control input 2 (active LOW); resets wake-up request on RXD2 |
| TXD2 | 6 | transmit data input 2 |
| n.c. | 7 to 18 | not connected |
| GND | 19[1] | ground |
| LIN2 | 20 | LIN bus line 2 input/output |
| $V_{BAT}$ | 21 | battery supply |
| LIN1 | 22 | LIN bus line 1 input/output |
| n.c. | 23, 24 | not connected |

[1] For enhanced thermal and electrical performance, the exposed center pad of the DHVQFN24 package should be soldered to board ground.

# 7. Functional description

The TJA1022 is the interface between the LIN master/slave protocol controller and the physical bus in a LIN network. According to the Open System Interconnect (OSI) model, this is the LIN physical layer.

The LIN transceivers are optimized for, but not limited to, automotive applications with excellent ElectroMagnetic Compatibility (EMC) performance.

## 7.1 LIN 2.x/ISO 17987/SAE J2602 compliant

The TJA1022 is fully LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602 compliant. The LIN physical layer is independent of higher OSI model layers (e.g. the LIN protocol). Consequently, nodes containing a LIN 2.2A-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1 and LIN 2.2).

## 7.2 Operating modes

The transceivers are fully operational in Normal mode. A low-power Sleep mode is also supported, as well as a Reset mode. Standby mode facilitates the transition between Sleep and Normal modes.

The transceivers operate independently (except in Reset mode), so one transceiver can be in Normal mode while the other is Sleep or Standby etc. Power consumption is at a minimum when both transceivers are in Sleep mode.

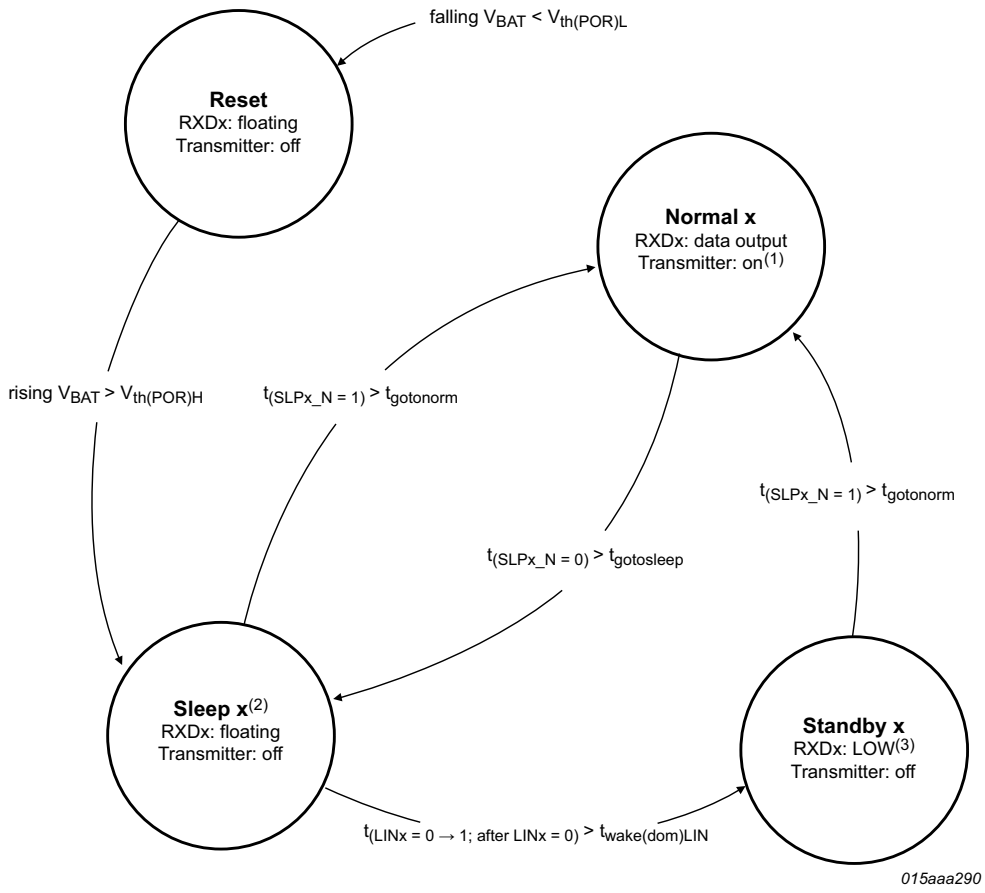
### 7.2.1 Normal mode

In Normal mode, the TJA1022 can transmit and receive data via the LIN bus lines. The transceivers operate independently, so one can be active while the other is off.

A transceiver will switch from Sleep or Standby mode to Normal mode if SLPx_N is held HIGH for $t_{gotonorm}$. If SLPx_N is held LOW for $t_{gotosleep}$, the transceiver will switch from Normal to Sleep mode.

The receivers detect data streams on the LIN bus lines (via pins LIN1 and LIN2) and transfer the input via pins RXD1 and RXD2 to the microcontroller (see Figure 7): HIGH for a recessive level and LOW for a dominant level on the bus. The receivers have supply-voltage related thresholds with hysteresis and integrated filters to suppress bus line noise.

Transmit data streams from the protocol controller are detected on the TXDx pins and are converted by the transmitters into optimized bus signals shaped to minimize EME. The LIN bus output pins are pulled HIGH via internal slave termination resistors. For a master application, an external resistor in series with a diode should be connected between pin $V_{BAT}$ and the appropriate LINx pin (see Figure 7).




(1) A positive edge on SLPx_N triggers a transition to Normal mode in the corresponding LIN transceiver; the LIN transmitter is enabled once TXDx goes HIGH; in the event of thermal shutdown, both LIN transceivers are disabled.

(2) Power dissipation is at a minimum when both transceivers are in Sleep mode.

(3) When a transceiver switches to Standby mode in response to a LIN bus wake-up event, the associated RXDx pin (RXD1 or RXD2) will be LOW to indicate which LIN channel was the source of the wake-up request.

**Fig 4. State diagram**

### 7.2.2 Sleep mode

A transceiver will switch to Sleep mode from Normal mode if SLPx_N is held LOW for $t_{gotosleep}$. The relevant LIN transmit path is disabled as soon as SLPx_N goes LOW. Power consumption is very low when both transceivers are in Sleep mode.

The voltage levels on LINx and TXDx have no effect on a transition to Sleep mode. So the transceiver will still switch to Sleep mode even if TXDx is held LOW or there is a continuous dominant level on LINx (e.g. due to a short circuit to ground).

Although current consumption is extremely low when both transceivers are in Sleep mode, the TJA1022 can still be woken up remotely via the LIN bus pins or by the microcontroller via pins SLPx_N. Filters on the receiver inputs (LIN1 and LIN 2) and on pins SLPx_N prevent unwanted wake-up events occurring due to automotive transients or radio frequency interference. To be valid, all wake-up events must be maintained for a specific length of time ($t_{wake(dom)LIN}$ for a remote wake-up and $t_{gotonorm}$ for a wake-up via SLPx_N). Pin RXDx is floating when a transceiver is in Sleep mode.

If a remote wake-up event (see Figure 5) is detected on either of the LIN bus lines, the associated transceiver will switch to Standby mode. A wake-up initiated by the microcontroller (SLPx_N HIGH for $t_{gotonorm}$) will cause the relevant transceiver to switch to Normal mode while the other transceiver remains in its current state.

### 7.2.3 Standby mode

Standby mode is an intermediate mode between Sleep and Normal modes. A transceiver will switch from Sleep mode to Standby mode in response to a LIN bus wake-up event. Pin RXDx will go low to indicate to the microcontroller the source of the remote wake-up (LIN1 or LIN2). A transceiver will switch from Standby to Normal mode if the microcontroller holds SLPx_N HIGH for $t_{gotonorm}$.

### 7.2.4 Reset mode

When the TJA1022 is in Reset mode, all input signals are ignored and all output drivers are off. The TJA1022 switches to Reset mode when the voltage on $V_{BAT}$ drops below the LOW-level power-on reset threshold, $V_{th(POR)L}$. When the voltage on $V_{BAT}$ rises above the HIGH-level power-on reset threshold, $V_{th(POR)H}$, the transceivers switch to Sleep mode.

**Table 5. Operating modes**

| Mode | SLPx_N | RXDx | Transmitter x | Description |
|---|---|---|---|---|
| Reset | x | floating | off | all inputs ignored; all output drivers off |
| Sleep x[1] | 0 | floating | off | no wake-up request detected |
| Standby x[2] | 0 | LOW[3] | off | remote wake-up request detected |
| Normal x | 1 | HIGH: recessive<br>LOW: dominant | on/off[4] | bus signal shaping enabled |

[1] Both transceivers enter Sleep mode after a power-on reset (e.g. after switching on $V_{BAT}$).

[2] The appropriate transceiver will switch automatically to Standby x mode if a remote LINx wake-up event is detected in Sleep x mode.

[3] RXDx will be LOW to indicate the source of the remote wake-up request; RXDx will go HIGH in response to a positive edge on pin SLPx_N.

[4] A positive edge on SLPx_N will trigger a transition to Normal mode; the transmitter will be off if TXDx is LOW and will be enabled as soon as TXDx goes HIGH.

## 7.3 Transceiver wake-up

### 7.3.1 Remote wake-up via the LIN bus

A falling edge on pin LINx followed by a LOW level maintained for $t_{wake(dom)LIN}$ followed by a rising edge on pin LINx triggers a remote wake-up (see Figure 5). It should be noted that the time period $t_{wake(dom)LIN}$ is measured either in Normal mode while TXDx is HIGH, or in Sleep mode irrespective of the status of pin TXDx.

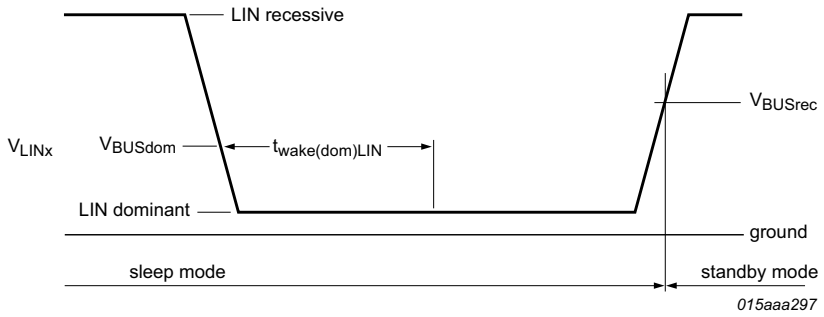



**Fig 5. Remote wake-up behavior**

### 7.3.2 Wake-up via SLPx_N

If SLPx_N is held HIGH for $t_{gotonorm}$, the transceiver will switch from Sleep mode to Normal mode.

## 7.4 Operation during automotive cranking pulses

TJA1022 remains fully operational during automotive cranking pulses because the LIN transceivers are fully specified down to $V_{BAT}$ = 5 V.

## 7.5 Operation when supply voltage is outside specified operating range

If $V_{BAT}$ > 18 V or $V_{BAT}$ < 5 V, the TJA1022 may remain operational, but parameter values cannot be guaranteed to remain within the operating ranges specified in Table 8 and Table 9.

In Normal mode:

- If the input level on pin TXDx is HIGH, the LIN transmitter output on pin LINx will be recessive.
- If the input level on pin LINx is recessive, the receiver output on pin RXDx will be HIGH.
- If the voltage on pin $V_{BAT}$ rises to 27 V (e.g. during an automotive jump-start), the total LIN network pull-up resistance should be greater than 680 Ω and the total LIN network capacitance should be less than 6.8 nF to ensure reliable LIN data transfer.
- If the voltage on pin $V_{BAT}$ drops below the LOW-level $V_{BAT}$ LOW threshold, $V_{th(VBATL)L}$, the active LIN transmit path(s) is interrupted and both LIN outputs will be recessive. The previously active LIN transmit path(s) is switched on again when $V_{BAT}$ rises above $V_{th(VBATL)H}$ and the associated TXDx pin is HIGH.

If the voltage on pin $V_{BAT}$ drops below the LOW-level power-on reset threshold, $V_{th(POR)L}$, the TJA1022 switches to Reset mode (i.e. all output drivers are disabled and all inputs are ignored). The TJA1022 switches to Sleep mode if $V_{BAT} > V_{th(POR)H}$.

## 7.6 Fail-safe features

Pin TXDx is pulled down to ground in order to force a predefined level on the transmit data input if the pin is disconnected.

Pin SLPx_N is pulled down to ground to ensure the transceiver is forced to Sleep x mode if SLPx_N is disconnected.

Pins RXD1 and RXD2 are set floating if $V_{BAT}$ is disconnected.

The current in the transmitter output stage is limited in order to protect the transmitter against short circuits to pins $V_{BAT}$ or GND.

A loss of power (pins $V_{BAT}$ and GND) has no impact on the bus lines or on the microcontroller. No reverse current will flow from the bus lines into the LINx pins. The current path from $V_{BAT}$ to LINx via the integrated LIN slave termination resistors remains. The TJA1022 can be disconnected from the power supply without influencing the LIN busses.

The output drivers on pins LIN1 and LIN2 are protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the thermal protection circuit disables the output drivers. The drivers are enabled again when the junction temperature falls below $T_{j(sd)}$ and pin TXDx is HIGH.

The initial TXD dominant check prevents the bus being driven to a permanent dominant state (blocking all network communications) if pin TXDx is forced permanently LOW by a hardware and/or software application failure. The input level on TXDx is checked after a transition to Normal mode. If TXDx is LOW, the transmit path will remain disabled and will only be enabled when TXDx goes HIGH.

Once the transmitter has been enabled, a TXD dominant time-out timer is started every time pin TXDx goes LOW. If the LOW state on pin TXDx persists for longer than the

TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus

line to recessive state. The TXD dominant time-out timer is reset when pin TXDx goes HIGH.

# 8. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to pin GND, unless otherwise specified. Positive currents flow into the IC.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | battery supply voltage | | | –0.3 | +42 | V |
| $V_{TXD}$ | voltage on pin TXD | pins TXD1 and TXD2 | | –0.3 | +7 | V |
| $V_{RXD}$ | voltage on pin RXD | pins RXD1 and RXD2 | | –0.3 | +7 | V |
| $V_{SLP\_N}$ | voltage on pin SLP_N | pins SLP1_N and SLP2_N | | –0.3 | +7 | V |
| $V_{LIN}$ | voltage on pin LIN | pins LIN1 and LIN2; with respect to GND and $V_{BAT}$ | | –42 | +42 | V |
| $\lvert\Delta V_{(LIN1-LIN2)}\rvert$ | voltage difference between pin LIN1 and pin LIN2 (absolute value) | | | - | 42 | V |
| $V_{ESD}$ | electrostatic discharge voltage | | | | | |
| | according to IEC 61000-4-2 | on pins LIN1, LIN2 and $V_{BAT}$ | [1] | –8 | +8 | kV |
| | human body model | on pins LIN1, LIN2 and $V_{BAT}$ | [2] | –8 | +8 | kV |
| | | on pins TXD1, TXD2, RXD1, RXD2, SLP1_N and SLP2_N | [2] | –2 | +2 | kV |
| | charge device model | all pins | | –750 | +750 | V |
| | machine model | all pins | [3] | –200 | +200 | V |
| $T_{vj}$ | virtual junction temperature | | [4] | –40 | +150 | °C |
| $T_{stg}$ | storage temperature | | | –55 | +150 | °C |

[1] Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

[3] Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH coil.

[4] Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_j = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value. The rating for $T_{vj}$ limits the allowable combinations of power dissipation (P) and ambient temperature ($T_{amb}$).

# 9. Thermal characteristics

**Table 7. Thermal characteristics**

*According to IEC 60747-1.*

| Symbol | Parameter | Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | SO14 package | [1] | 145 | K/W |
| | | HVSON14 package | [2] | 50 | K/W |
| | | DHVQFN24 package | [2] | 42.7 | K/W |

[1] According to JEDEC JESD51-2 and JESD51-3 at natural convection on 1s board.

[2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

# 10. Static characteristics

**Table 8. Static characteristics**

*$V_{BAT}$ = 5 V to 18 V; $T_{vj}$ = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at $V_{BAT}$ = 12 V; unless otherwise specified.*[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_{BAT}$ | battery supply voltage | | 5 | - | 18 | V |
| $I_{BAT}$ | battery supply current | Sleep mode (both channels); bus recessive (both channels); $V_{LINx} = V_{BAT}$; $V_{SLPx\_N}$ = 0 V | 2.5 | 7 | 10 | µA |
| | | Sleep mode (both channels); bus dominant (both channels); $V_{LINx}$ = 0 V; $V_{SLPx\_N}$ = 0 V; $V_{BAT}$ = 12 V | 300 | 800 | 3200 | µA |
| | | Standby mode (both channels); bus recessive (both channels); $V_{LINx} = V_{BAT}$; $V_{SLPx\_N}$ = 0 V | 2.5 | 7 | 10 | µA |
| | | Standby mode (both channels); bus dominant (both channels); $V_{LINx}$ = 0 V; $V_{SLPx\_N}$ = 0 V; $V_{BAT}$ = 12 V | 200 | 600 | 2000 | µA |
| | | Normal mode (both channels); bus recessive (both channels); $V_{TXDx}$ = 5 V; $V_{LINx} = V_{BAT}$; $V_{SLPx\_N}$ = 5 V | 300 | 1600 | 3200 | µA |
| | | Normal mode (both channels); bus dominant (both channels); $V_{TXDx}$ = 0 V; $V_{SLPx\_N}$ = 5 V; $V_{BAT}$ = 12 V | 1 | 4 | 10 | mA |
| **Undervoltage reset** | | | | | | |
| $V_{th(POR)L}$ | LOW-level power-on reset threshold voltage | power-on reset | 1.6 | 3.1 | 3.9 | V |
| $V_{th(POR)H}$ | HIGH-level power-on reset threshold voltage | | 2.3 | 3.4 | 4.3 | V |
| $V_{hys(POR)}$ | power-on reset hysteresis voltage | [2] | 0.05 | 0.3 | 1 | V |
| $V_{th(VBATL)L}$ | LOW-level $V_{BAT}$ LOW threshold voltage | | 3.9 | 4.4 | 4.7 | V |
| $V_{th(VBATL)H}$ | HIGH-level $V_{BAT}$ LOW threshold voltage | | 4.2 | 4.7 | 4.9 | V |
| $V_{hys(VBATL)}$ | $V_{BAT}$ LOW hysteresis voltage | [2] | 0.15 | 0.3 | 0.6 | V |
| **Pins TXDx and SLPx_N** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2 | - | 7 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | +0.8 | V |
| $V_{hys}$ | hysteresis voltage | [2] | 50 | 200 | 400 | mV |
| $R_{pd}$ | pull-down resistance | on TXDx | 50 | 125 | 325 | kΩ |
| | | on SLPx_N | 100 | 250 | 650 | kΩ |

**Table 8. Static characteristics** *...continued*

*$V_{BAT}$ = 5 V to 18 V; $T_{vj}$ = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at $V_{BAT}$ = 12 V; unless otherwise specified.*[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | LOW-level input current | $V_{TXDx}$ = 0 V or $V_{SLPx\_N}$ = 0 V | −5 | - | +5 | µA |
| **Pin RXDx (open-drain)** | | | | | | |
| $I_{OL}$ | LOW-level output current | $V_{RXDx}$ = 0.4 V | 2 | - | - | mA |
| $I_{LH}$ | HIGH-level leakage current | [2] | −5 | - | +5 | µA |
| **Pin LINx** | | | | | | |
| $I_{BUS\_LIM}$ | current limitation for driver dominant state | $V_{BAT}$ = 18 V; $V_{LINx}$ = 18 V; $V_{TXDx}$ = 0 V | 40 | - | 100 | mA |
| $I_{BUS\_PAS\_dom}$ | receiver dominant input leakage current including pull-up resistor | [2] $V_{BAT}$ = 12 V; $V_{LINx}$ = 0 V; $V_{TXDx}$ = 5 V | −600 | - | - | µA |
| $I_{BUS\_PAS\_rec}$ | receiver recessive input leakage current | [2] $V_{BAT}$ = 5 V; $V_{LINx}$ = 18 V; $V_{TXDx}$ = 5 V | - | 0 | 1 | µA |
| $I_{BUS\_NO\_GND}$ | loss-of-ground bus current | [2] $V_{BAT}$ = 18 V; $V_{LINx}$ = 0 V | −750 | - | +10 | µA |
| $I_{BUS\_NO\_BAT}$ | loss-of-battery bus current | [2] $V_{BAT}$ = 0 V; $V_{LINx}$ = 18 V | - | - | 1 | µA |
| $V_{BUSdom}$ | receiver dominant state | | - | - | $0.4V_{BAT}$ | V |
| $V_{BUSrec}$ | receiver recessive state | | $0.6V_{BAT}$ | - | - | V |
| $V_{BUS\_CNT}$ | receiver center voltage | $V_{BUS\_CNT}$ = ($V_{BUSdom}$ + $V_{BUSrec}$) / 2 | $0.475V_{BAT}$ | $0.5V_{BAT}$ | $0.525V_{BAT}$ | V |
| $V_{HYS}$ | receiver hysteresis voltage | $V_{HYS}$ = $V_{BUSrec}$ − $V_{BUSdom}$ | - | - | $0.175V_{BAT}$ | V |
| $V_{SerDiode}$ | voltage drop at the serial diode | [2] in pull-up path with $R_{slave}$; $I_{SerDiode}$ = 0.9 mA | 0.4 | - | 1.0 | V |
| $V_{O(dom)}$ | dominant output voltage | [2] Normal mode; $V_{TXDx}$ = 0 V; $V_{BAT}$ = 7.0 V | - | - | 1.4 | V |
| | | [2] Normal mode; $V_{TXDx}$ = 0 V; $V_{BAT}$ = 18 V | - | - | 2.0 | V |
| $R_{slave}$ | slave resistance | | 20 | 30 | 60 | kΩ |
| $C_{LIN}$ | capacitance on pin LIN | [2] pins LIN1 and LIN2; with respect to GND | - | - | 20 | pF |
| **Thermal shutdown** | | | | | | |
| $T_{j(sd)}$ | shutdown junction temperature | [2] | 150 | - | 200 | °C |

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not tested in production; guaranteed by design.

# 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

*$V_{BAT}$ = 5 V to 18 V; $T_{vj}$ = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at $V_{BAT}$ = 12 V, unless otherwise specified.*[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Duty cycles** | | | | | | |
| δ1 | duty cycle 1 | $V_{th(rec)(max)}$ = 0.744 × $V_{BAT}$; $V_{th(dom)(max)}$ = 0.581 × $V_{BAT}$; $t_{bit}$ = 50 µs; $V_{BAT}$ = 7 V to 18 V [2][4][5] | 0.396 | - | - | |
| | | $V_{th(rec)(max)}$ = 0.768 × $V_{BAT}$; $V_{th(dom)(max)}$ = 0.6 × $V_{BAT}$; $t_{bit}$ = 50 µs; $V_{BAT}$ = 5 V to 7 V [2][4][5] | 0.396 | - | - | |
| δ2 | duty cycle 2 | $V_{th(rec)(min)}$ = 0.422 × $V_{BAT}$; $V_{th(dom)(min)}$ = 0.284 × $V_{BAT}$; $t_{bit}$ = 50 µs; $V_{BAT}$ = 7.6 V to 18 V [3][4][5] | - | - | 0.581 | |
| | | $V_{th(rec)(min)}$ = 0.405 × $V_{BAT}$; $V_{th(dom)(min)}$ = 0.271 × $V_{BAT}$; $t_{bit}$ = 50 µs; $V_{BAT}$ = 5.6 V to 7.6 V [3][4][5] | - | - | 0.581 | |
| δ3 | duty cycle 3 | $V_{th(rec)(max)}$ = 0.778 × $V_{BAT}$; $V_{th(dom)(max)}$ = 0.616 × $V_{BAT}$; $t_{bit}$ = 96 µs; $V_{BAT}$ = 7 V to 18 V [2][4][5] | 0.417 | - | - | |
| | | $V_{th(rec)(max)}$ = 0.805 × $V_{BAT}$; $V_{th(dom)(max)}$ = 0.637 × $V_{BAT}$; $t_{bit}$ = 96 µs; $V_{BAT}$ = 5 V to 7 V [2][4][5] | 0.417 | - | - | |
| δ4 | duty cycle 4 | $V_{th(rec)(min)}$ = 0.389 × $V_{BAT}$; $V_{th(dom)(min)}$ = 0.251 × $V_{BAT}$; $t_{bit}$ = 96 µs; $V_{BAT}$ = 7.6 V to 18 V [3][4][5] | - | - | 0.590 | |
| | | $V_{th(rec)(min)}$ = 0.372 × $V_{BAT}$ $V_{th(dom)(min)}$ = 0.238 × $V_{BAT}$ $t_{bit}$ = 96 µs; $V_{BAT}$ = 5.6 V to 7.6 V [3][4][5] | - | - | 0.590 | |
| **Timing characteristics** | | | | | | |
| $t_{rx\_pd}$ | receiver propagation delay | rising and falling; $C_{RXDx}$ = 20 pF; $R_{RXDx}$ = 2.4 kΩ [5] | - | - | 6 | µs |
| $t_{rx\_sym}$ | receiver propagation delay symmetry | $C_{RXDx}$ = 20 pF; $R_{RXDx}$ = 2.4 kΩ; rising edge with respect to falling edge [5] | −2 | - | +2 | µs |
| $t_{wake(dom)LIN}$ | LIN dominant wake-up time | Sleep mode | 30 | 80 | 150 | µs |
| $t_{gotonorm}$ | go to normal time | time period for mode change from Sleep or Standby mode to Normal mode | 2 | 6 | 10 | µs |
| $t_{init(norm)}$ | normal mode initialization time | | 7 | - | 20 | µs |
| $t_{gotosleep}$ | go to sleep time | time period for mode change from Normal to Sleep mode | 2 | 6 | 10 | µs |
| $t_{to(dom)TXD}$ | TXD dominant time-out time | timer started at falling edge on TXDx | 6 | 12 | 50 | ms |

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 6.

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 6.

[4] Bus load conditions: $C_{BUS}$ = 1 nF and $R_{BUS}$ = 1 kΩ; $C_{BUS}$ = 6.8 nF and $R_{BUS}$ = 660 Ω; $C_{BUS}$ = 10 nF and $R_{BUS}$ = 500 Ω.

[5] See timing diagram in Figure 6.

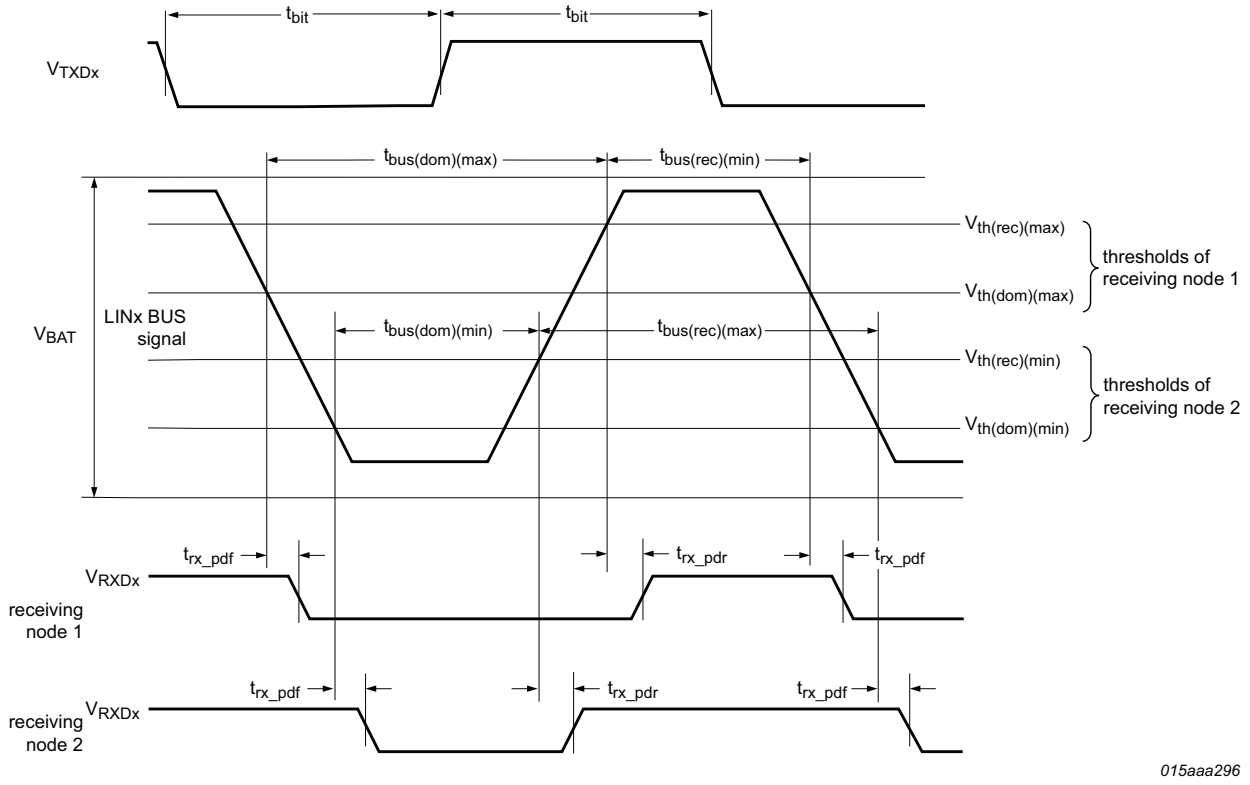
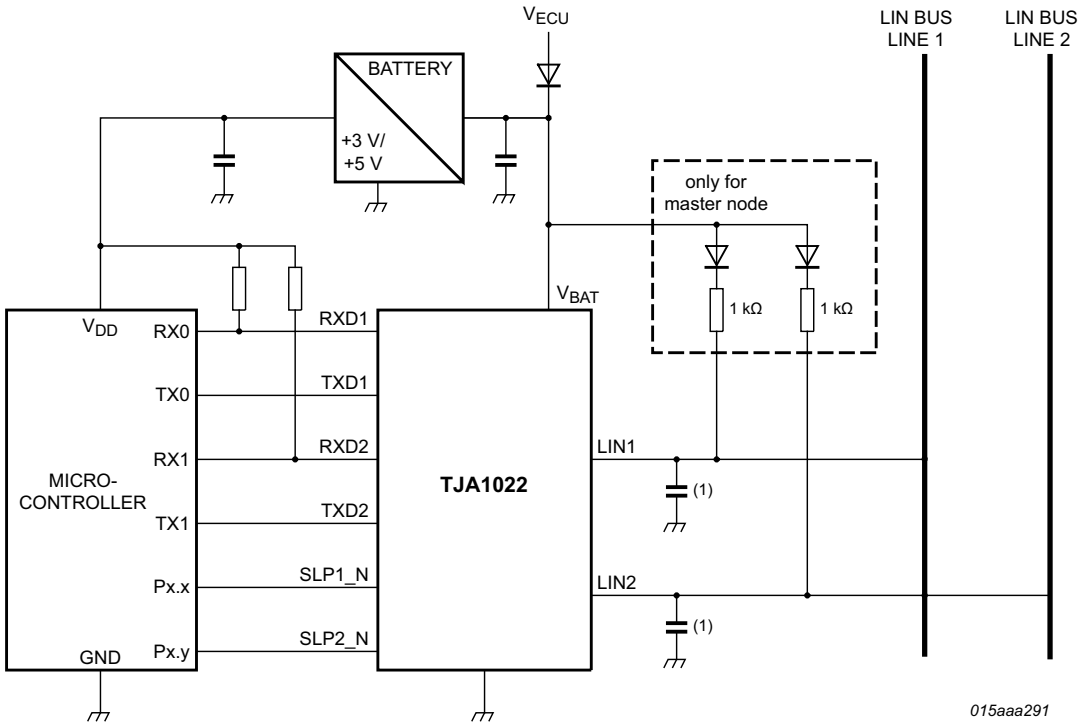



**Fig 6. Timing diagram of LIN transceiver duty cycle**

# 12. Application information

## 12.1 Application diagram




(1) Typically specified by car manufacturer: e.g. 680 pF for LIN master and 220 pF for LIN slave

**Fig 7. Application diagram**

## 12.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) of the 14-pin variants (SO14 and HVSON14 packages) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

**Table 10. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification**

| Pin | Test configuration | Value | Unit |
|---|---|---|---|
| LIN | no capacitor connected to LIN pin | ±12 | kV |
| | 220 pF capacitor connected to LIN pin | ±12 | kV |
| $V_{BAT}$ | 100 nF capacitor connected to $V_{BAT}$ pin | > \|14\| | kV |

## 12.3 Hardware requirements for LIN interfaces in automotive applications

The TJA1022 satisfies the "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications", Version 1.2, March 2011.

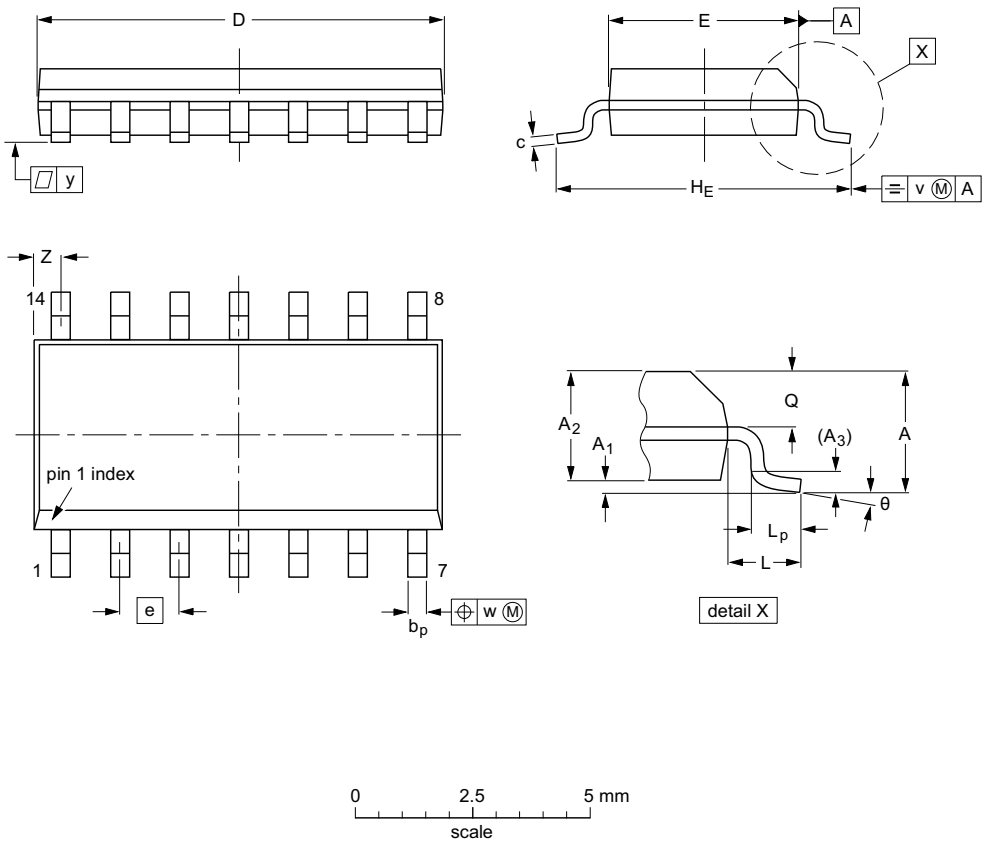
# 13. Test information

## 13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

# 14. Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

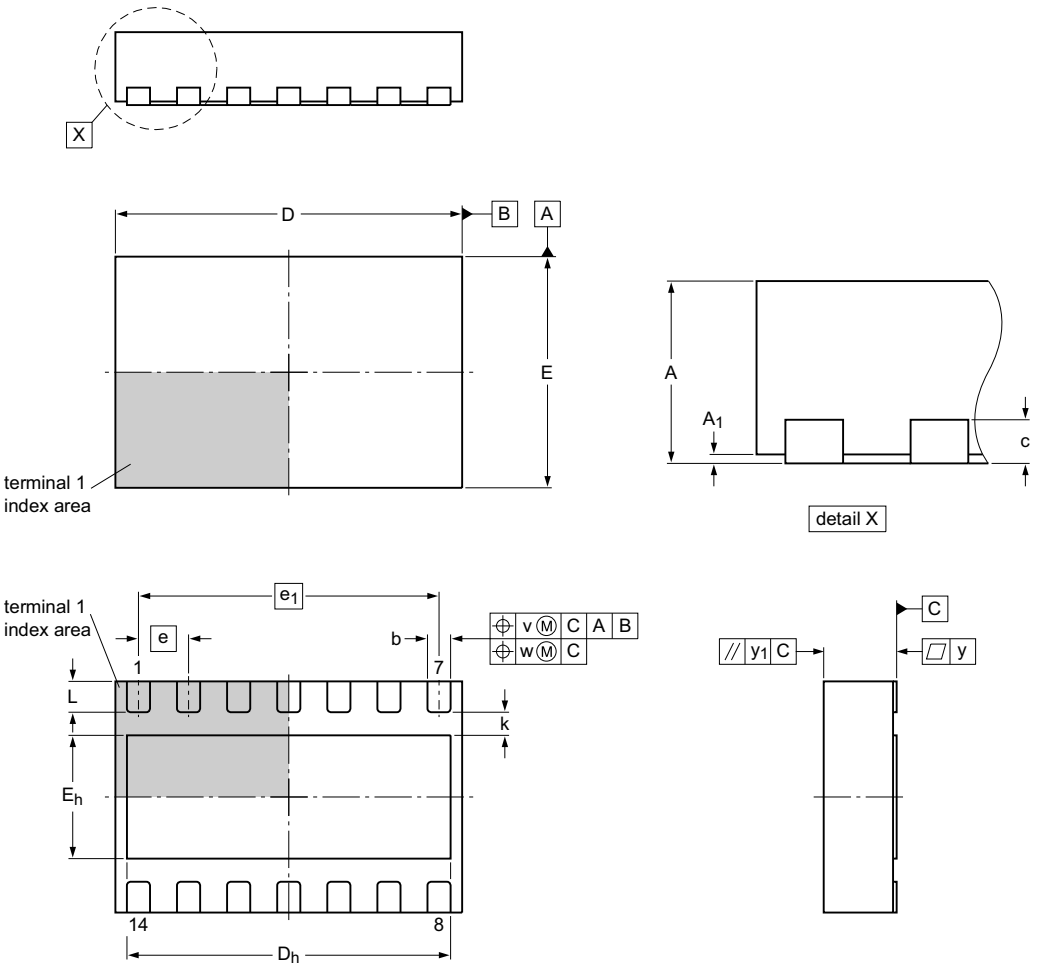
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT108-1 (SO14)**

**HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm** **SOT1086-2**




Dimensions

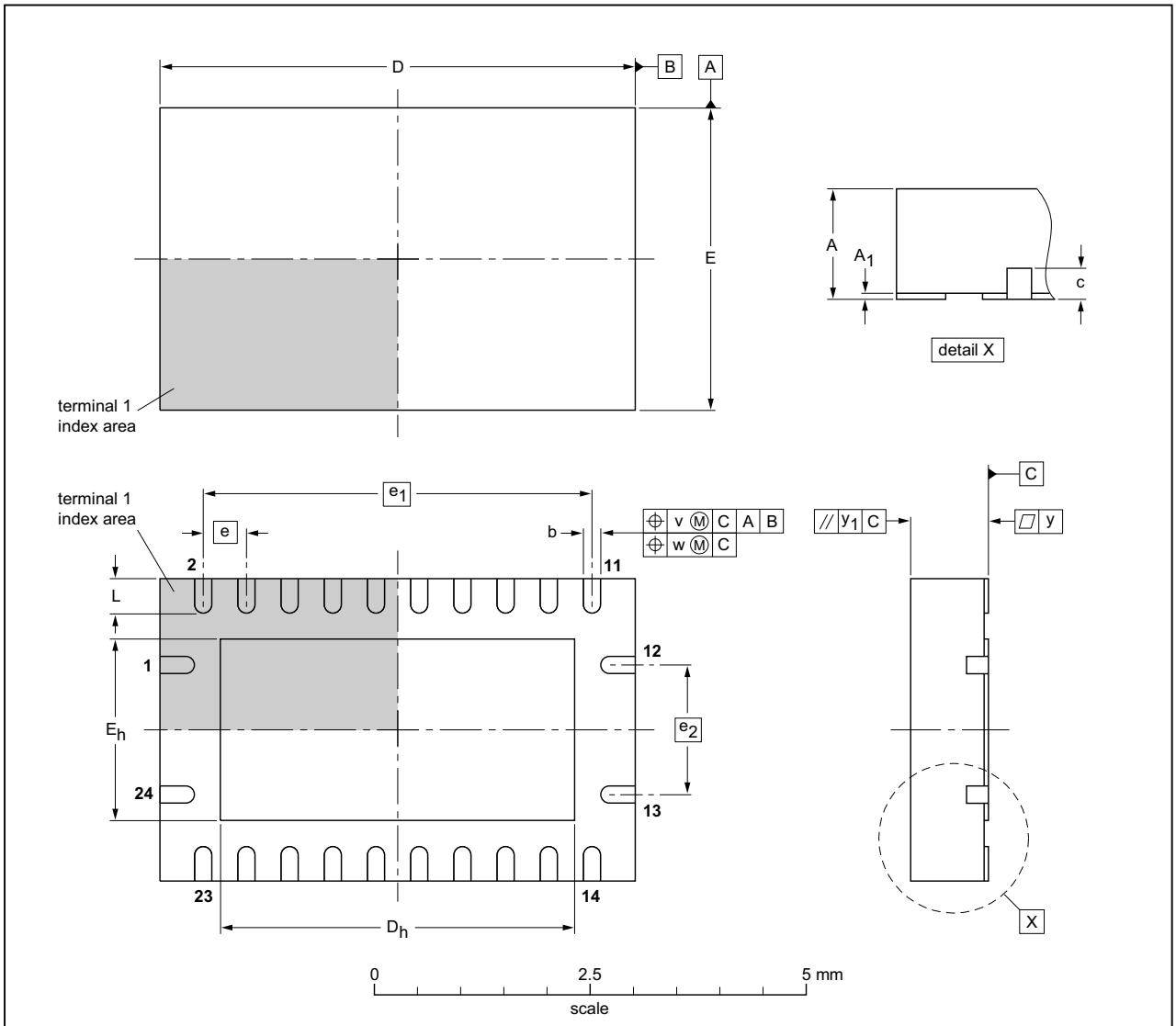
| Unit | | A | $A_1$ | b | c | D | $D_h$ | E | $E_h$ | e | $e_1$ | k | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.00 | 0.05 | 0.35 | | 4.6 | 4.25 | 3.1 | 1.65 | | | 0.35 | 0.45 | | | | |
| | nom | 0.85 | 0.03 | 0.32 | 0.2 | 4.5 | 4.20 | 3.0 | 1.60 | 0.65 | 3.9 | 0.30 | 0.40 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.29 | | 4.4 | 4.15 | 2.9 | 1.55 | | | 0.25 | 0.35 | | | | |

*sot1086-2*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1086-2 | - - - | MO-229 | - - - | | | ~~10-07-14~~ 10-07-15 |

**Fig 9. Package outline SOT1086-2 (HVSON14)**

**DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm** **SOT815-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 5.6<br>5.4 | 4.25<br>3.95 | 3.6<br>3.4 | 2.25<br>1.95 | 0.5 | 4.5 | 1.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT815-1 | - - - | - - - | - - - | | | 03-04-29 |

**Fig 10. Package outline SOT815-1 (DHVQFN24)**

# 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

**Table 11. SnPb eutectic process (from J-STD-020D)**

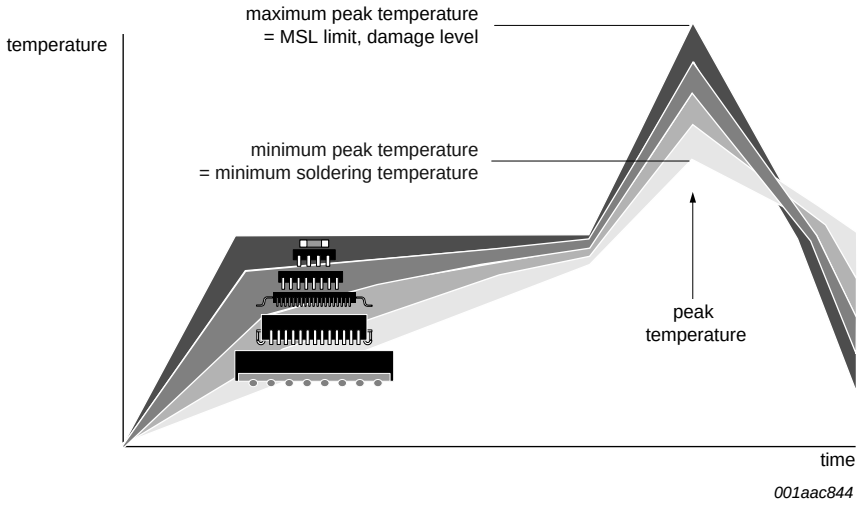
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 12. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.




MSL: Moisture Sensitivity Level

**Fig 11. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 17. Soldering of HVSON and DHVQFN packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering leadless package ICs can be found in the following application notes:

- *AN10365 "Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

## 18. Mounting

The TJA1022T/TJA1022TK pin layout has been designed to be compatible with the TJA1020, TJA1021, TJA1027 and TJA1029. This makes it possible to design a board with a single socket that can accommodate all five IC's. The appropriate device would be inserted into the socket, depending on the application, as illustrated in Figure 12. The TJA1022HG pin layout is a compatible subset of the TJA1024HG.

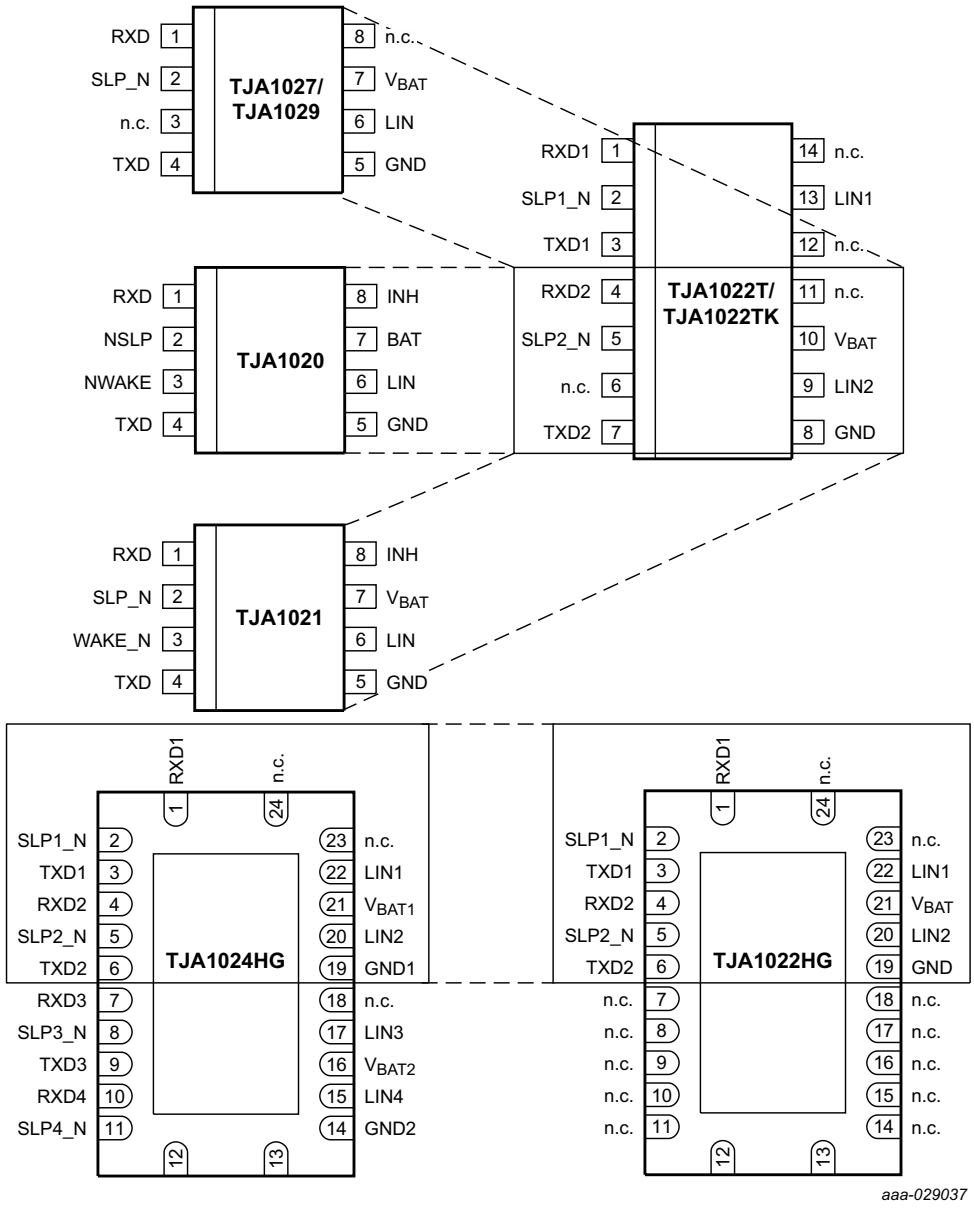



**Fig 12. TJA1022 pin compatibility**

# 19. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TJA1022 v.3 | 20180524 | Product data sheet | - | TJA1022 v.2 |
| Modifications: | • Added variant TJA1022HG in DHVQFN24 package<br>• ISO 17987-4:2016 (12 V LIN) compliant<br>• Figure 7, Figure note 1 amended | | | |
| TJA1022 v.2 | 20120424 | Product data sheet | - | TJA1022 v.1 |
| TJA1022 v.1 | 20130330 | Product data sheet | - | - |

# 20. Legal information

## 20.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 22. Contents





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**Document identifier: TJA1022**