TK18

Capacitive Touch Key Flash MCU with ADC/PWM/LED Driver

Datasheet

TK MCU Series

Revision 1.7
Jan. 2016

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Revision History

Version	Content	Date
V1.0	Initial release	2015/05
V1.1	Updated DC/AC characteristics → Max. IDD	2015/05
V1.2	Updated DC/AC characteristics → A/D & Data Flash	2015/06
V1.3	Updated Application Circuit	2015/06
V1.4	1. Add pin assignment note 2. CEXT Pin function list (in section 10 I/O introduction) 3. Add X-ISP use note from Appendix 1	2015/08
V1.5	1. Updated GPIO26 & GPIO27 initialize status 2. UART changed to half-duplex	2015/09
V1.6	1. Add ADC_CTRL Bit4 note 2. Updated I^2C section	2015/11
V1.7	Updated Timer & UART Section	2016/01

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1.General Description

1.1 Overview

TK18 ia a 8-bit flash microcontroller embedded with 8501 core and capacitive touch keys solutions. The operating voltage is from 2.7V to 5.5V and operating temperature is from -40℃ to 85℃. There is also a 28 MHz internal high-accuracy oscillator for system frequency. TK18 support up to 28-channel touch keys and includes: 32K bytes flash memory, 128 bytes Data Flash, 256bytes IRAM and 1K bytes XRAM, 4×8-bit PWM, 6×10-bit high resolution ADC and I^2C, half-duplex UART communication interfaces.

All TK18 ports are interchangeable with GPIO ports. Some ports provide high current driving forces, among which COM0~COM5, with high current driving capatility, can directly drive digitrons or LED indicators and support maximum of 7 COM×8 SEG hardware driving control.

TK18, an industrial grade IC with excellent anti-EFT and CS capability. It is an ideal touch key solution for home appliances that require high anti- EFT capatility such as microwave ovens, kitchen hoods, dish washers, and rice cooker.

1.2 Characteristics

- **Core**
  - 2T 8051 MCU
  - maximum system frequency: 28 MHz
  - operation voltage: 2.7V – 5.5V
  - operating temperature range: -40℃- 85℃
  - embedded RC high-accuracy oscillator at 28MHz ± 3% -40℃ ~ 85℃ that can save external
- **Memory**
  - 32K bytes flash memory
  - 256 bytes IRAM
  - 1K bytes XRAM
  - 128- bytes EEPROM (Data Flash)
  - online system update ISP (In-System Programming)
  - online circuit update ICP (In-Circuit Programming)
  - online TK signal debugging
- **maximum of 28-channel touch key**
- **maximum of 36 general GPIOs**
- **maximum of 7 COM×8 SEG hardware LED driving control**
  - 146mA high current drive from each COM0~COM5
- **4×8-bit PWM**
- **Analog to Digital Converter (ADC)**
  - 6 channels available
  - 10 bits resolution
  - maximum sampling frequency: 65 kSPS
- **Connectivity**
  - 1 set of I²C device (maximum 400 kHz)
  - 1 set of half-duplex UART interface
- **2 units of 16-bit timer/counter**
- **LVR resetting at low voltage**
- **LVD detection at low voltate**
- **16 bit watch-dog timer**

1.3 Ordering Information

Part Number	VDD	Flash (Bytes)	RAM (Bytes)	TK	LED Driver	I/O	Connectivity		A/D	PWM	Package
							UART	I^2C			
TK18A10W6B	2.7V ~5.5V	32K	256 + 1K	10	---	12	1	1	10-bitx3	8-bitx3	NSOP16
TK18A14W0B	2.7V ~5.5V	32K	256 + 1K	14	5COMx 8SEG	16	1	1	10-bitx3	8-bitx2	SOP20
TK18A18W4B	2.7V ~5.5V	32K	256 + 1K	18	5COMx 8SEG	20	1	1	10-bitx4	8-bitx3	SOP24
TK18A18U4B	2.7V ~5.5V	32K	256 + 1K	18	5COMx 8SEG	20	1	1	10-bitx4	8-bitx3	QFN24
TK18A22W8B	2.7V ~5.5V	32K	256 + 1K	22	7COMx 8SEG	24	1	1	10-bitx4	8-bitx3	SOP28
TK18A26W2B	2.7V ~5.5V	32K	256 + 1K	26	7COMx 8SEG	28	1	1	10-bitx6	8-bitx3	SOP32
TK18A26U2B	2.7V ~5.5V	32K	256 + 1K	26	7COMx 8SEG	28	1	1	10-bitx6	8-bitx3	QFN32
TK18A28Q4B	2.7V ~5.5V	32K	256 + 1K	28	7COMx 8SEG	36	1	1	10-bitx6	8-bitx4	LQFP44

Table 1-1 TK18 Serial Product Selection Table

Naming Rules

TK18A28Q4B

- Product version
- Packaging types：Q4=LQFP44，W2=SOP32，U2=QFN32，W8=SOP28，W4=SOP24， U4=QFN24， W0=SOP20，W6=NSOP16
- Maximum number of supported TK channels
- Product type: A=32K bits Flash ROM
- Product: TKxx=Touch-key Single-Chip Microcomputer

1.4 System block diagram

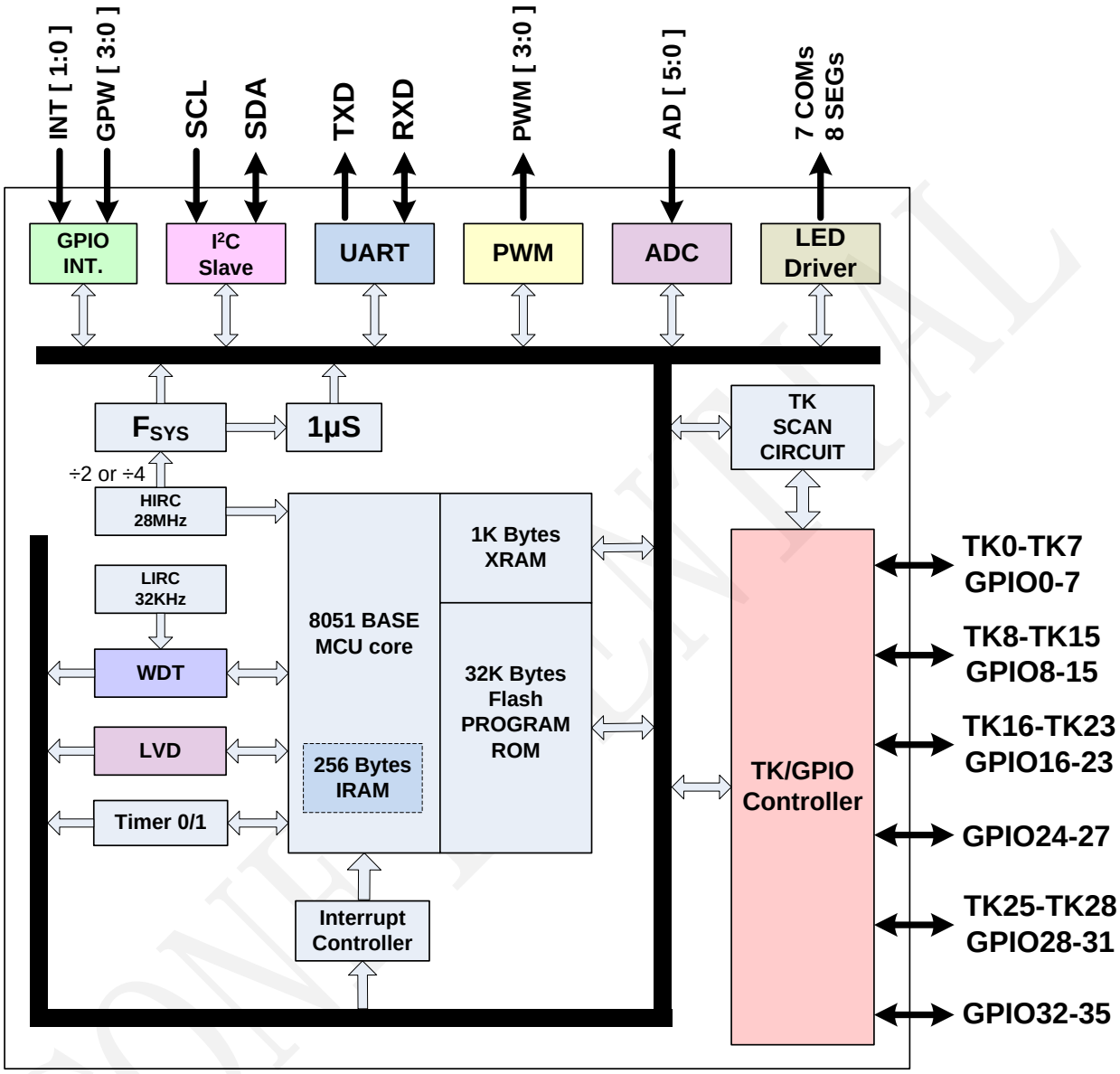
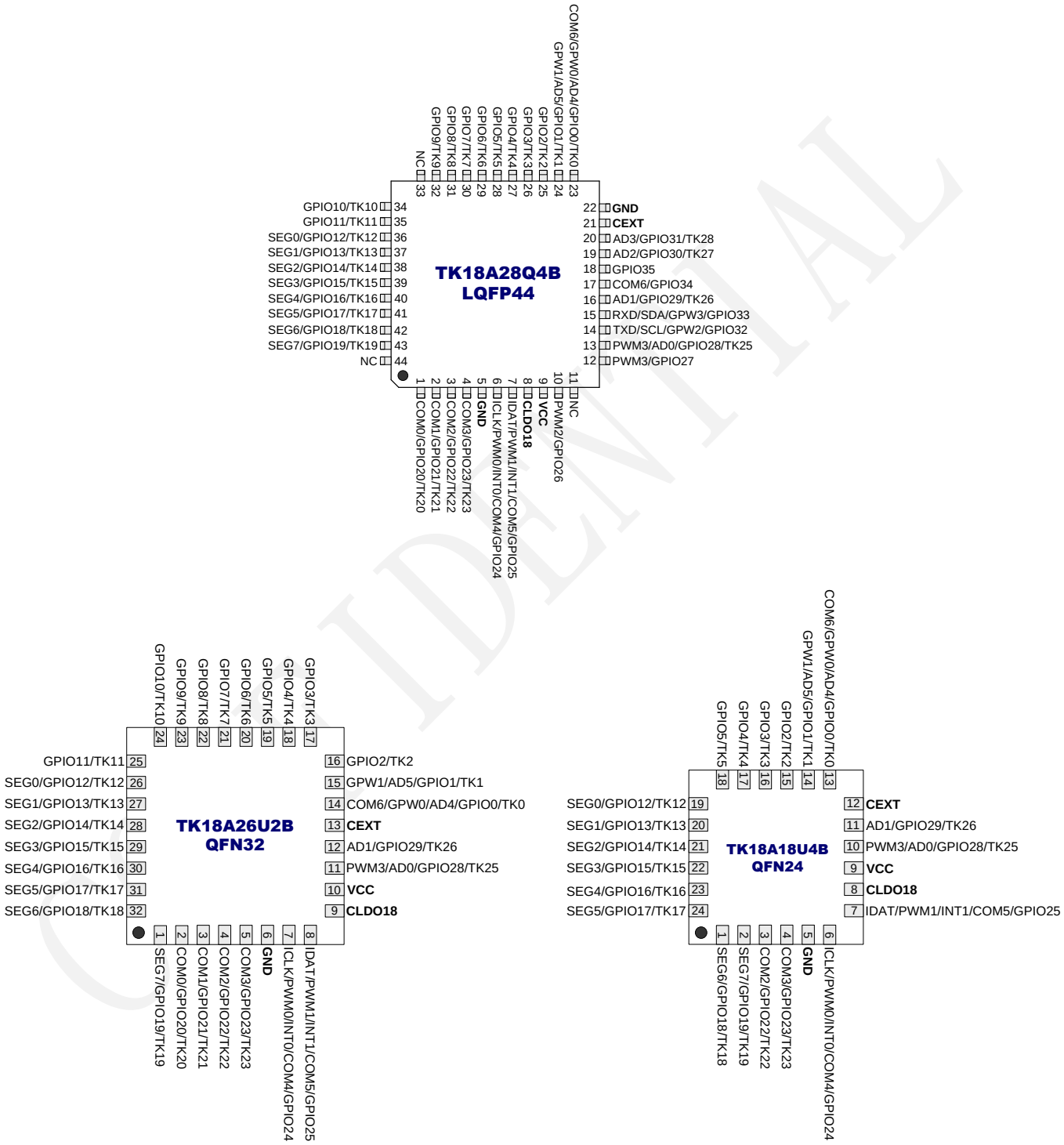


Diagram 1-1 TK18 Block Diagram

1.5 Pins Assignment and Description

1.5.1 Pins package diagram



Note 1 : Unused pin should be set to I/O mode and output Low.

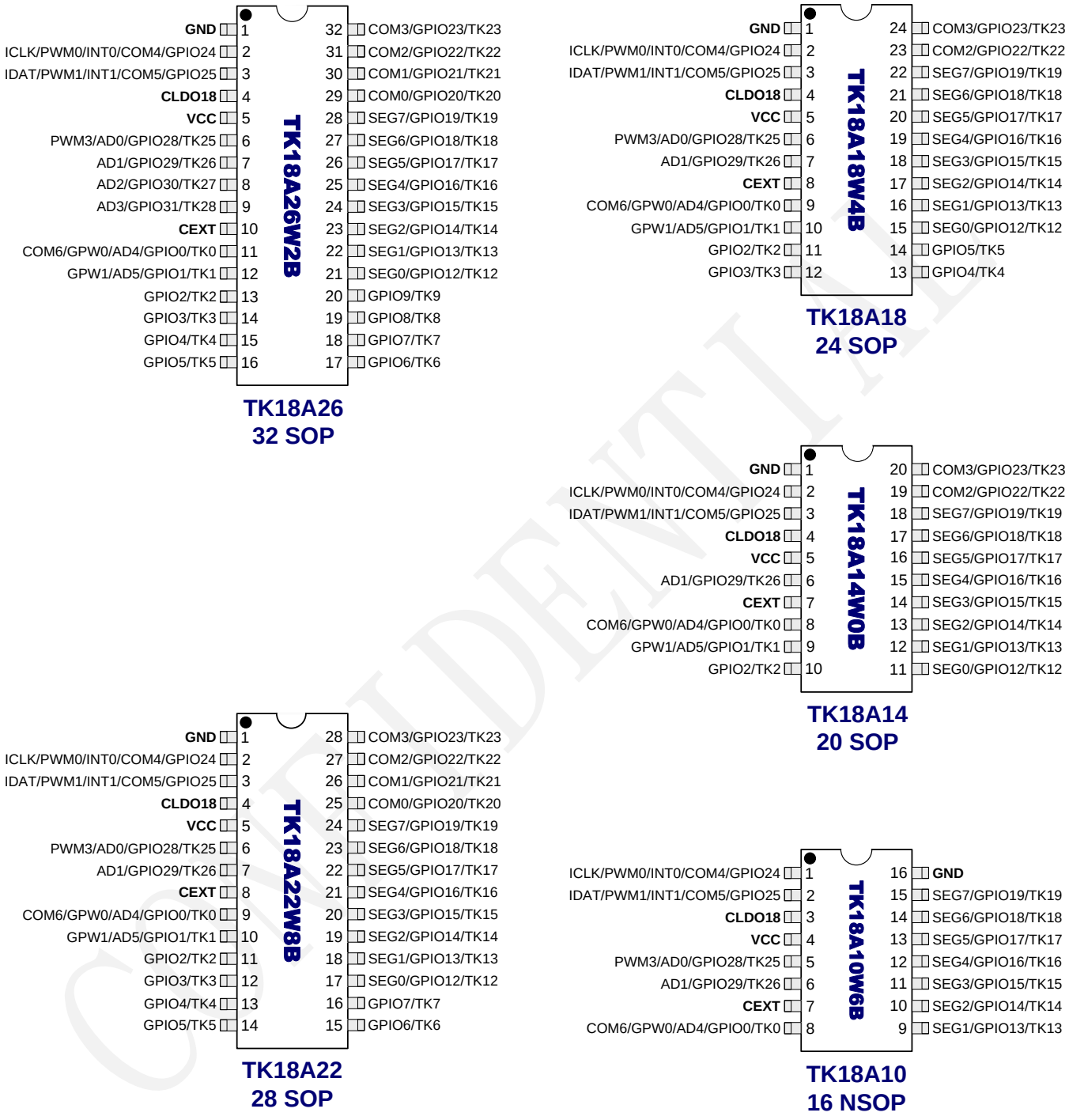


Diagram 1-2 TK18 Pins Package Diagram

Note 1 : Unused pin should be set to I/O mode and output Low.

1.5.2 Reference table for pin package

Pin Name	Pin Number vs. Package Type							
	LQF44	QFN32	SOP32	SOP28	QFN24	SOP24	SOP20	NSOP16
GND	5	6	1	1	5	1	1	16
ICLK/PWM0/INT0/COM4/GPIO24	6	7	2	2	6	2	2	1
IDAT/PWM1/INT1/COM5/GPIO25	7	8	3	3	7	3	3	2
CLDO18	8	9	4	4	8	4	4	3
VCC	9	10	5	5	9	5	5	4
PWM2/GPIO26	10							
NC	11							
PWM3/GPIO27	12							
PWM3/AD0/GPIO28/TK25	13	11	6	6	10	6		5
TXD/SCL/GPW2/GPIO32	14							
RXD/SDA/GPW3/GPIO33	15							
AD1/GPIO29/TK26	16	12	7	7	11	7	6	6
COM6/GPIO34	17							
GPIO35	18							
AD2/GPIO30/TK27	19		8					
AD3/GPIO31/TK28	20		9					
CEXT	21	13	10	8	12	8	7	7
GND	22							
COM6/GPW0/AD4/GPIO0/TK0	23	14	11	9	13	9	8	8
GPW1/AD5/GPIO1/TK1	24	15	12	10	14	10	9	
GPIO2/TK2	25	16	13	11	15	11	10	
GPIO3/TK3	26	17	14	12	16	12		
GPIO4/TK4	27	18	15	13	17	13		
GPIO5/TK5	28	19	16	14	18	14		
GPIO6/TK6	29	20	17	15				
GPIO7/TK7	30	21	18	16				
GPIO8/TK8	31	22	19					
GPIO9/TK9	32	23	20					
NC	33							
GPIO10/TK10	34	24						
GPIO11/TK11	35	25						
SEG0/GPIO12/TK12	36	26	21	17	19	15	11	
SEG1/GPIO13/TK13	37	27	22	18	20	16	12	9
SEG2/GPIO14/TK14	38	28	23	19	21	17	13	10

(Continuance 1)

Pin Name	Pin Number vs. Package Type							
	LQF44	QFN32	SOP32	SOP28	QFN24	SOP24	SOP20	NSOP16
SEG3/GPIO15/TK15	39	29	24	20	22	18	14	11
SEG4/GPIO16/TK16	40	30	25	21	23	19	15	12
SEG5/GPIO17/TK17	41	31	26	22	24	20	16	13
SEG6/GPIO18/TK18	42	32	27	23	1	21	17	14
SEG7/GPIO19/TK19	43	1	28	24	2	22	18	15
NC	44							
COM0/GPIO20/TK20	1	2	29	25				
COM1/GPIO21/TK21	2	3	30	26				
COM2/GPIO22/TK22	3	4	31	27	3	23	19	
COM3/GPIO23/TK23	4	5	32	28	4	24	20	

Table 1-2 Reference Table for Pin Package

1.5.3 Pin functional summary

Pin Name	Pin multiplexing	Types	Reset state	Functional summary	Note
GND	GND	P	-	Ground, reference point for Chip 0V	
ICLK/PWM0/INT0/COM4/GPIO24	ICLK	I	I	Clock pin, used to connect with X-ISP tools	Note 1
	PWM0	O	-	8 bytes PWM Channel output 0	
	INT0	I	-	External interrupt input 0	
	COM4	O	-	LED COM Channel output 4	
	GPIO24	I/O	-	Input/output channel 24	
IDAT/PWM1/INT1/COM5/GPIO25	IDAT	I/O	I	Data pin, used to connect with X-ISP tools	Note 1
	PWM1	O	-	8 bytes PWM Channel output 1	
	INT1	I	-	External interrupt input 1	
	COM5	O	-	LED COM channel output 5	
	GPIO25	I/O	-	Input/output channel 25	
CLDO18	CLDO18	P	-	Regulator capacitor for internal 1.8V power	Note 2
VCC	VCC	P	-	Chip power (2.7V-5.5V)	
PWM2/GPIO26	PWM2	O	-	8 bytes channel output 2	
	GPIO26	I/O	HiZ	Input/output channel 26	
PWM3/GPIO27	PWM3	O	-	8 bytes PWM channel output 3	Note 3
	GPIO27	I/O	HiZ	Input/output channel 27	
PWM3/AD0/GPIO28/TK25	PWM3	O	-	8 bytes PWM channel output 3	Note 3
	AD0	I	-	ADC simulated channel input 0	
	GPIO28	I/O	HiZ	Input/output channel 28	
	TK25	A	-	Touch key channel 25	

(Continuance 1)

Pin Name	Pin multiplexing	Types	Reset state	Functional summary	Note
TXD/SCL/GPW2 /GPIO32	TXD	O	-	UART ports communication data output	Note 4
	SCL	I	-	I^2C bus clock input	Note 4
	GPW2	I	-	External wake-up interrupt input 2	
	GPIO32	I/O	HiZ	Input/output channel 32	
RXD/SDA/GPW3 /GPIO33	RXD	I	-	UART ports communication data input	Note 4
	SDA	I/O	-	I^2C bus data output/input	Note 4
	GPW3	I	-	External wake-up interrupt input 3	
	GPIO33	I/O	HiZ	Input/output channel 33	
AD1/GPIO29/TK26	AD1	I	-	ADC simulated channel input 1	
	GPIO29	I/O	HiZ	Input/output channel 29	
	TK26	A	-	Touch key channel 26	
COM6/GPIO34	COM6	O	-	LED COM channel output 6	Note 5
	GPIO34	I/O	HiZ	Input/output channel 34	
GPIO35	GPIO35	I/O	HiZ	Input/output channel 35	
AD2/GPIO30/TK27	AD2	I	-	ADC simulated input 2	
	GPIO30	I/O	HiZ	Input/output channel 30	
	TK27	A	-	Touch key channel 27	
AD3/GPIO31/TK28	AD3	I	-	ADC simulated channel input 3	
	GPIO31	I/O	HiZ	Input/output channel 31	
	TK28	A	-	Touch key channel 28	
CEXT	CEXT	A	HiZ	Touch key reference capacitance input	Note 6
COM6/GPW0/AD4 /GPIO0/TK0	COM6	O	-	LED COM channel output 6	Note 5
	GPW0	I	-	External wake-up interrupt input 0	
	AD4	I	-	ADC simulated channel input 4	
	GPIO0	I/O	HiZ	Input/output channel 0	
	TK0	A	-	Touch key channel 0	
GPW1/AD5/GPIO1/TK1	GPW1	I	-	External wake-up interrupt input 1	
	AD5	I	-	ADC simulated channel input 5	
	GPIO1	I/O	HiZ	Input/output channel 1	
	TK1	A	-	Touch key channel 1	
GPIO2/TK2	GPIO2	I/O	HiZ	Input/output channel 2	
	TK2	A	-	Touch key channel 2	
GPIO3/TK3	GPIO3	I/O	HiZ	Input/output channel 3	
	TK3	A	-	Touch key channel 3	

(Continuance 2)

Pin Name	Pin multiplexing	Types	Reset state	Functional summary	Note
GPIO4/TK4	GPIO4	I/O	HiZ	Input/output channel 4	
	TK4	A	-	Touch key channel 4	
GPIO5/TK5	GPIO5	I/O	HiZ	Input/output channel 5	
	TK5	A	-	Touch key channel 5	
GPIO6/TK6	GPIO6	I/O	HiZ	Input/output channel 6	
	TK6	A	-	Touch key channel 6	
GPIO7/TK7	GPIO7	I/O	HiZ	Input/output channel 7	
	TK7	A	-	Touch key channel 7	
GPIO8/TK8	GPIO8	I/O	HiZ	Input/output channel 8	
	TK8	A	-	Touch key channel 8	
GPIO9/TK9	GPIO9	I/O	HiZ	Input/output channel 9	
	TK9	A	-	Touch key channel 9	
GPIO10/TK10	GPIO10	I/O	HiZ	Input/output channel 10	
	TK10	A	-	Touch key channel 10	
GPIO11/TK11	GPIO11	I/O	HiZ	Input/output channel 11	
	TK11	A	-	Touch key channel 11	
SEG0/GPIO12/TK12	SEG0	O	-	LED SEG channel output 0	
	GPIO12	I/O	HiZ	Input/output channel 12	
	TK12	A	-	Touch key channel 12	
SEG1/GPIO13/TK13	SEG1	O	-	LED SEG channel output 1	
	GPIO13	I/O	HiZ	Input/output channel 13	
	TK13	A	-	Touch key channel 13	
SEG2/GPIO14/TK14	SEG2	O	-	LED SEG channel output 2	
	GPIO14	I/O	HiZ	Input/output channel 14	
	TK14	A	-	Touch key channel 14	
SEG3/GPIO15/TK15	SEG3	O	-	LED SEG channel output 3	
		I/O	HiZ	Input/output channel 15	
	TK15	A	-	Touch key channel 15	
SEG4/GPIO16/TK16	SEG4	O	-	LED SEG channel output 4	
	GPIO15	I/O	HiZ	Input/output channel 16	
	TK15	A	-	Touch key channel 16	
SEG5/GPIO17/TK17	SEG5	O	-	LED SEG channel output 5	
	GPIO16	I/O	HiZ	Input/output channel 17	
	TK16	A	-	Touch key channel 17	

(Continuance 3)

Pin Name	Pin multiplexing	Types	Reset state	Functional summary	Note
SEG6/GPIO18/TK18	SEG6	O	-	LED SEG channel output 6	
	GPIO18	I/O	HiZ	Input/output channel 18	
	TK18	A	-	Touch key channel 18	
SEG7/GPIO19/TK19	SEG7	O	-	LED SEG channel output 7	
	GPIO19	I/O	HiZ	Input/output channel 19	
	TK19	A	-	Touch key channel 19	
COM0/GPIO20/TK20	COM0	O	-	LED SEG channel output 0	
	GPIO20	I/O	HiZ	Input/output channel 20	
	TK20	A	-	Touch key channel 20	
COM1/GPIO21/TK21	COM1	O	-	LED COM channel output 1	
	GPIO21	I/O	HiZ	Input/output channel 21	
	TK21	A	-	Touch key channel 21	
COM2/GPIO22/TK22	COM2	O	-	LED COM channel output 2	
	GPIO22	I/O	HiZ	Input/output channel 22	
	TK22	A	-	Touch key channel 22	
COM3/GPIO23/TK23	COM3	O	-	LED COM channel output 3	
	GPIO23	I/O	HiZ	Input/output channel 23	
	TK23	A	-	Touch key channel 23	

Table 1-3 Pin Functional Summary

Note 1: ICLK and IDAT (default pull-up is 4.7KΩ) are communication interface used to connected with ene X-ISP debugging tools, through which pin functions can be mapped to and realized at any GPIO port by setting register so as to flexibly meet the user's actual requirements (Refer to ISPCLK MUX and ISPDAT MUX registers for instructions).

Note 2: Pin CLDO 18 is set for the regulator capacitor of internal 1.8V power, which is supposed to externally connect with 2.2-4.7μF earth capacitor.

Note 3: Since packages below LQFP44 will not include any pin for PWM3/GPIO27, if there is any need to realize PWM3 function, pins for PWM3/AD0/GPIO28/TK25 can be applied. Refer to MAC_OPT Register in Chapter 11: PWM for detailed operating instructions.

Note 4: Although packages below LQFP44 will not include pins for TXD, RXD, SCL, SDA, the user still can map the pin function to any GPIO port by setting the register. (Refer to TXDMUX, RXDMUX, I2CCLK_MUX and I2CDAT_MUX registers for details.)

Note 5: Since packages below LQFP44 will not include any pin for COM6/GPIO34, if there is any need to realize COM6 function, pins for COM6/GPW0/AD4/GPIO0/TK0 can be applied. Refer to LEDCOMEN Register in Chapter 13: LED Driver Module for detailed operating instructions.

Note 6: CEXT is the reference capacitance input pin for touch keys, which needs to be externally connected to 3.9nF earth capacitor (this capacitor shall be made of 10% high accuracy NPO or X7R materials).

Note 7: I/O=Input/Output, O=Output, I=Input, P=Power, A=Analog, HiZ=High impedance.

2. MCU Core

2.1 Overview

TK18 is a touch-key MCU specially designed by ene. It still adopts 8501 standard core, which is the most popular on the market, and can perfectly support instructions from standard 8051. Related register system diagram of TK18 core is as follows:

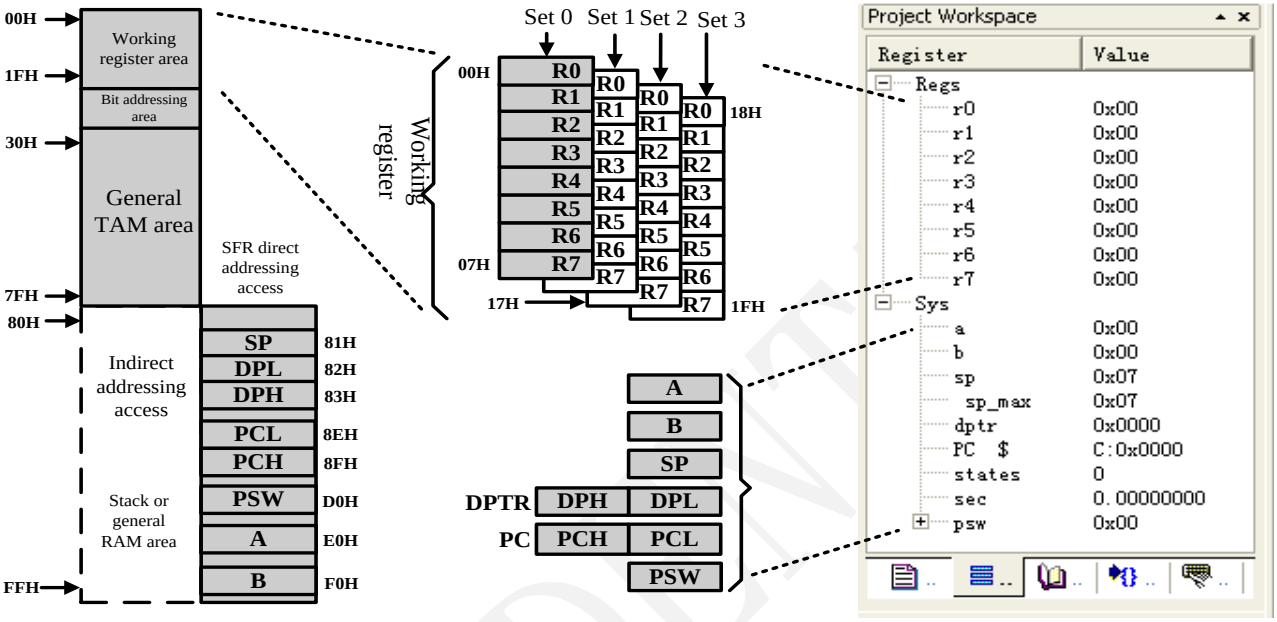


Diagram 2-1 Core Register System Diagram

2.2 Arithmetic Unit

2.2.1 ALU (Arithmetic Logic Unit)

ALU is composed of adder and other logic electric circuits, which are used to conduct four arithmetic and logic operations, and shifting function and bit operation. The status information of operational results is sent to the status register (PSW).

2.2.2 ACC (Accumulator)

ACC is a 8 byte register (A for short), connected to ALU through register. It is the most frequently used register when CPU executes demands, where operands or intermediate results are stored.

2.2.3 Register B

It is used to store upper 8 bytes of multiplier/product in multiplication, and divisor/remainder in division.

2.2.4 PSW (Program Status Word)

PSW is a special 8-bit register, used to store various program status information in process of program operation. It can conduct bit addressing. PSW bit are defined as follows: (if reset, PSW=00H)

PSW (D0H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Flag	CY	AC	F0	RS1	RS0	OV	---	P

Bit7 **CY**: Carry
In addition or subtraction operation, if the top bit of product carries or borrows, CY will be set at 1 in hardware, otherwise, 0.

Bit6 **AC**: Auxiliary carry (half carry)
In addition or subtraction operation, lower 4 bit carry to or borrow from upper 4 bit, this bit will be set at 1 in hardware, otherwise, 0.

Bit5 **F0**: User
Set or reset by usert. It can be used as a status flag defined by user.

Bit4-3 **RS1-RS0**: Working register set pointer, used to select register set for the current work of CPU.
00: Select Set 0 R0-R7 working register: 00H~07H
01: Select Set 1 R0-R7 working register: 08H~0FH
10: Select Set 2 R0-R7 working register: 10H~17H
11: Select Set 3 R0-R7 working register: 18H~1FH

Bit2 **OV**: Overflow
In arithmetic operations, in case of any overflow, OV bit will be set at 1 in hardware; otherwise, 0.

Bit0 **P**: Parity
This bit will from beginning to end track the parity of 1 in the content of ACC A. If there is an odd number of 1 in the content of ACC A, P will be set at 1; otherwise, 0. Any change of instruction to the content of ACC A will change the flag of P.

2.3 Controller

2.3.1 PC (Program Counter)

PC is byte address counter of program memory, the content of which is the address of the next instruction that is to be executed, and its addressing range is up to 64KB. It is also able to automatically add 1 so as to realise the sequential execution of program. It is possible to change its content through instructions such as transfer, invocation, and return to realize program transfer (if reset, PC=0000H).

PC includes 16 bit, among which=> PCL (8EH): PC lower 8 bit
PCH (8FH): PC upper 8 bit

2.3.2 Instruction register (IR) and instruction decoder (ID)

Instruction register (IR): Used to temporarily store instructions that are waiting to be executed and decoded. Instruction decoder (ID): Used to decode instructions in the instruction register, that is to convert instructions to needed level signals.

2.3.3 Data Pointer (DPTR)

DPTR is a 16-bit register. It is used to store 16-bit addresses, which are used in accessing external program memory and external data memory. In programming, DPTR can be used as both 16-bit register and 2×8-bit register separately, that is:

DPL (82H): DPTR lower 8 bit

DPH (83H): DPTR upper 8 bit

2.3.4 SP (Stack Pointer)

<Concept>

Stack is a special memory area in RAM for particular purposes (which can be accessed through only one end).

<Structure>

One end has a permanent address, that is the stack bottom; while the address of the other end is dynamic, that is the stack top.

<Accessing principle>

First in, last out, that is, data pushed on first will be pushed down last.

<Operating methods>

There two operating methods: data push and pop operation.

Both push and pop are operated on the top of the stack so that data must be accessed in the method of "first in, last out", and "last in, first out".

<Application>

1. Automatic stack application by CPU: CPU will automatically push return address on stack in the invocation of sub program or response interrupt as well as in the treatment of interrupt service program; stack can also be used to transfer parameters.
2. Stack application by programmer: stack can be used for temporary data storage.

<Stack pointer (SP)>

It is both the address of the top of stack, that is, SP points to the top of stack and the indirect addressing register for accessing the stack, which can automatically add or subtract 1. When data is pushed on stack, SP will aad 1 at first, and then CPU will memory data; when data is poped down stack, CPU will send out date at first, and then SP will automatically subtract 1. Since the value of SP increases when data is pushed on, that is, the stack grows in the direction of upper address as well as the stack top is effective data, this stack is full ascending (if reset, SP=07H).

Note: In the application of stack, the address of SP cannot be overlapped with that of data memory so as to prevent program from running out of track.

3. Memory

3.1 Overview

TK18 MCU includes two parts, "Process ROM" and "Data RAM". Process ROM has 32 bytes flash (including 128 bytes EEPROM realized through flash); Data RAM has 256 bytes of MCS-52 IRAM, 128 bytes SFR, 1K bytes XRAM and TK18 REG. Please see below for TK18 memory block diagram.

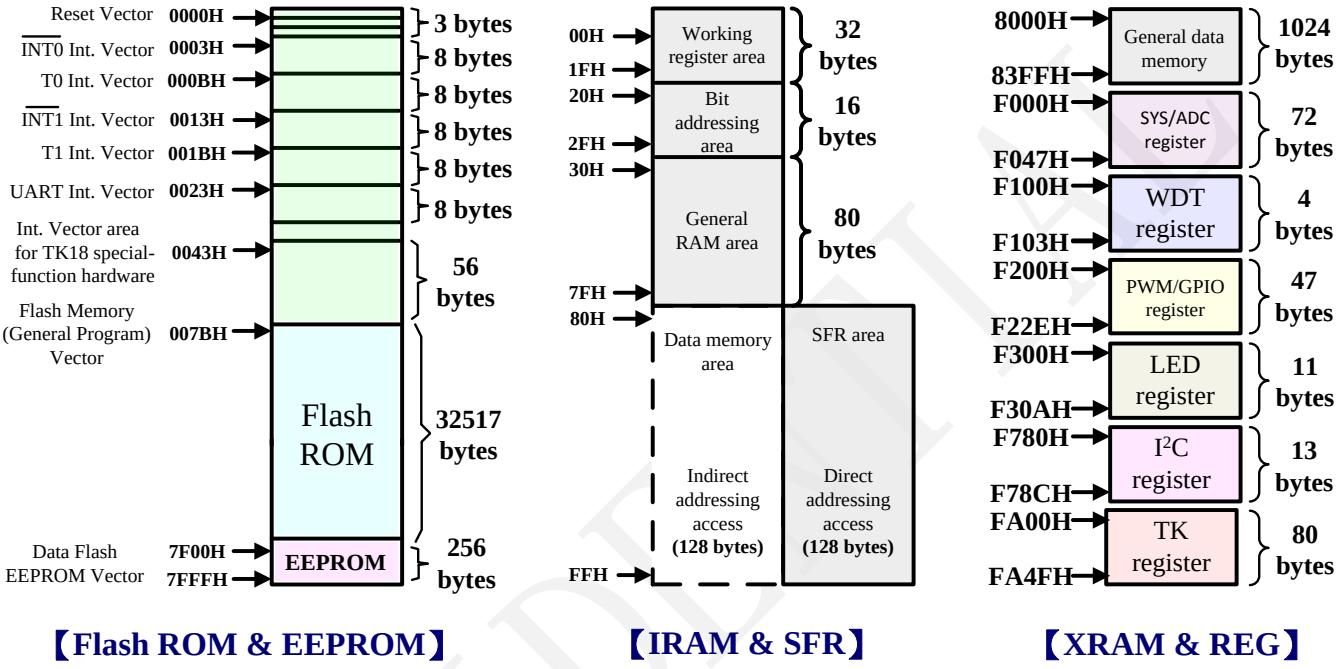


Diagram 3-1: TK18 Memory Block Diagram

3.2 ROM

3.2.1 Flash ROM

TK18 provides 32K bytes flash (0000H-7FFFH). The memory is mainly used for fixed procedure and data (parameter table etc) storage, and also maintains the reset and interrupt address for operation codes.

3.2.2 Data Flash EEPROM

TK18 program flash applies the latest flash technique so that user may control the program to achieve 128-byte EEPROM (7F00H -7FFFH, where the lower 128-byte is for EEPROM data storage and the upper 128-byte is for EEPROM management control). This function should be enable by ene F/W library (X-LIB) if needed (otherwise, this memory spaces (7F00H-7FFFH) keeps the normal flash memory functionary). Please refer to ene X-LIB user guide for detail information.

3.3 RAM

3.3.1 IRAM

TK18 IRAM is compatible with MCS-52 and provides total 256 bytes (00H-FFH) space with related address introduction as follows: (refer to Diagram 3-2)):

◇ 00H～7FH (0～127): Lower 128-byte RAM area, it may be accessed by direct or indirect address mapping method, where

00H～1FH: Working registers, which can be controlled by RS1/RS0 bits in PSW.

20H～2FH: General purpose RAM. Total 128 bits available, and may be used as bit addressing area.

30H～7FH: It can be used as general purpose RAM or stack.

◇ 80H～FFH (128～256): Upper 128-byte RAM area, it can be accessed only by indirect address mapping method. It can be used as general purpose RAM or stack.

◇ 80H～FFH (128～256): Upper 128-byte is for SFR area (this address is the same as general purpose RAM area), and can be accessed only by direct address mapping method.

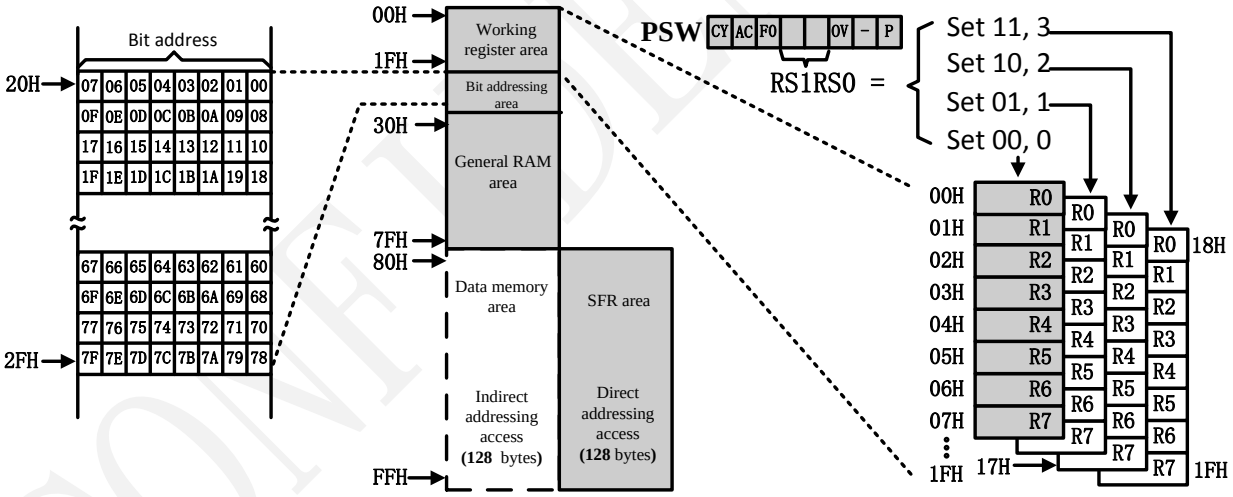


Diagram 3-2: TK18 Internal IRAM Block Diagram

3.3.2 External XRAM

TK18 provides external data memory (XRAM) with total 1024 bytes (8000H-83FFH). It is for temporary data input/output and the intermediate calculation result.

Note: When TK18 is powered, it enters power-on reset state and the XRAM is disable during this period. XRAM can only be initiated and function normally till PCON2.4 XRAMEN is set to "1".

3.4 Function Register (REG)

3.4.1 SFR

TK18 special function register (SFR, 80h-FFh) includes not only standard 8501, but also some additional redefined SFR to control the external modules (timer/counter, UART and interrupts etc). See the following Table 3-1 for TK18 SFR registers.

Address	Name	Description	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
80h	P0IE	Port 0 interrupt enable register	---	I2CRSI	I2CI	ADCI	LVDI	WDTI	GPWI	TKI	00h
81h	SP	Stack pointer	SP[7: 0]								07h
82h	DPL	DPTR lower byte	DPL[7: 0]								00h
83h	DPH	DPTR upper byte	DPH[7: 0]								00h
86h	PCON2	Processor control register 2	---	---	---	XRAMEN	---	---	TIMCLK	---	20h
87h	PCON	Processor control register	---	---	---	---	---	---	PWD	---	00h
88h	TCON	Timer/counter control register	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
89h	TMOD	Timer/counter mode register	GATE1	CT1	TM1		GATE0	CT0	TM0		00h
8Ah	TL0	Timer 0 lower byte	TL0[7: 0]								00h
8Bh	TL1	Timer 1 lower byte	TL1[7: 0]								00h
8Ch	TH0	Timer 0 upper byte	TH0[7: 0]								00h
8Dh	TH1	Timer 1 upper byte	TH1[7: 0]								00h
8Eh	PCL	Program counter lower byte	PCL[7: 0]								00h
8Fh	PCH	Program counter upper byte	PCH[7: 0]								00h
98h	SCON	Serial port UART control register	SM1	SM0	-	REN	TB8	RB8	TI	RI	50h
99h	SBUF	Serial port data buffer	SBUF[7: 0]								00h
9Ah	SCON2	Serial port control register 2	SCON2[7: 0]								00h
9Bh	SCON3	Serial port control register 3	SCON3[7: 0]								89h
9Ch	SCON4	Serial port mode 0 Baud-rate control register	SCON4[7: 0]								00h
A0h	P2	Port 2 latch register	P2[7: 0]								00h
A8h	IE	Interrupt enable register	EA	---	---	ES	ET1	EX1	ET0	EX0	00h
B8h	IP	Interrupt enable register	---	---	---	PS	PT1	PX1	PT0	PX0	00h
D0h	PSW	Program status word	CY	AC	F0	RS1	RS0	OV	---	P	00h
D8h	P0IF	Port 0 interrupt flag	---	I2CRSIF	I2CIF	ADCIF	LVDIF	WDTIF	GPWIF	TKIF	00h
E0h	ACC	Accumulator	ACC[7: 0]								00h
F0h	B	Register B	B[7: 0]								00h

Table 3-1: TK18 SFR Registers Table

Note: Registers on the orange ground colour in Table 3-1 represent redefined TK18 registers, which are not included in standard 8051 SFR.

3.4.2 External module function register

Beside original external modules included in 8501 standard core, TK18 also provides powerful external modules. By configuring related register, user is able to initiate the module function. Table 3-2 outlines the external module registers: (Please refer to related chapters for details)

Module	Register description	Address	Bytes
SYS/ADC	System related and ADC	F000H-F047H	72
WDT	Watchdog timer module register	F100H~F102H	3
PWM/GPIO	PWM/GPIO module registers	F200H-F22EH	47
LED	LED driver module registers	F300H-F30AH	11
I^2C slave	I^2C slave module registers	F780H-F78CH	13
TK	Touch key module registers	FA00H-FA4FH	80

Table 3-2: TK18 External Function Registers Description Table

Note: When TK18 is powered and enters power-on reset state, TK18 "XRAM" and "the external module REG" are disable. To enable XRAM and the external module REG, configure PCON2.4 XRAMEN as "1". Therefore, user needs to set XRAMEN as "1" immediately after the user's program enters power-on reset state. Details of PCON2 in SFR are as follows:

PCON2 (86H) Register

Byte number	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	XRAMEN	---	---	TIMCLK	---
Read/write	---	---	---	R/W	---	---	R/W	---
Default	0	0	0	0	0	0	0	0

bit7-5 Reserved

bit4 **XRAMEN**: "XRAM" and "External REG"

When TK18 is powered and enters power-on reset state, user needs to immediately set XRAMEN to "1" before TK18 "XRAM" and " the external module REG " can function normally.

0: disable, TK18 XRAM & REG (default)

1: enable, TK18 XRAM & REG

bit3-2 Reserved

bit0 Reserved

Note: When accessing different procedure or data RAM, different commands are required:

Access ROM: use MOVC command,

Access IRAM and SFR, use MOV command,

Access XRAM and TK18 REG, use MOVX command.

4. Oscillator

4.1 Overview

TK18 applies 2 internal RC oscillators as clock source for core operation, which are HIRC and LIRC. Whenever TK 18 is powered, HIRC and LIRC will operate the same time as chip operates. Then, TK18 will operate normally. Detailed description of RC oscillators is as follows.

4.2 Internal HIRC

The internal HIRC of TK18 oscillates at a permanent frequency of 28MHz. This high frequency (F_{HOSC}) provides Flash Controller and System Frequency (F_{SYS}) with clock source. Instructions for use and block diagram of HIRC are as follows:

◇ Flash controller: TK18 flash includes a highly efficient controller, while F_{HOSC} directly provides high-speed clock source.

◇ F_{SYS}: TK18 core operation mainly depends upon F_{SYS}. F_{HOSC} produces 2 clock sources of $F_{HOSC}/4$ and $F_{HOSC}/2$ through Second-order Frequency divider. And then the final F_{SYS} is decided upon through the selection of SYSCLK register.

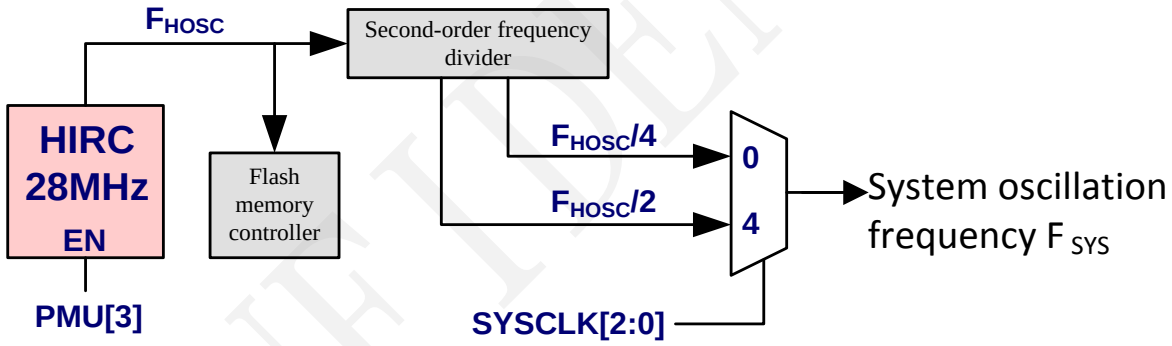


Diagram 4-1 Internal HIRC Block Diagram

4.3 Internal LIRC

The internal LIRC of TK18 oscillates at a permanent frequency of 32KHz. This low frequency (F_{LOSC}) mainly provides Watchdog Timer Frequency (F_{WDT}) with clock source. The block diagram of LIRC is as follows:

Diagram 4-2: Internal LIRC Block Diagram

4.4 Normal System Operational Mode

4.4.1 System Oscillating Frequency

The system frequency (F_{SYS}) is decided upon by SYSCLK register through selecting between $F_{HOSC}/4$ and $F_{HOSC}/2$, which are produced from F_{HOSC} by the second-order frequency divider. The description of SYSCLK register is as follows:

SYSCLK (F009H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	SCLK2	SCLK1	SCLK0
Read/write	---	---	---	---	---	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 3 Reserved

bit2 – 0 **SCLK2-SCLK0**: System clock F_{SYS} selection (initial value F_{SYS} = 7MHz)

000: $F_{HOSC}/4$ (F_{SYS} = 28MHz/4 = 7MHz)

100: $F_{HOSC}/2$ (F_{SYS} = 28MHz/2 = 14MHz)

Others: Reserved

4.4.2 Instruction Cycle and Time

TK18 core fully support 8051 instructions. The clock source for instructions comes from F_{SYS}. The instruction cycle is 2T ($2/F_{SYS}$). TK18 single instruction cycle will be illustrated in the eference:

◇ Assumed F_{SYS} = 14MHz

then, single instruction cycle = 1/[(14MHz/2)]= 0.14285μS

4.5 System Sleep Mode

In order to reduce the power consumption of TK18, PMU register can be used to operate TK18 in the Sleep Mode. In the sleep mode, only HIRC, LIRC, WDT and GPW modules are still operating, while other external function module and PC are out of service. An illustration of PMU register is as follows:

PMU (F000H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	SLPRST	---	---	---	SLPHF	ENTSLP	WAKWDT	WAKGPW
Read/write	R/W	---	---	---	R/W	-/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

bit7 **SLPRST**: Chip reset upon being waked up from sleep mode

0: Upon being waked up from sleep mode, PC will execute the next instruction address of ENTSLP.

1: Upon being waked up from sleep mode, chip will immediately reset while PC will execute from the reset entry address 0000H.

bit6 – 4 Reserved

bit3 **SLPHF**: Sleep-mode HIRC operating

0: HIRC stops operating in sleep mode.

1: HIRC continues to operating in sleep mode.

Bit2 **ENTSLP**: Enter sleep mode.

If this bit is set at "1", then enter sleep mode.

Bit1 **WAKWDT**: Wakes up the system from sleep mode through watchdog timer overflow.

0: Disable

1: Enable

Bit0 **WAKPGW**: Wake up the system from sleep mode through external wake-up interrupt GPW port

0: Disable

1: Enable

4.5.1 Enter sleep mode

TK18 will enter sleep mode after PMU.2 ENTSLP bit is set to "1". However, since HIRC is operating while the system is in operational mode, PMU.3 SLPHF bit has to be set to "0" to stop HIRC from operating before the system enters sleep mode so as to realize a minimum power consumption in sleep mode.

4.5.2 Wake up from sleep mode theough WDT overflow

If WDT overflow is eferen to wake up the system from sleep mode, PMU.1 WAKWDT bit should be set to "1" before the system enters sleep mode. Otherwise, set WAKWDT bit to "0".

4.5.3 Wake up from sleep mode through external wake-up interrupt GPW port

If external wake-up interrupt GPW port is applied to wake up the system from sleep mode, PMU.0 WAKGPW bit should be set to "1" before the system enters sleep mode. Otherwise, please set WAKGPW bit to "0".

Note: Whether being waked up from sleep mode through WDT or external wake-up interrupt GPW, user should make sure PMU.7 SLPRST bit is set up so that PC will continue to work with necessary wake-up address.

5. Reset

5.1 Overview

TK18 provides RESET modules. Since whether reset condition qualifies or not, it is completely decided upon by the embedded module, external pin is not needed to lead in signal (TK18 doesn't provide any RESET pin). Whenever either of the following two conditions qualifies, TK18 will reset, after which all internal registers will be reset to initial status.

◇ Power-on-Reset (POR)

Following reset→ IRAM, XRAM values are eference ce; registers are restored to initial values; flash remains the same.

◇ WDT overflow reset

Following reset→ IRAM, XRAM, registers and flash all remain the same.

Note: When POR is finished, data RAM values are unknown so that users need to initialize in the program on their own.

6. Interrupt

6.1 Overview

TK18 provides 12 interrupt sources (Table 6-1). Other than the 5 interrupt sources from standard 8051, TK18 provides additional 7 interrupt sources for external modules only. These 7 interrupt sources have their own control registers for enable and flag control. Only 5 interrupt sources from standard 8051 can set priorities. The rest 7 interrupts do not support priority function. Moreover, TK18 only supports one level priority interrupt without nest interrupting function. That means the on-going interrupt procedure will not be interfered by other interrupts till RETI command is executed. Please refer to the following Diagram 6-1.

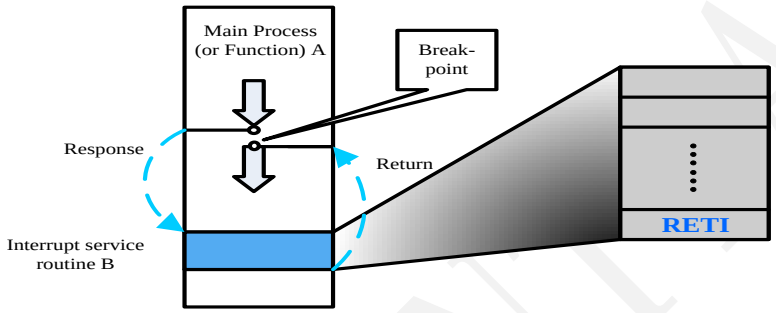


Diagram 6-1: Standard Interrupt Block Diagram without Nest Interrupting Function

Interrupt Source	Entry Vector Address	Hardware Module Interrupt Control	Hardware Module Interrupt Flag	Interrupt Control	Interrupt Flag	Interrupt description	Priority
INT0	0003H			EX0	IE0	External interrupt 0	Highest
T0	000BH			ET0	TF0	Timer 0 interrupt	
INT1	0013H			EX1	IE1	External interrupt 1	
T1	001BH			ET1	TF1	Timer 1 interrupt	
TXD/RXD	0023H			ES	RI / TI	UART interrupt	
TK	0043H	TKMI	TKMIF	TKI	TKIF	TK interrupt	
GPW0	004BH	GPW0MI	GPW0MIF	GPWI	GPWIF	GPW0 external wakeup call interrupt	
GPW1		GPW1MI	GPW1MIF			GPW1 external wakeup call interrupt	
GPW2		GPW2MI	GPW2MIF			GPW2 external wakeup call interrupt	
GPW3		GPW3MI	GPW3MIF			GPW3 external wakeup call interrupt	
WDT	0053H	WDTHI	WDTHI	WDTI	WDTIF	Watchdog timer interrupt	
LVD	005BH	LVDMI	LVDMIF	LVDI	LVDIF	Low voltage interrupt	
ADC	0063H	ADCMI	ADCMIF	ADCI	ADCIF	ADC interrupt	
I2C	006BH	I2C_INT REG	I2C_PF REG	I2CI	I2CIF	I2C slave interrupt	
I2C Restart	0073H			I2CRSI	I2CRSIF	I2C slave restart interrupt	Lowest

Table 6-1: TK18 Interrupt Sources Table

6.2 System Block Diagram

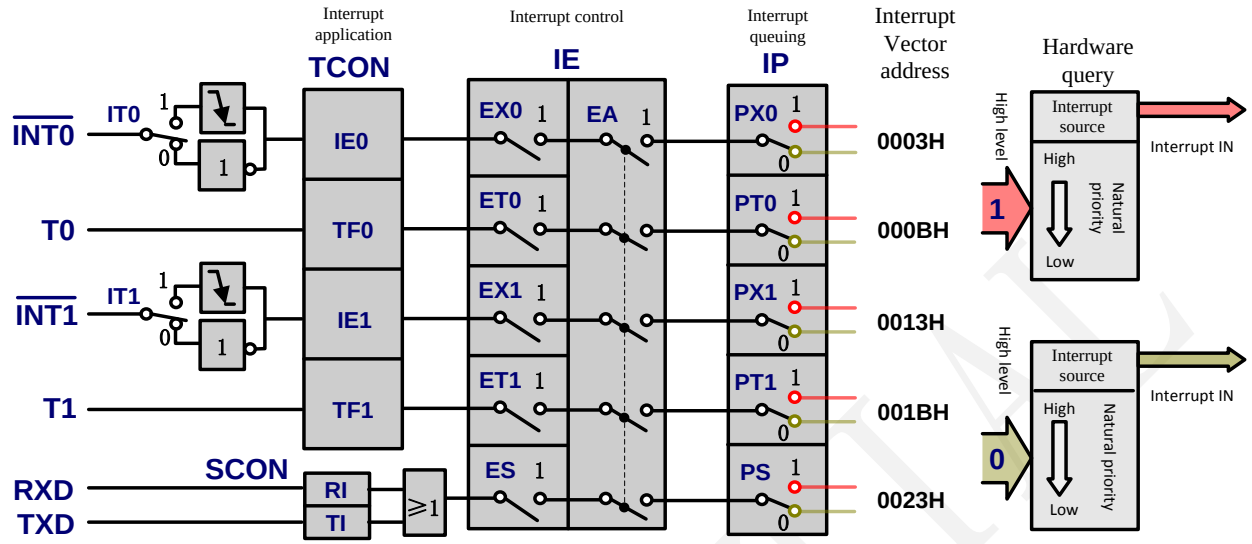


Diagram 6-2: TK18 CPU 8051 Interrupt Block Diagram

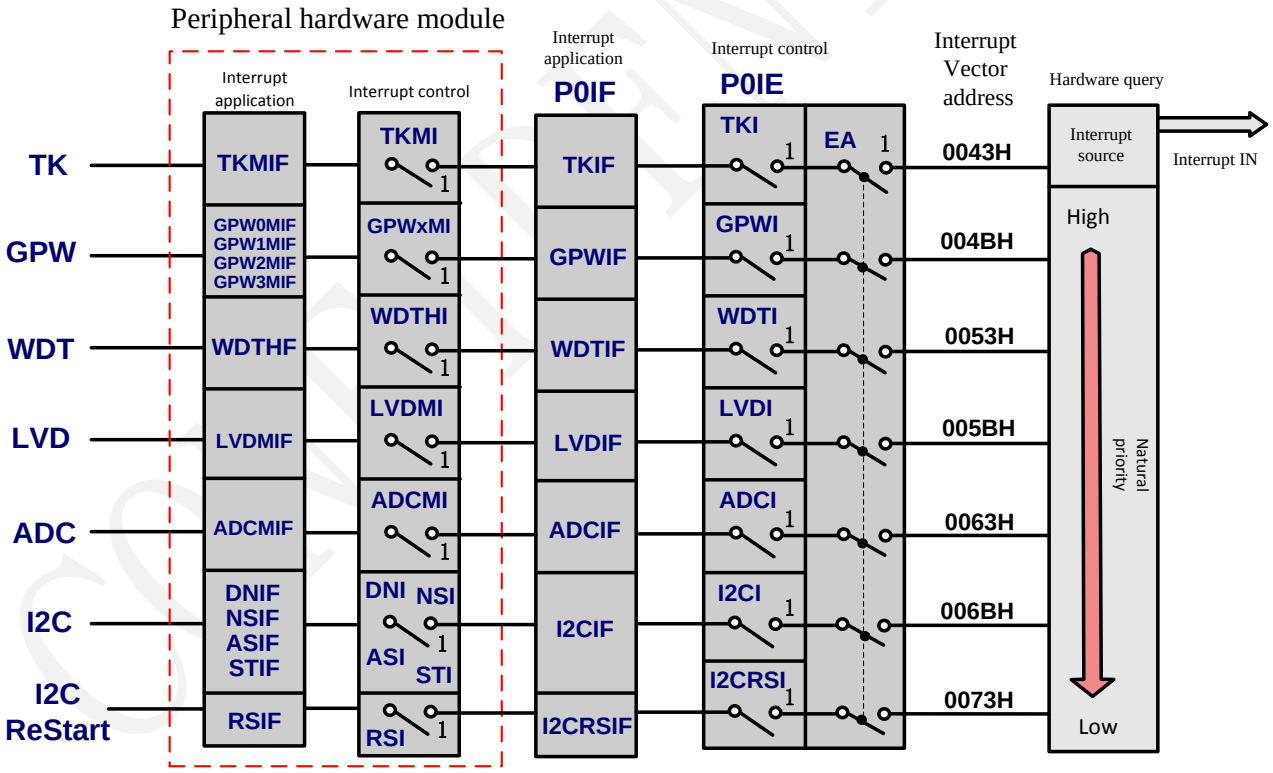


Diagram 6-3: TK18 CPU Interrupt Block Diagram for External Modules

Note: 7 external interrupts of TK18 have its own interrupt control bit and flag respectively. Please make sure to set the interrupt control bit to "1" to make the interrupt function runs normally.

6.3 Related Control Registers

6.3.1 Interrupt enable eferen registers

IE (A8H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	EA	---	---	ES	ET1	EX1	ET0	EX0
Read/write	R/W	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **EA**: Interrupt
0: Disable
1: Enable
bit6 – 5 Reserved
bit4 **ES**: UART interrupt
0: Disable
1: Enable
bit3 **ET1**: Timer 1 (T1) interrupt
0: Disable
1: Enable
bit2 **EX1**: External interrupt 1 (INT1)
0: Disable
1: Enable
bit1 **ET0 :** Timer0 (T0) interrupt
0: Disable
1: Enable
bit0 **EX0**: External interrupt0 (INT0)
0: Disable
1: Enable

IP (B8H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	PS	PT1	PX1	PT0	PX0
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved
bit4 **PS**: UART interrupt priority
bit3 **PT1**: T1 interrupt priority
bit2 **PX1**: INT1 interrupt priority
bit1 **PT0**: T0 interrupt priority
bit0 **PX0**: INT0 interrupt priority

In above configurations, 1 represents “higher priority”; 0 represents “lower priority”.

The natural order on the same priority level is INT0→T0→INT1→T1→Serial port.

P0IE (80H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	I2CRSI	I2CI	ADCI	LVDI	WDTI	GPWI	TKI
Read/write	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 Reserved

bit6 **I2CRSI**: I^2C slave module restart interrupt
0: Disable
1: Enable

bit5 **I2C**: I^2C slave module interrupt
0: Disable
1: Enable

bit4 **ADCI**: ADC0-5 interrupt
0: Disable
1: Enable

bit3 **LVDI**: LVD interrupt
0: Disable
1: Enable

bit2 **WDTI**: WDT interrupt
0: Disable
1: Enable

bit1 **GPWI**: External wakeup call GPW0-3 interrupt
0: Disable
1: Enable

bit0 **TKI**: TK0-28 scan interrupt
0: Disable
1: Enable

INTEN (FA22H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	TKMI
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit0 **TKMI**: TK port scan finish module interrupt
To ensure that TK port Occureds for interrupt on finishing scan and interrupt responds
successfully, both TKI bit and this hardware module interrupt enable bit have to be set to “1” beforehand. Otherwise, interrupt cann’t respond.
0: Disable
1: Enable

GPWUA0 (F230H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	GPW1IP1	GPW1IP0	GPW1TP	**GPW1MI**	GPW0IP1	GPW0IP0	GPW0TP	**GPW0MI**
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit4 **GPW1MI**: GPW1 hardware module interrupt

To ensure that GPW1 port Occureds for interrupt on qualified trigger conditions
and interrupt responds successfully, both GPWI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.
0: Disable
1: Enable

bit0 **GPW0MI**: GPW0 hardware module interrupt

To ensure that GPW0 port Occureds for interrupt on qualified trigger conditions
and interrupt responds successfully, both GPWI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.
0: Disable
1: Enable

GPWUA1 (F231H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	GPW3IP1	GPW3IP0	GPW3TP	**GPW3MI**	GPW2IP1	GPW2IP0	GPW2TP	**GPW2MI**
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit4 **GPW3MI**: GPW3 hardware module interrupt

To ensure that GPW3 port Occureds for interrupt on qualified trigger conditions
and interrupt responds successfully, both GPWI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.
0: Disable
1: Enable

bit0 **GPW2MI**: GPW2 hardware module interrupt

To ensure that GPW2 port Occureds for interrupt on qualified trigger conditions
and interrupt responds successfully, both GPWI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.
0: Disable
1: Enable

WDTCFG (F100H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	WDTEN	---	WDTHI	WDTCL
Read/write	---	---	---	---	R/W	---	R/W	-/W
Default	0	0	0	0	0	0	0	0

bit1 **WDTHI**: WDT module half overflow interrupt

Once this bit is set to "1" and WDT counts to half of WDTVAL, WDTPF.1 half overflow flag bit WDTHF will be set to "1". However, to ensure that WDT Occureds for interrupt on half overflow and interrupt responds successfully, both WDTI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.

0: Disable

1: Enable

LVDCTL (F007H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	LVDEN	---	---	---	LVDMI
Read/write	---	---	---	R/W	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit0 **LVDMI**: LVD hardware module interrupt

To ensure that LVD Occureds for interrupt on detecting low voltage and interrupt responds successfully, both LVDI bit and this hardware module interrupt enable bit have to be set to "1". Otherwise, interrupt cann't respond.

0: Disable

1: Enable

ADC_CTL1 (F035H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	ADWC3	ADWC2	ADWC1	ADWC0	---	ADCOFF	ADCINI	ADCMI
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit0 **ADCMI**: ADC hardware module interrupt

To ensure that ADC Occureds for interrupt on finishing converting operation and interrupt responds successfully, both ADCI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.

0: Disable

1: Enable

I2C_INT (782H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	RSI	STI	ASI	NSI	DNI
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved

bit4 **RSI**: I^2C restart interrupt
0: Disable
1: Enable

bit3 **STI**: I^2C start interrupt
0: Disable
1: Enable

bit2 **ASI**: I^2C abnormal interrupt
0: Disable
1: Enable

bit1 **NSI**: I^2C normal stop
0: Disable
1: Enable

bit0 **DNI**: I^2C data finish interrupt
0: Disable
1: Enable

Note: To ensure that I2C bus Occureds for interrupt in communication and interrupt responds so that procedure can successfully receive and send data, except P0IE.5 (I2CI) and P0IE.6 (I2CRSI), corresponding module interrupt enable bit also has to be set to "1" beforehand. Otherwise, interrupt cann't respond.

6.3.2 Interrupt Occured flag register

TCON (88H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Read/write	R/W	R/W	R/W	R/W	R/-	R/W	R/-	R/W
Default	0	0	0	0	0	0	0	0

bit7 **TF1**: T1 overflow interrupt, this bit will be automatically cleared after response.
0: Not occur
1: Occured

Bit5 **TF0**: T0 overflow interrupt, this bit will be automatically cleared after response.
0: Not occur
1: Occured

bit3 **IE1**: INT1 trigger interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured

bit2 **IT1**: INT1 trigger mode
0: Low level trigger
1: Falling edge

bit1 **IE0**: INT0 trigger interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured
bit0 **IT0**: INT0 trigger mode
0: Low-level trigger
1: Falling edge

SCON (98H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	SM1	SM1	---	REN	TB8	RB8	TI	RI
Read/write	R/W	R/W	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit5 Reserved
bit1 **TI**: Serial port transmitting TXD interrupt
This bit will not be automatically cleared after response only if this bit is set to "1".
0: Not occur
1: Occured
bit0 **RI:** Serial port receiving RXD interrupt
This bit will not be automatically cleared after response only if this bit is set to "1".
0: Not occur
1: Occured

P0IF (D8H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	I2CRSIF	I2CIF	ADCIF	LVDIF	WDTIF	GPWIF	TKIF
Read/write	---	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 Reserved
bit6 **I2CRSIF**: I^2C slave module restart interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured
bit5 **I2CIF**: I^2C slave module interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured
bit4 **ADCIF**: ADC0-5 interrupt, this bit will be automatically cleared after response
0: Disable
1: Enable
bit3 **LVDIF**: LVD interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured

bit2 **WDTIF**: WDT interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured

bit1 **GPWIF**: GPW0-3 interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured

bit0 **TKIF**: TK0-28 scan interrupt, this bit will be automatically cleared after response
0: Not occur
1: Occured

PENDFLAG (FA23H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	TKMIF
Read/write	---	---	---	---	---	---	---	-/W
Default	0	0	0	0	0	0	0	0

bit0 **TKMIF**: TK port scan finish module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

GPWUPF (F232H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	GPW3MIF	GPW2MIF	GPW1MIF	GPW0MIF
Read/write	---	---	---	---	-/W	-/W	-/W	-/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Rserved

bit3 **GPW3MIF**: GPW3 hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

bit2 **GPW2MIF**: GPW2 hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

bit1 **GPW1MIF**: GPW1 hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

bit0 **GPW0MIF**: GPW0 hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

WDTPF (F101H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	WDTHF	WDTOF
Read/write	---	---	---	---	---	---	-/W	-/W
Default	0	0	0	0	0	0	0	0

bit1 **WDTHF**: WDT module half overflow interrupt. Once this bit is set to "1", it can be cleared.

0: Not overflow

1: Overflow

LVDSTA (F008H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	LVDSTS	---	---	---	LVDMIF
Read/write	---	---	---	R/W	---	---	---	-/W
Default	0	0	0	0	0	0	0	0

bit0 **LVDMIF**: LVD hardware module interrupt. Once this bit is set to "1", it can be cleared.

0: Not trigger (VCC > LVD threshold value, low voltage not detected!)

1: Trigger (VCC < LVD threshold value, low voltage detected!)

ADC_PF (F037H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	ADCMIF
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 1 Rserved

bit0 **ADCMIF**: ADC hardware module interrupt. Once this bit is set to "1", it can be cleared.

0: Not trigger

1: Trigger

I2C_PF (F783H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	RSIF	STIF	ASIF	NSIF	DNIF
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved

bit4 **RSIF**: I^2C restart interrupt. Once this bit is set to "1", it can be cleared.
0: Disable
1: Enable

bit3 **STIF**: I^2C start interrupt. Once this bit is set to "1", it can be cleared.
0: Disable
1: Enable

bit2 **ASIF**: I^2C abnormal interrupt. Once this bit is set to "1", it can be cleared.
0: Disable
1: Enable

bit1 **NSIF**: I^2C normal stop interrupt. Once this bit is set to "1", it can be cleared.
0: Disable
1: Enable

bit0 **DNIF**: I^2C data finish interrupt. Once this bit is set to "1", it can be cleared.
0: Disable
1: Enable

Note: Flag bit of TK18 external efere will not be automatically cleared after responding to interrupt only if this bit is set to "1".

7. LVD

7.1 Overview

TK18 LVD provides a target low voltage level ranged from 2.5V – 3.2V. This programmable detection range can be write into LVDATRM register to realize voltage level detection. Once current VCC voltage level is detected lower than the target voltage, it can be detected by LVD so as to trigger flag bit and interrupt.

7.2 Related Control Registers

LVDATRM (F006H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	LVDV4	LVDV3	LVDV2	LVDV1	LVDV0
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

bit7 – 5 Reserved

bit4 – 0 **LVDV4~LVDV0**: Low voltage threshold (the range is from 2.455V to 3.182V with 45.5mV each step.)

01111: 2.455V (initial value)

10000: 2.500V

: :

11111: 3.182V

LVDCTL (F007H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	LVDEN	---	---	---	LVDMI
Read/write	---	---	---	R/W	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Reserved

bit4 **LVDEN**: LVD enable bit

0: Disable

1: Enable

bit3 – 1 Reserved

bit0 **LVDMI**: LVD hardware module interrupt

To ensure that LVD Occureds for interrupt on detecting low voltage and interrupt responds successfully, both LVDI bit and this hardware module interrupt enable bit have to be set to “1” beforehand. Otherwise, interrupt cann’t respond.

0: Disable

1: Enable

LVDSTA (F008H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	LVDSTS	---	---	---	LVDMIF
Read/write	---	---	---	R/-	---	---	---	-/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Reserved

bit4 **LVDSTS**: LVD status flag

0: VCC < LVDATRM threshold value

1: VCC > LVDATRM threshold value

bit3 – 1 Reserved

bit0 **LVDMIF**: LVD hardware module interrupt. Once this bit is set to "1", it can be cleared.

0: Not trigger (VCC > LVD threshold value, low voltage not detected!)

1: Trigger (VCC < LVD threshold value, low voltage detected!)

7.3 Instructinos and Notes

LVD is used to detect current VCC level, but for the case that VCC varies frequently caused by high-frequency noise eference ce, it's recommended to enable debounce option. Otherwise, frequent LVD trigger or interrupt may fail system normal operations. The following is an illustration:

For example, to check VCC value is lower than 3V, issue LVD interrupt:

◇ Set LVDATRM= 1CH (LVD threshold is 3.0V)

◇ Set LVDCTL= 11H (enable LVD function and interrupt)

◇ With the above configuration, LVD interrupt will be issued when VCC < LVD threshold.

8. WDT

8.1 Overview

TK18 adopts 32KHz LIRC as clock source for the 16 bit WDT. WDT internal counter is 16 bit up counter, in which lower 8 bit (CNT[7: 0]) are counted by the counter. While upper 8 bit count value can directly configure WDTVAL register. Once upper 8 bit count buffer value is equal to that of WDTVAL register, WDT will overflow and WDTOF will be set to "1" while chip be reset. Otherwise, if upper 8 bit count buffer value is equal to half count of WDTVAL register, WDTHF will be set to "1" and then WDT will interrupt. Related WDT functions are as follows:

- ◇ Reset chip
- ◇ Sleep mode wakeup
- ◇ 8 bit timer
- ◇ To prevent procedure from entering abnormal Disabled loop

8.2 Block Diagram

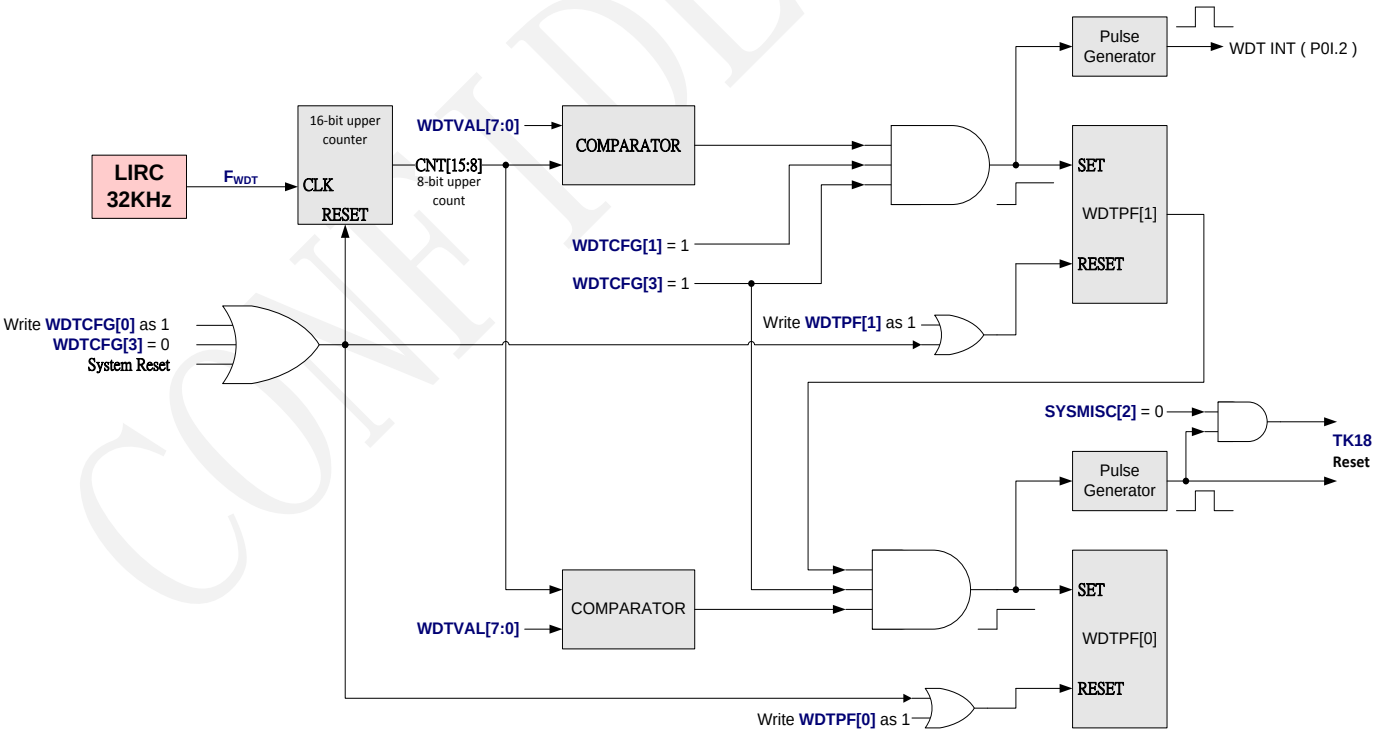


Diagram 8-1: WDT Block Diagram

8.3 Related Control Registers

WDTCFG (F100H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	WDTEN	---	WDTHI	WDTCL
Read/write	---	---	---	---	R/W	---	R/W	-/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Reserved

bit3 **WDTEN**: WDT enable bit

0: Disable

1: Enable

bit2 Reserved

bit1 **WDTHI**: WDT module half overflow interrupt

Once this bit is set to "1" and WDT counts to half way, WDTPF.1 half overflow flag bit WDTHF will be set to "1". However, to ensure that WDT Occureds for interrupt on half overflow and interrupt responds successfully, both WDTI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.

0: Disable

1: Enable

bit0 **WDTCL**: WDT reset

Once this bit is set to "1", WDT can be reset while both WDTHF and WDTOF bit will be cleared at the same time.

WDTPF (F101H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	WDTHF	WDTOF
Read/write	---	---	---	---	---	---	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 2 Reserved

bit1 **WDTHF**: WDT module half overflow interrupt. Once this bit is set to "1", it can be cleared.

0: Not overflow

1: Overflow

bit0 **WDTOF**: WDT overflow. Once this bit is set to "1", it can be cleared.

Once this bit overflows, TK18 will immediately reset and user can apply procedure in the chip reset entry to judge whether this bit is normal power on reset or WDT overflow reset, after which it should be set to "1" to clear it.

0: Not overflow

1: Overflow

WDTVAL (F102H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	WDTVAL							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **WDTVAL**: 8 bit WDT timer counter

The following is an illustration of how to use WDT overflow time to calculate WDTVAL assignment:

It's assumed that the expected WDT overflow time is 1.25 seconds, then the calculation formula is :

=> Overflow time = $(1/F_{WDT})$ x 256 x WDTVAL

1.25S= (1/32768Hz) * 256 * WDTVAL

1.25S= 7.8125mS * WDTVAL

WDTVAL= 1.25S / 7.8125mS= 160

then,the calculation formula of **WDTVAL** assignment is => WDT overflow time/7.8125mS

8.4 Instructions and Notes

Once TK18 enters normal operational mode after power-on reset, the internal LIRC 32KHz will keep operating till TK18 loses power. Therefore, it only needs initializing WDTCFG, WDTPF and WDTVAL to start WDT. The following is an illustration:

Example 1: WDT keeps monitoring so as to prevent procedure from entering abnormal Disabled loop. In that case, chip will be reset, steps are as follows:

◇ Set WDTVAL= 128 (WDT overflow time is 1S)

◇ Set WDTCFG= 09H (enable WDT, and clear WDT counter to begin counting)

◇ With the above configuration, WDT will overflow after 1S to reset chip. Therefore, it is recommended that user should regularly set WDTCFG.0 WDTCL to "1" to clear count in half overflow time.

Example 2: WDT is used as 8 bit timer to produce interrupt for every 500mS, and steps are as follows:

◇ Set WDTVAL= 128 (WDT overflow time is 1S, therefore half overflow time is 500mS)

◇ Set WDTCFG= 0BH (enable WDT and module interrupt, clear WDT counter to count)

◇ Set P0IE.2 WDTI to "1" (enable WDT interrupt source to respond)

◇ With the above configuration, WDT will produce interrupt for every 500mS.

Note: LIRC clock source produces ±20% error, which shall be take into consideration in setting WDT time.

9. Timer/Counter Timer0 and Timer1

9.1 Overview

TK18 provides 2 16-bits timers/counters, Timer 0 and Timer 1 (T0 and T1). These two timers can be internal or external timer. When used as internal timer, it counts the internal pulse. When on the 16 bits counting mode, timer can count 2^{16} pulse (65536). When treated as external counter, it counts the pulse transmitted from the T0 or T1 pin. Similarlly, if on the 16 bits counting mode, timer can count 2^{16} pulse (65536).

TK18 timer/counter T0 and T1 can be configured into different modes:

Mode	Bit	Range	Others
Mode 0	13	0～8191	
Mode 1	16	0～65535	
Mode2	8	0～255	Auto load
Mode3	8	0～255	

9.2 Block Diagram

9.2.1 T0 & T1 Mode 0 instruction

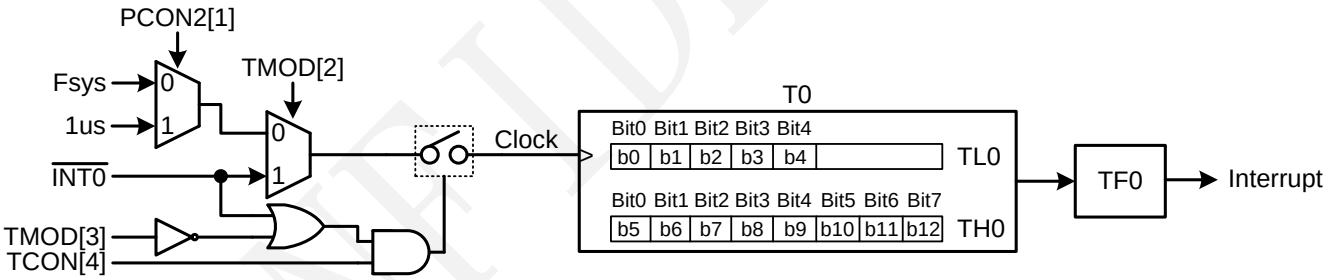


Diagram 9-1 TK18 T0 & T1 Mode 0 block diagram (T0 as example)

As demonstrated in Diagram 9-1, Mode 0 (TMOD[1:0]=00) is a 13 bits timer/counter, the counted value is saved respectively in TH0/1 and TL0/1 where TH0/1 has 8 bits, and TL0/1 has 5 bits. When executing timer function, set TMOD[2] as 0 and select counter frequency from Fsys or 1us. When executing counter function, set TMOD[2] as 1 and the counter source will be the pulse from $\overline{\text{INT0/1}}$ input pin.

There are two ways to enable timer/counter. One is to provide frequency from $\overline{\text{INT0/1}}$ for T0 or T1. To set TMOD[3] as 1 and TCON[4] as 1, then wait for the signal from $\overline{\text{INT0/1}}$ pin. When $\overline{\text{INT0/1}}$ is at low, counter will add 1 automatically, count from 0 to the default value and set TF0 as 1 to issue interrupt, then count from 0 to the default and set TF0 as 1 to issue interrupt and

reiterate this action.

Second way is to set Fsys or 1us (configured via PCON2[1]) as the frequency source of T0 or T1. Set TMOD[3:2] as 00, TCON[4] as 1, and timer will count from 0 to the default value and set TF0 as 1 to issue interrupt, then count from 0 to default value and set TF0 as I to issue interrupt and reiterate this action.

9.2.2 T0 & T1 Mode 1 instruction

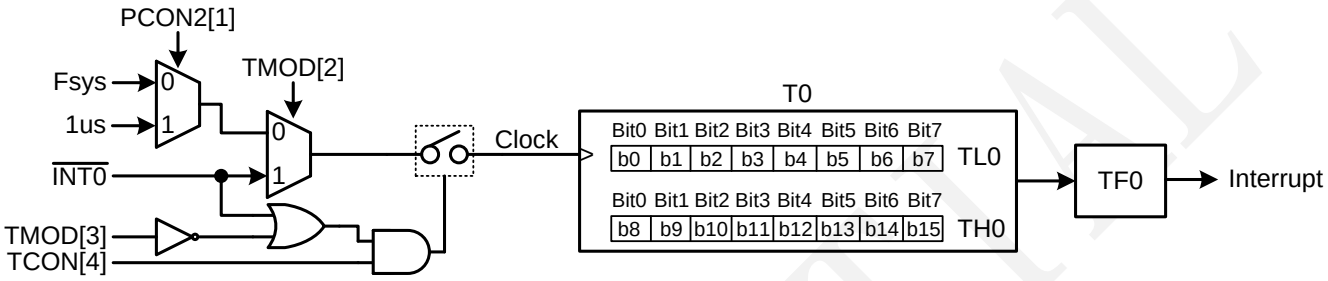


Diagram 9-2 TK18 T0 & T1 Mode 1 block diagram (T0 as example)

As demonstrated above, Mode 1 (TMOD[1:0]=01 is a 16 bit timer/counter. Its configuration is the same as Mode 0, please refer to Section 9.2.1 for details.

9.2.3 T0 & T1 Mode 1 instruction

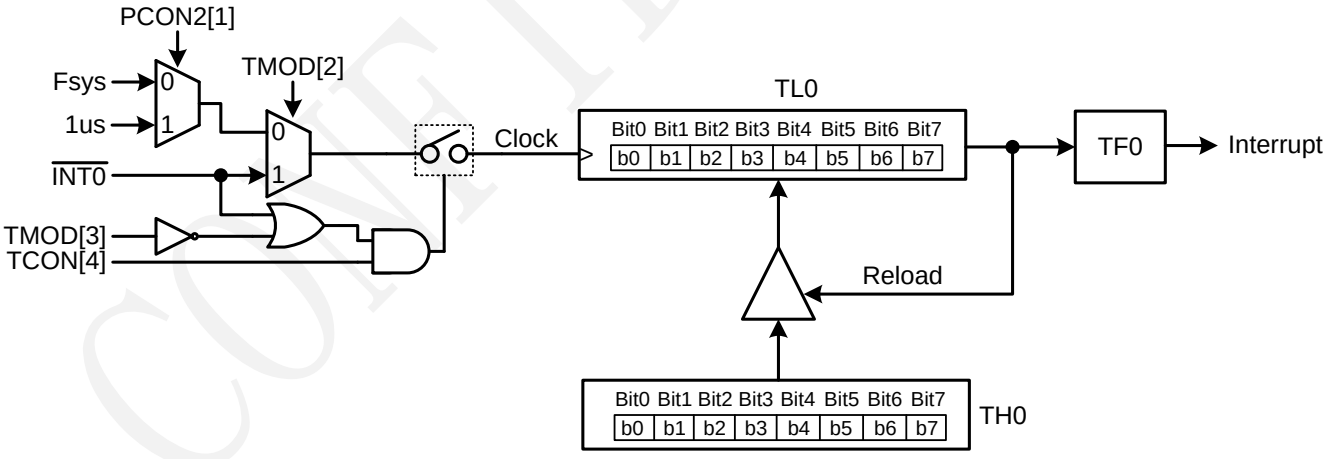


Diagram 9-3 TK18 T0 & T1 Mode 2block diagram (T0 as example)

As demonstrated in 9-3, Mode 2 is to provide 2 8-bits auto loading counters (T0 and T1), its value is saved in TL0. When TL0 counts to the default value (eg TL0=200), counter issues interrupt and automatically load the counted value from TH0 to TL0 and then count from 0 to the default value. As TL0/TH0 has 8 bits, the maximum counting range is 0~255, total of 256 pulse.

Counter/Timer switch method for T0 and T1 in Mode 2 is the same as in Mode 0; the initiation is also the same as Mode 0. Please refer to related details in Section 9.2.1. Except TMOD[1:0] must be configured as 11 to function under Mode 2.

9.3 Related Control Register

PCON2 (86H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	XRAMEN	---	---	TIMCLK	---
Read/write	---	---	---	R/W	---	---	R/W	---
Default	0	0	0	0	0	0	0	0

bit7-5 Reserved
bit3-2 Reserved
bit1 **TIMCLK**: TIMER0/TIMER1 F_{TIMCLK}
0: Set $F_{TSYSIMCLK}$ as TIMER0/Timer1 F_{TIMCLK}
1: Set 1μS as TIMER0/Timer1 F_{TIMCLK}
bit0 Reserved

Note: 1μS pulse is a unique design in TK18, which is for the convenience of user.

TCON (88H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **TF1**: T1 overflow interrupt, this bit will be automatically cleared after response.
0: Not occur
1: Occured
bit6 **TR1**: T1
0: Off
1: On, T1 begins to count
bit5 **TF0**: T0 overflow interrupt, this bit will be automatically cleared after response.
0: Not occur
1: Occured
bit4 **TR0**: T0 operation
0: Off
1: On, T0 begins to count
bit3 **IE1**: INT1 trigger interrupt
This bit will not be automatically cleared after response only if this bit is set to "1".
0: Not occur
1: Occured
bit2 **IT1**: INT1 trigger mode
0: Low-level trigger

1: Negative transition (high level→low level) trigger

bit1 **IE0**: INT0 trigger interrupt
This bit will not be automatically cleared after response only if this bit is set to "1".
0: Not occur
1: Occured

bit0 **IT0**: INT0 trigger mode
0: Low-level trigger
1: Negative transition (high level→low level) trigger

TMOD (89H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	GATE1	CT1	M1	M0	GATE0	CT0	M1	M0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **GATE1**: T1 gate
0: Timer/Counter1 operation is only controlled by TR1 other than level led in through external
pin INT1.
1: Timer/Counter1 operation is controlled by both TRI and level of external pin INT1.

Bit6 **CT1**: T1 operational mode
0: Timer
1: Counter

bit5-4 **M1~M0**: T1 operational mode
00: T1 is 13 bit timer (all TH1 8 bit and lower 5 bit in TL1)
01: T1 is 16 bit timer (all TH1 8 bit and TL1 8 bit)
10: T1 is 8 bit automatic reloading timer (once TL1 overflows, THI will reload)
11: T1 stops (the same as TR1=0)

bit3 **GATE0**: T0 gate
0: Timer/Counter0 operation is only controlled by TR0 other than level led in through external pin INT0
1: Timer/Counter0 operation is controlled by both TR0 and level of external pin INT0.

Bit2 **CT0**: T0 operational mode
0: Timer
1: Counter

bit1-0 **M1~M0**: T0 operational mode
00: T0 is 13 bit timer (all TH0 8 bit and lower 5 bit in TL0)
01: T0 is 16 bit timer (all TH0 8 bit and TL0 8 bit)
10: T0 is 8 bit automatic reloading timer (once TL0 overflows, TH0 will reload)
11: T0 stops (the same as TR0=0)

TL0 (8AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	**TL0**							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **TL0**: T0 lower byte data register

TL1 (8BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	**TL1**							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **TL1**: T0 upper byte data register

TH0 (8CH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	**TH0**							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **TH0**: T1 lower byte data register

TH1 (8DH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	**TH1**							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **TH1:** T1 upper byte data register

10. GPIO

10.1 Overview

TK18 has a maximum of 36 general GPIO, and each has its own input/output registers (input/output data RAM register, input/output enable control, and strong driving capability control). Certain ports have pull-up resistor enable control. In addition, all GPIO are optionally configured to be TXD/RXD/ICLK/IDAT/ SCL/SDA function ports. Pleaser refer to Diatram 10-1.

10.2 Block Diagram

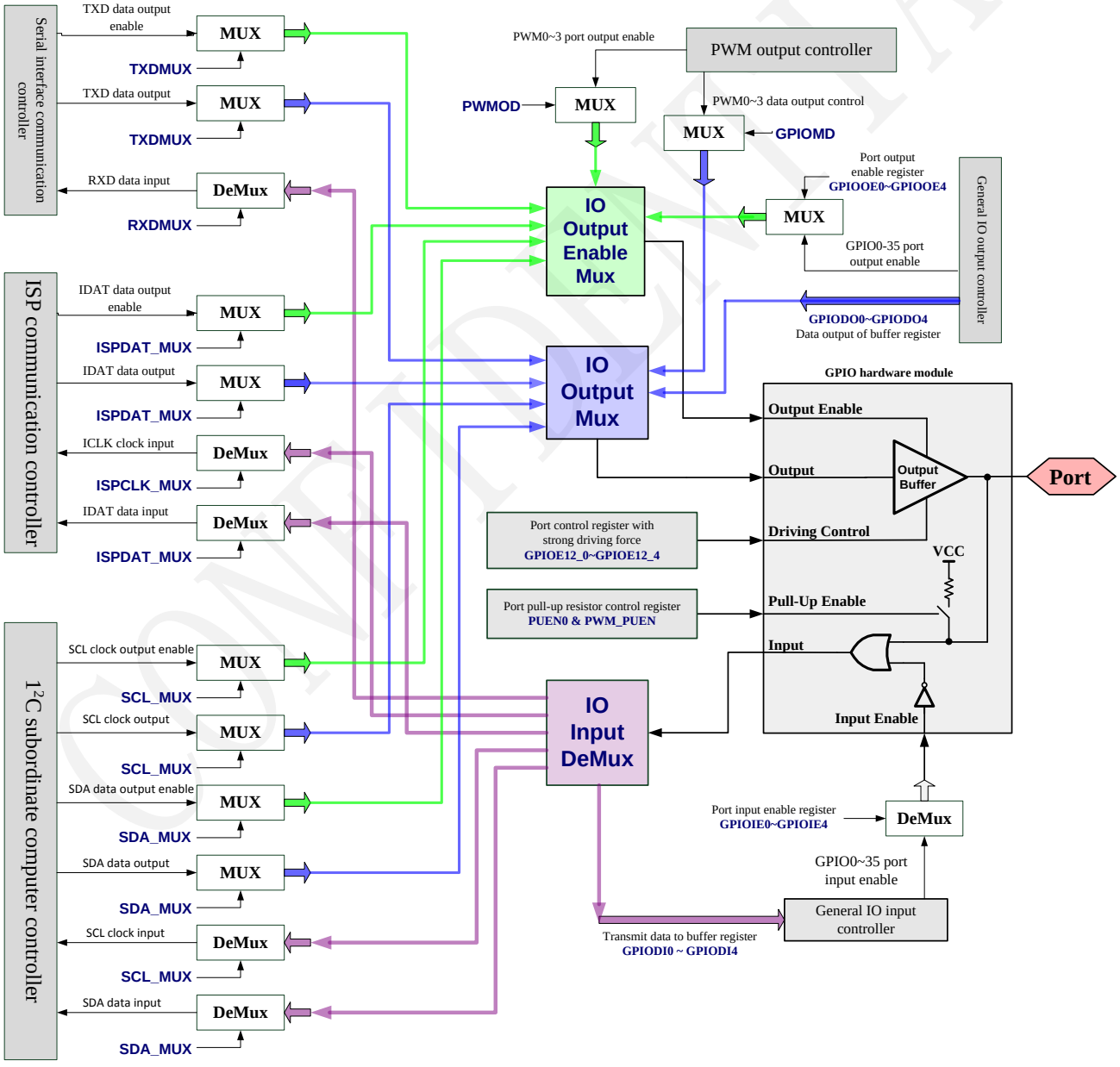


Diagram 10-1: Tk18 GPIO Module Block Diagram

10.3 Related Control Registers

GPIOMD (F200H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	G27PWM3	G26PWM2	G25PWM1	G24PWM0
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Rserved

bit3 **G27PWM3** : GPIO27 / PWM3 port

0: Disable PWM3 port, enable GPIO27 port (default)

1: Enable PWM3 port, disable GPIO27 port

bit2 **G26PWM2** : GPIO26 / PWM2 port

0: Disable PWM2 port, enable GPIO26 port (default)

1: Enable PWM2 port, disable GPIO26 port

bit1 **G25PWM1** : GPIO25 / PWM1 port

0: Disable PWM1 port, enable GPIO25 port (default)

1: Enable PWM1 port, disable GPIO25 port

bit0 **G24PWM0** : GPIO24 / PWM0 port

0: Disable PWM0 port, enable GPIO24 port (default)

1: Enable PWM0 port, disable GPIO24 port

GPIOOE0 (F202H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO7OE	IO6OE	IO5OE	IO4OE	IO3OE	IO2OE	IO1OE	IO0OE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO7OE~IO0OE**: GPIO7~GPIO0 port output

0: Disable (default)

1: Enable

GPIOOE1 (F203H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO15OE	IO14OE	IO13OE	IO12OE	IO11OE	IO10OE	IO9OE	IO8OE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO15OE~IO8OE**: GPIO15~GPIO8 port output

0: Disable (default)

1: Enable

GPIOOE2 (F204H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO23OE	IO22OE	IO21OE	IO20OE	IO19OE	IO18OE	IO17OE	IO16OE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO23OE~IO16OE**: GPIO23~GPIO16 port output

0: Disable (default)

1: Enable

GPIOOE3 (F205H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO31OE	IO30OE	IO29OE	IO28OE	IO27OE	IO26OE	IO25OE	IO24OE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO31OE~IO24OE**: GPIO31~GPIO24 port output

0: Disable (default)

1: Enable

GPIOOE4 (F206H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	IO35OE	IO34OE	IO33OE	IO32OE
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO35OE~IO32OE**: GPIO35~GPIO32 port output

0: Disable (default)

1: Enable

GPIODO0 (F207H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO7DO	IO6DO	IO5DO	IO4DO	IO3DO	IO2DO	IO1DO	IO0DO
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO7DO~IO0DO**: GPIO7~GPIO0 port data output register

0: Port output low level (default)

1: Port output high level

GPIODO1 (F208H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO15DO	IO14DO	IO13DO	IO12DO	IO11DO	IO10DO	IO9DO	IO8DO
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO15DO~IO8DO**: GPIO15~GPIO8 port data output register

0: Port output low level (default)

1: Port output high level

GPIODO2 (F209H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO23DO	IO22DO	IO21DO	IO20DO	IO19DO	IO18DO	IO17DO	IO16DO
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO23DO~IO16DO**: GPIO23~GPIO16 port data output register

0: Port output low level (default)

1: Port output high level

GPIODO3 (F20AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO31DO	IO30DO	IO29DO	IO28DO	IO27DO	IO26DO	IO25DO	IO24DO
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO31DO~IO24DO**: GPIO31~GPIO24 port data output register

0: Port output low level (default)

1: Port output high level

GPIODO4 (F20BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	IO35DO	IO34DO	IO33DO	IO32DO
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO35DO~IO32DO**: GPIO35~GPIO32 port data output register

0: Port output low level (default)

1: Port output high level

GPIOIE0 (F20CH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO7IE	IO6IE	IO5IE	IO4IE	IO3IE	IO2IE	IO1IE	IO0IE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO7IE~IO0IE**: GPIO7~GPIO0 port input

0: Disable (default)

1: Enable

GPIOIE1 (F20DH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO15IE	IO14IE	IO13IE	IO12IE	IO11IE	IO10IE	IO9IE	IO8IE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO15IE~IO8IE**: GPIO15~GPIO8 port input

0: Disable (default)

1: Enable

GPIOIE2 (F20EH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO23IE	IO22IE	IO21IE	IO20IE	IO19IE	IO18IE	IO17IE	IO16IE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO23IE~IO16IE**: GPIO23~GPIO16 port input

0: Disable (default)

1: Enable

GPIOIE3 (F20FH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO31IE	IO30IE	IO29IE	IO28IE	IO27IE	IO26IE	IO25IE	IO24IE
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO31IE~IO24IE**: GPIO31~GPIO24 port input

0: Disable (default)

1: Enable

GPIOIE4 (F210H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	IO35IE	IO34IE	IO33IE	IO32IE
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO35IE~IO32IE**: GPIO35~GPIO32 port input

0: Disable (default)

1: Enable

GPIODI0 (F211H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO7DI	IO6DI	IO5DI	IO4DI	IO3DI	IO2DI	IO1DI	IO0DI
Read/write	R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **IO7DI~IO0DI**: GPIO7~GPIO0 port data input register

0: Port input low level (default)

1: Port input high level

GPIODI1 (F212H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO15DI	IO14DI	IO13DI	IO12DI	IO11DI	IO10DI	IO9DI	IO8DI
Read/write	R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **IO15DI~IO8DI**: GPIO15~GPIO8 port data input register

0: Port input low level (default)

1: Port input high level

GPIODI2 (F213H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO23DI	IO22DI	IO21DI	IO20DI	IO19DI	IO18DI	IO17DI	IO16DI
Read/write	R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **IO23DI~IO16DI**: GPIO23~GPIO16 port data input register

0: Port input low level (default)

1: Port input high level

GPIODI3 (F214H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO31DI	IO30DI	IO29DI	IO28DI	IO27DI	IO26DI	IO25DI	IO24DI
Read/write	R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **IO31DI~IO24DI**: GPIO31~GPIO24 port data input register

0: Port input low level (default)

1: Port input high level

GPIODI4 (F215H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	IO35DI	IO34DI	IO33DI	IO32DI
Read/write	---	---	---	---	R/-	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **IO35DI~IO32DI**: GPIO35~GPIO32 port data input register

0: Port input low level (default)

1: Port input high level

GPIOE12_0 (F228H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO7HD	IO6HD	IO5HD	IO4HD	IO3HD	IO2HD	IO1HD	IO0HD
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO7HD~IO0HD**: port strong driving force

0: Disable (default)

1: Enable

GPIOE12_1 (F229H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO15HD	IO14HD	IO13HD	IO12HD	IO11HD	IO10HD	IO9HD	IO8HD
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO15HD~IO8HD**: Port strong driving force

0: Disable (default)

1: Enable

GPIOE12_2 (F22AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO23HD	IO22HD	IO21HD	IO20HD	IO19HD	IO18HD	IO17HD	IO16HD
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO23HD~IO16HD**: Port strong driving force

0: Disable (default)

1: Enable

GPIOE12_3 (F22BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IO31HD	IO30HD	IO29HD	IO28HD	IO27HD	IO26HD	IO25HD	IO24HD
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO31HD~IO24HD**: Port strong driving force

0: Disable (default)

1: Enable

GPIOE12_4 (F22CH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	IO35HD	IO34HD	IO33HD	IO32HD
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **IO35HD~IO32HD**: Port strong driving force

0: Disable (default)

1: Enable

GPWUA0 (F230H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	**GPW1IP1**	**GPW1IP0**	**GPW1TP**	**GPW1MI**	**GPW0IP1**	**GPW0IP0**	**GPW0TP**	**GPW0MI**
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-6 **GPW1IP1~GPW1IP0**: GPW1 trigger source (operate with GPW1TP bit)

While GPW1 is edge trigger (GPW1TP is 0),

00: Rising edge trigger (default)

01: Falling dege trigger

10: Twin edge (rising/falling) trigger

11: Reserved

While, GPW1 is level trigger (GPW1TP is 1),
00: High-level trigger
01: Low-level trigger
10: Reserved
11: Reserved

bit5 **GPW1TP**: GPW1 trigger
0: Edge trigger (default)
1: Level trigger

bit4 **GPW1MI**: GPW1 hardware module interrupt
0: Disable
1: Enable

bit3-2 **GPW0IP1~GPW0IP0:** GPW0 trigger source (operate with GPW0TP bit)
While GPW0 is edge trigger (GPW0TP is 0)
00: Rising edge trigger (default)
01: Falling dege trigger
10: Twin edge (rising/falling) trigger
11: Reserved
While GPW1 is level trigger (GPW0TP is 1)
00: High-level trigger
01: Low-level trigger
10: Reserved
11: Reserved

bit1 **GPW0TP**: GPW0 trigger
0: Edge trigger (default)
1: Level trigger

bit0 **GPW0MI**: GPW0 hardware module interrupt
0: Disable
1: Enable

GPWUA1 (F231H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	**GPW3IP1**	**GPW3IP0**	**GPW3TP**	**GPW3MI**	**GPW2IP1**	**GPW2IP0**	**GPW2TP**	**GPW2MI**
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-6 **GPW3IP1~GPW3IP0**: GPW3 trigger source (operate with GPW3TP bit)
While GPW3 is edge trigger (GPW3TP is 0))
00: Rising edge trigger (default)
01: Falling dege trigger
10: Twin edge (rising/falling) trigger
11: Reserved

While GPW3 is level trigger (GPW3TP is 1)
00: High-level trigger
01: Low-level trigger
10: Reserved
11: Reserved

bit5 **GPW3TP**: GPW3 trigger
0: Edge trigger (default)
1: Level trigger

bit4 **GPW3MI**: GPW3 hardware module interrupt
0: Disable
1: Enable

bit3-2 **GPW2IP1~GPW2IP0**: GPW2 trigger source (operate with GPW2TP bit)
While GPW2 is edge trigger (GPW2TP is 0))
00: Rising edge trigger (default)
01: Falling dege trigger
10: Twin edge (rising/falling) trigger
11: Reserved
While GPW2 is level trigger (GPW2TP is 1)
00: High-level trigger
01: Low-level trigger
10: Reserved
11: Reserved

bit1 **GPW2TP**: GPW2 trigger
0: Edge trigger (default)
1: Level trigger

bit0 **GPW2MI**: GPW2 hardware module interrupt
0: Disable
1: Enable

GPWUPF (F232H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	GPW3MIF	GPW2MIF	GPW1MIF	GPW0MIF
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Rserved

bit3 **GPW3MIF**: GPW3 hardware module interrupt. Once this bit is set to “1”, it can be cleared.
0: Not occur
1: Occured

bit2 **GPW2MIF**: GPW2 hardware module interrupt. Once this bit is set to “1”, it can be cleared.
0: Not occur
1: Occured

bit1 **GPW1MIF**: GPW1 hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

bit0 **GPW0MIF**: GPW0 hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not occur
1: Occured

PUEN0 (F004H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	P33R4K7	P32R4K7	P35R4K7	P34R4K7	P33R40K	P32R40K	P35R40K	P34R40K
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	0	0	0	0

bit7 **P33R4K7**: GPIO33 port 4.7K pull-up resistor
0: Disable
1: Enable (default)

bit6 **P32R4K7**: GPIO32 port 4.7K pull-up resistor
0: Disable
1: Enable (default)

bit5 **P35R4K7**: GPIO35 port 4.7K pull-up resistor
0: Disable
1: Enable (default)

bit4 **P34R4K7**: GPIO34 port 4.7K pull-up resistor
0: Disable
1: Enable (default)

bit3 **P33R40K**: GPIO33 port 40K pull-up resistor
0: Disable (default)
1: Enable

bit2 **P32R40K**: GPIO32 port 40K pull-up resistor
0: Disable (default)
1: Enable

bit1 **P35R40K**: GPIO35 port 40K pull-up resistor
0: Disable (default)
1: Enable

bit0 **P34R40K**: GPIO34 port 40K pull-up resistor
0: Disable (default)
1: Enable

PWM_PUEN (F031H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	P27R4K7	P26R4K7	P25R4K7	P24R4K7	P27R40K	P26R40K	P25R40K	P24R40K
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	1	0	0	0	0

bit7 **P27R4K7**: GPIO27 (PWM3) port 4.7K pull-up resistor
0: Disable (default)
1: Enable

bit6 **P26R4K7**: GPIO26 (PWM2) port 4.7K pull-up resistor
0: Disable (default)
1: Enable

bit5 **P25R4K7**: GPIO25 (PWM1) port 4.7K pull-up resistor
0: Disable
1: Enable (default)

bit4 **P24R4K7**: GPIO24 (PWM0) port 4.7K pull-up resistor
0: Disable
1: Enable (default)

bit3 **P27R40K**: GPIO27 (PWM3) port 40K pull-up resistor
0: Disable (default)
1: Enable

bit2 **P26R40K**: GPIO26 (PWM2) port 40K pull-up resistor
0: Disable (default)
1: Enable

bit1 **P25R40K**: GPIO25 (PWM1) port 40K pull-up resistor
0: Disable (default)
1: Enable

bit0 **P24R40K**: GPIO24 (PWM0) port 40K pull-up resistor
0: Disable (default)
1: Enable

CEXT_Ctrl (FA2BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	DI	Reserved	HCO	IOEN	CXEN	DIEN	DOEN	DO
Read/write	R/-	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **DI**: input value
0: Low
1: High

bit6 **Reserved**

bit5 **HCO**: High current output enable
0: Normal current output
1: High current output
Detail list as below

Item	I_{OH} (VCC = 5V, V_{OH} = 4.5V)	I_{OL} (VCC = 5V, V_{OL} = 0.4V)
HCO = 0	-5mA (Typ)	8mA (Typ)
HCO = 1	-19mA (Typ)	25mA (Typ)

bit4 **IOEN**: GPIO or CEXT selection
0: Reserved
1: I/O mode

bit3 **CXEN**: GPIO or CEXT selection
0: I/O mode
1: CEXT function
Detail list as below

Bit4:3	CEXT Pin status
00	Unknow
01	CEXT function
10	I/O mode
11	Unknow

bit2 **DIEN**: Input enable
0: Disable (default)
1: Enable

bit1 **DOEN**: Output enable
0: Disable (default)
1: Enable

bit0 **DO**: Output value
0: Low
1: High

11. PWM

11.1 Overview

TK18 provides up to 4 channel 8 bit PWMs, which are PWM0, PWM1, PWM2, and PWM3. Althouth sharing one 8 bit PWM clock source, each PWM has its own independent 8 bit Cycle Length and Duty Ratio registers to configure. If only procedure configures related registers, PWM module will produce corresponding PWM wave output.

Note: Since package below LQFP44 will not provide PWM3/GPIO27 pin, PWM3 function can be realized through PWM3/AD0/GPIO28/TK25 pin, if necessary. Refer to MAC_OPT register for detailed operational instructions.

11.2 Block Diagram

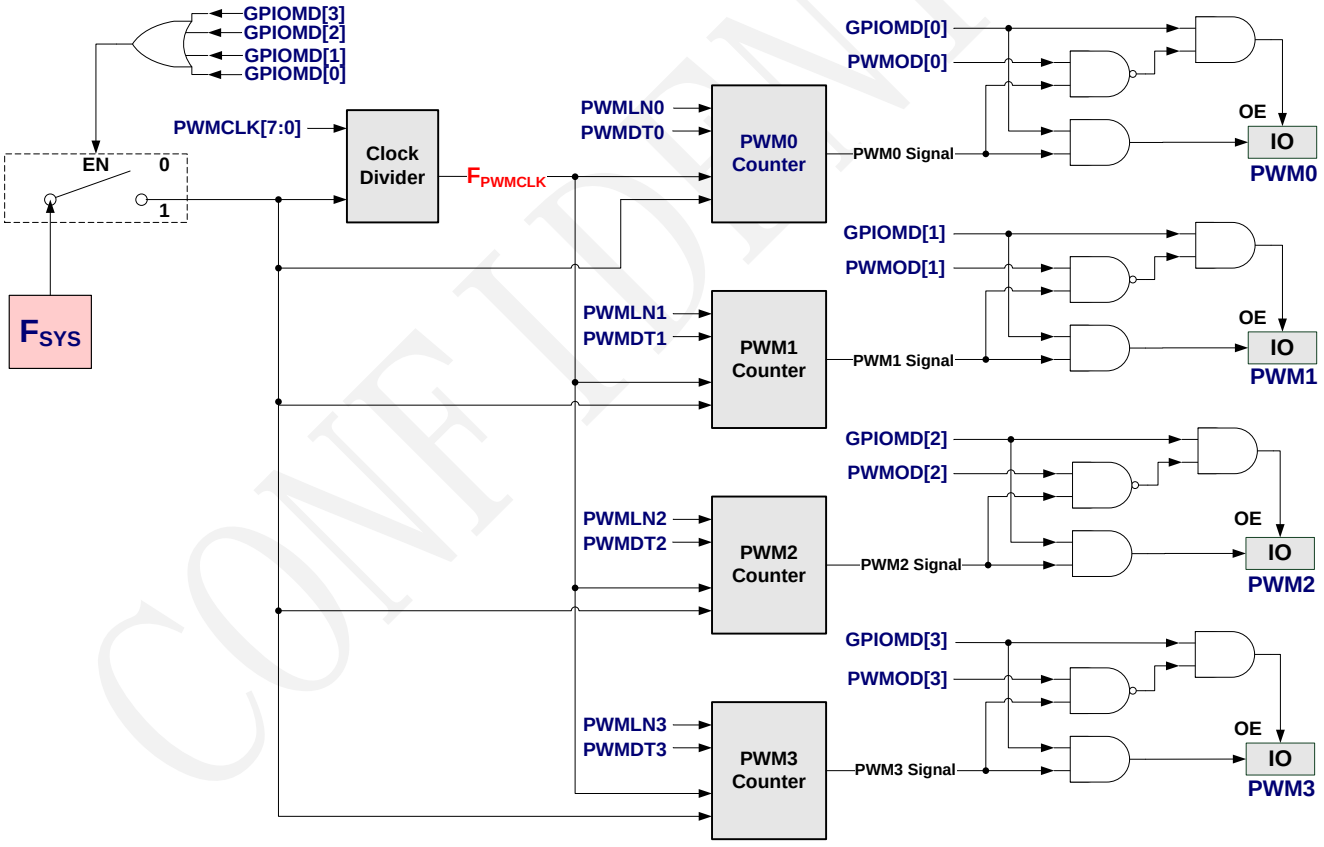


Diagram 11-1 TK18 PWM Module Block Diagram

11.3 Related Control Registers

GPIOMD (F200H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	G27PWM3	G26PWM2	G25PWM1	G24PWM0
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Rserved

bit3 **G27PWM3** : GPIO27 / PWM3 port

0: Disable PWM3 port, enable GPIO27 port (default)

1: Enable PWM3 port, disable GPIO27 port

bit2 **G26PWM2** : GPIO26 / PWM2 port

0: Disable PWM2 port, enable GPIO26 port (default)

1: Enable PWM2 port, disable GPIO26 port

bit1 **G25PWM1** : GPIO25 / PWM1 port

0: Disable PWM1 port, enable GPIO25 port (default)

1: Enable PWM1 port, disable GPIO25 port

bit0 **G24PWM0** : GPIO24 / PWM0 port

0: Disable PWM0 port, enable GPIO24 port (default)

1: Enable PWM0 port, disable GPIO24 port

PWMLN0 (F220H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMLN0: PWM0 cycle control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMDT0 (F221H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMDT0: PWM0 duty ratio control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMLN1 (F222H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMLN1: PWM1 cycle control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMDT1 (F223H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMDT1: PWM1 duty ratio control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMLN2 (F224H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMLN2: PWM2 cycle control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMDT2 (F225H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMDT2: PWM2 duty ratio control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMLN3 (F226H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMLN3: PWM3 cycle control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMDT3 (F227H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMDT3: PWM3 duty ratio control register							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWMLN0~PWMLN3 Cycle Length Configuraiton Instruction

00000000: 256 F_{PWMCLK} (default)
00000001: 1 F_{PWMCLK}
00000010: 2 F_{PWMCLK}
: : : :
11111111: 255 F_{PWMCLK}

F_{PWMCLK} clock source comes from PWMCLK configuration

PWMDT0~PWMDT3 Duty Ratio Configuration Instruction

00000000: 256 F_{PWMCLK} (default)
00000001: 1 F_{PWMCLK}
00000010: 2 F_{PWMCLK}
: : : :
11111111: 255 F_{PWMCLK}

PWMOD (F22DH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	PWM3O	PWM2O	PWM1O	PWM0O
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-4 Reserved
bit3 **PWM3O**: PWM3 port output type
0: PWM3 port is push-put output (default)
1: PWM3 port is open-drain output
bit2 **PWM2O**: PWM2 port output type
0: PWM2 port is push-put output (default)
1: PWM2 port is open-drain output
bit1 **PWM1O**: PWM1 port output type
0: PWM1 port is push-put output (default)
1: PWM1 port is open-drain output
bit0 **PWM0O**: PWM0 port output type
0: PWM0 port is push-put output (default)
1: PWM0 port is open-drain output

PWMCLK (F22EH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	PWMCLK: PWM clock source control							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **PWMCLK**: F_{PWMCLK} clock source configuration
00000000: F_{PWMCLK}= F_{SYS} /1
00000001: F_{PWMCLK}= F_{SYS} /2
: :
11111111: F_{PWMCLK}= F_{SYS} /256

MAC_OPT (F047H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	AD0PWM3	---	---	---	---	---	---	---
Read/write	R/W	---	---	---	---	---	---	---
Default	0	0	0	0	0	0	0	0

bit7 **AD0PWM3**: PWM3/AD0/GPIO28/TK25 PWM3 output
0: Disable PWM3/AD0/GPIO28/TK25 PWM3 signal output (default)
1: Enable PWM3/AD0/GPIO28/TK25 PWM3 signal output

Bit6-0 Reserved

11.4 Relations between PWM Output and GPIOD Initial Value

Since TK18 has 4 PWM output ports that are multiplexed with 4 GPIO respectively (that is PWM3/GPIO27, PWM2/GPIO26, PWM1/GPIO25 and PWM0/GPIO24), related GPIOD initial values will also decide the voltage level status of PWM output. The following is an illustration.

◇ GPIOD initial value is "1" previously, PWM port output will be at high level.

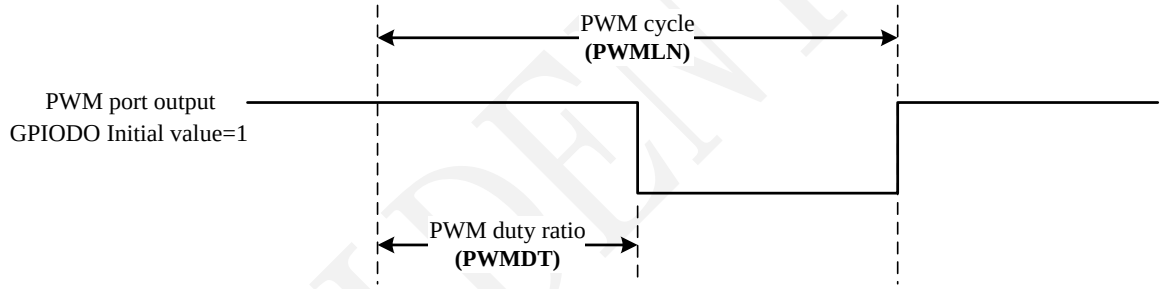


Diagram 11-2: PWM Output Waveform when GPIOD Initial Value is 1

◇ GPIOD initial value is "0" previously, PWM port output will be at low level.

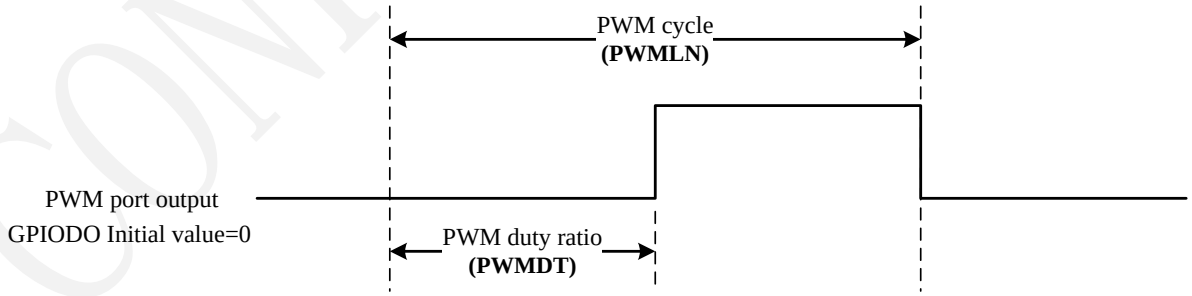


Diagram 11-3: PWM Output Wafeform when GPIOD Initial Value is 0

Note: When configured time of PWMDT is larger than or equal to that of PWMLN, PWM will output waveform with 100% duty ratio.

12. TK

12.1 Overview

TK18 integrates a hardware touch sensor controller, which adopes scheme derived from Kirchhoff theorem (that is charge transfer scheme), to perform highly cost effective capacitive sensor touch key. Each complete touch scan cycle consists of Charge, Charge Transfer & Discharge phases, which are controlled by S0, S1 & S2 control registers.

TK18 supports up to 28 touch keys. Each TK port can be enable or disable by its individual control register.Moreover, TK18 provides advanced various hardware of signal shielding, noise reducing and automatic environmental adjustment for application in varous environments and products. As to TK hardware modules that are particular to TK18, ene also provide special C language and Assembly Language software package for Tk18 so that usrs can immediately start and finish their projects.

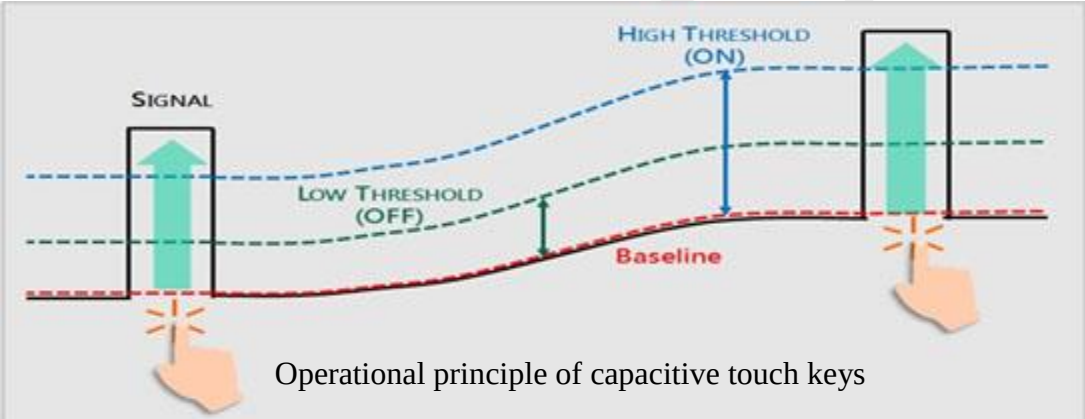


Diagram 12-1: TK18 TK Signal Scan Schematic Diagram

12.2 Related Control Register

CHGCYC (FA00H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	S0T3	S0T2	S0T1	S0T0
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Reserved

bit3 – 0 **S0T3~ S0T0**: Charge cycle (S0) control

During S0 period, TK capacitor will be charged up to reference voltage.

1 charge cycle = 1 scan cycle (T_{TKSCAN})

0000: 1 T_{TKSCAN}

0001: 2 T_{TKSCAN}

: :

: :

1111: 16 T_{TKSCAN}

T_{TKSCAN} = 1/scan clock

TRNCYC (FA01H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	S1T3	S1T2	S1T1	S1T0
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Reserved

bit3 – 0 **S1T3~ S1T0**: Transfer cycle (S1) control

During S1 period, TK transfers its charge to CEXT for charge accumulation.

1 S1 = 1 T_{TKSCAN}

0000: 1 T_{TKSCAN}

0001: 2 T_{TKSCAN}

: :

: :

1111: 16 T_{TKSCAN}

TTKSCAN = 1/scan clock

IDLECYC (FA02H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	S2T3	S2T2	S2T1	S2T0
Read/write	---	---	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 4 Reserved

bit3 – 0 **S2T3~ S2T0**: Control of Idle cycle between S0 and S1

0000: 1 scan cycle idle

0001: 2 scan cycles idle

: :

: :

1111: 16 scan cycles idle

SCANWIN (FA05H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	TKSW7	TKSW6	TKSW5	TKSW4	TKSW3	S2T2	S2T1	TKSW0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **TKSW7~ TKSW0**: TK scan sampling cycle T_{TKSWIN}

00000000: 1 T_{TKSWIN}

00000001: 2 T_{TKSWIN}

: :

: :

11111111: 256 T_{TKSWIN}

WINCTRL (FA06H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	SWCTRL
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 1 Rserved

bit0 **SWCTRL**: T_{TKSWIN} source configuration
0: 1 T_{TKSWIN} = 512 T_{TKSCAN}
1: 1 T_{TKSWIN} = 1024 T_{TKSCAN}

REXTCTRL (FA0BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	RVAL5	RVAL4	RVAL3	RVAL2	RVAL1	RVAL0	---	REXTEN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 2 **RVAL5~ RVAL0**: TK scan discharge resistance REXT (REXT initial value = 14KΩ)
Set RVAL0 as 1: + 0.5KΩ
Set RVAL1 as 1: + 1KΩ
Set RVAL2 as 1: + 2KΩ
Set RVAL3 as 1: + 4KΩ
Set RVAL4 as 1: + 8KΩ
Set RVAL5 as 1: + 16KΩ
For example:
RVAL5-RVAL0 is 000000: REXT= 14KΩ (initial value)
RVAL5-RVAL0 is 000001: REXT= 14.5KΩ
RVAL5-RVAL0 is 001100: REXT= 20KΩ
RVAL5-RVAL0 is 100011: REXT= 31.5KΩ
RVAL5-RVAL0 is 111111: REXT= 45.5KΩ (Maximum)

bit1 Reserved

bit0 **REXTEN**: TK scan discharge resistance REXT
0: Disable
1: Enable

SHIELDCTRL (FA0CH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	SPFEN	STS	SSIGS
Read/write	---	---	---	---	---	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 3 Rserved

bit2 **SPFEN**: Shielding signal source
0: Ground (GND)
1: Floating

bit1 **STS:** Shielding signal high level source
0: I/O port high voltage level (approaching VCC)
1: 1.8V (LDO18 regulator tube level)
bit0 **SSIGS**: Shielding signal type
0: The same as TK port signal
1: Ground (GND)

SCANCTRL (FA0DH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	NSEP
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 1 Rserved
bit0 **NSEP**: Port status of TK that currently have not been scanned (starting TK)
0: Ground (GND)
1: Floating

PORTEN0 (FA17H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	P7EN	P6EN	P5EN	P4EN	P3EN	P2EN	P1EN	P0EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **P7EN~ P0EN** : TK7~TK0 port
0: Disable
1: Enable

PORTEN1 (FA18H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	P15EN	P14EN	P13EN	P12EN	P11EN	P10EN	P9EN	P8EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **P15EN~ P8EN** : TK15~TK8 port
0: Disable
1: Enable

PORTEN2 (FA19H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	P23EN	P22EN	P21EN	P20EN	P19EN	P18EN	P17EN	P16EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **P23EN~ P16EN** : TK23~TK16 port
0: Disable
1: Enable

PORTEN3 (FA1AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	P28EN	P27EN	P26EN	P25EN	P24EN
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved
bit4 – 1 **P28EN~ P25EN** : TK28~TK25 port
0: Disable
1: Enable
bit0 **P24EN**: TK24 (DUMMY port 24) for correction of internal environmental variation
This dummy port is used, if necessary, as a reference for automatic environmental correction through comparison of sampling values with other used ports.
0: Disable
1: Enable

Note: Each TK port has an individual port enable bit. Disable TK ports have to be disabled.

SHIELDEN0 (FA1BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	S7EN	S6EN	S5EN	S4EN	S3EN	S2EN	S1EN	S0EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **S7EN~ S0EN**: TK7~TK0 port shielding function
0: Disable
1: Enable

SHIELDEN1 (FA1CH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	S15EN	S14EN	S13EN	S12EN	S11EN	S10EN	S9EN	S8EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **S15EN~ S8EN**: TK15~TK8 port shielding function
0: Disable
1: Enable

SHIELDEN2 (FA1DH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	S23EN	S22EN	S21EN	S20EN	S19EN	S18EN	S17EN	S16EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 0 **S23EN~ S16EN**: TK23~TK16 port shielding function
0: Disable
1: Enable

SHIELDEN3 (FA1EH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	S28EN	S27EN	S26EN	S25EN	S24EN
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved
bit4 – 1 **S28EN~ S25EN**: TK28~TK25 port shielding function
0: Disable
1: Enable
bit0 **S24EN**: Shielding function of TK24 (DUMMY port 24) for correction of internal environmental variation
0: Disable
1: Enable

Note: Each TK port has an individual shielding function enable bit. Even if this TK channel is disable, the shielding function still can independently operate and control; however, shielding function is invalid to currently enable and scanned TK channels.

SCANMODEN (FA20H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	SCEN
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 1 Rserved
bit0 **SCEN**: TK module scanning
Once this bit is set to "1", TK module is enable, and then enable TK port scanning begins.
0: Disable
1: Enable

INTEN (FA22H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	TKMI
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit0 **TKMI**: TK port scan finish module interrupt

To ensure that TK port Occureds for interrupt on finishing scan and interrupt responds successfully, both TKI bit and this hardware module interrupt enable bit have to be set to "1" beforehand. Otherwise, interrupt cann't respond.

0: Disable

1: Enable

PENDFLAG (FA23H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	TKMIF
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit0 **TKMIF**: TK port scan finish module interrupt. Once this bit is set to "1", it can be cleared.

0: Not occur

1: Occured

SCANCLK_DIV (F032H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	TKCLK2	TKSCLK1	TKSCLK0
Read/write	---	---	---	---	---	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 3 Reserved

bit2 – 0 **TKSCLK2~TKSCLK0**: TK scan clock (F_{TKSCAN}) source (F_{TKSCAN} initial value=7MHz)

000: $F_{HOSC}/4$ (F_{TKSCAN} = 28MHz/4 = 7MHz)

100: $F_{HOSC}/2$ (F_{TKSCAN} = 28MHz/2 = 14MHz)

Others: Reserved

12.3 Instructions and Notes

Please refer to related files provided by ene such as "Software Package Manual", "Hardware Manual", or just contact ene.

13. LED Driver

13.1 Overview

TK18 provides up to 7 COM x 8 SEG (56) hardware common cathode LED drivers. This module is independent hardware with capabilities of digital display register, scanning driver and high driving current. Simply speaking, this LED driver is functionally similar to popular 16XX LED driving chip. It only needs to store display data in display register for users to directly drive LED.

13.2 Block Diagram

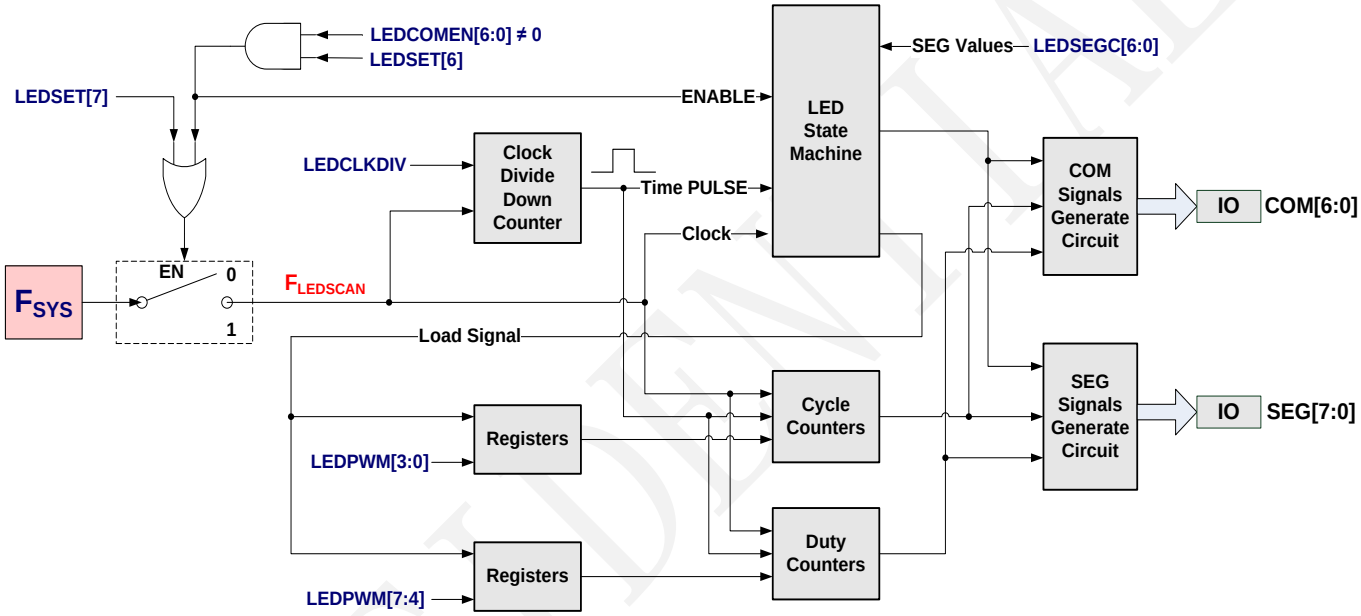


Diagram 13-1: TK18 LED Driver Block Diagram

13.3 Related Control Registers

LEDSET (F300H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	LCLKEN	LEDEN	---	---	COMT3	COMT2	COMT1	COMT0
Read/write	R/W	R/W	---	---	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **LCLKEN**: LED scan clock ($F_{LEDSCAN}$) source
0: Disable
1: Enable

bit6 **LEDEN**: LED module scan. Once this bit is set to "1", LED scan will be enable.
0: Disable
1: Enable

bit5-4 Reserved

bit3-0 **COMT3~COMT0**: PWM cycle configuration of COM port drive

0000: 1 LED PWM cycle (T_{LEDPWM})

0001: 2 LED PWM cycle (T_{LEDPWM})

: :

1111: 16 LED PWM cycle (T_{LEDPWM})

LEDCLKDIV (F301H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	LEDCLKDIV: LED Display Control clock divider							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **LEDCLKDIV**: LED scan clock ($F_{LEDSCAN}$) source configuration

00000000: $F_{LEDSCAN}$= F_{SYS} /1

00000001: $F_{LEDSCAN}$= F_{SYS} /2

: :

11111111: $F_{LEDSCAN}$= F_{SYS} /256

LEDPWM (F302H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	LPWMDUTY: LED PWM duty				TLEDPWM: LED PWM cycle length			
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-4 **LPWMDUTY**: LED PWM duty ratio configuration

0000: 0 LED clock ($F_{LEDSCAN}$) time

0001: 1 LED clock ($F_{LEDSCAN}$) time

: :

1111: 15 LED clock ($F_{LEDSCAN}$) time

bit3-0 **TLEDPWM**: LED PWM cycle (T_{LEDPWM}) configuration

0000: 16 LED clock ($F_{LEDSCAN}$) time

0001: 1 LED clock ($F_{LEDSCAN}$) time

: :

1111: 15 LED clock ($F_{LEDSCAN}$) time

LEDCOMEN (F303H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	COM6OP	COM6EN	COM5EN	COM4EN	COM3EN	COM2EN	COM1EN	COM0EN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **COM6OP**: COM6 signal output, default is GPIO34 port

0: Select GPIO34 port as COM6 signal output

1: Select GPIO0 port as COM6 signal output

bit6 **COM6EN**: COM6 port, COM6 signal will be output through COM6OP configured port
0: Disable
1: Enable

bit5 **COM5EN**: COM5 port
0: Disable
1: Enable

bit4 **COM4EN**: COM4 port
0: Disable
1: Enable

bit3 **COM3EN**: COM3 port
0: Disable
1: Enable

bit2 **COM2EN**: COM2 port
0: Disable
1: Enable

bit1 **COM1EN**: COM1 port
0: Disable
1: Enable

bit0 **COM0EN**: COM0 port
0: Disable
1: Enable

LEDSEGC0 (F304H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C0SEG7	C0SEG6	C0SEG5	C0SEG4	C0SEG3	C0SEG2	C0SEG1	C0SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C0SEG7~C0SEG0**: Data display register of COM0 corresponding SEG7~SEG0
0: LED OFF (COM port of currently scanned LED will pull down voltage level while SEG port push down it.)
1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

LEDSEGC1 (305H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C1SEG7	C1SEG6	C1SEG5	C1SEG4	C1SEG3	C1SEG2	C1SEG1	C1SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C1SEG7~C1SEG0**: Data display register of COM1 corresponding SEG7~SEG0
0: LED OFF (currently scanned LED and its COM port will pull down voltage level while SEG port will push down it.)
1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

LEDSEGC2 (F306H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C2SEG7	C2SEG6	C2SEG5	C2SEG4	C2SEG3	C2SEG2	C2SEG1	C2SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C2SEG7~C2SEG0**: Data display register of COM2 corresponding SEG7~SEG0
0: LED OFF (currently scanned LED and its COM port will pull down voltage level while SEG port will push down it.)
1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

LEDSEGC3 (F307H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C3SEG7	C3SEG6	C3SEG5	C3SEG4	C3SEG3	C3SEG2	C3SEG1	C3SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C3SEG7~C3SEG0**: Data display register of COM3 corresponding SEG7~SEG0
0: LED OFF (currently scanned LED and its COM port will pull down voltage level while SEG port will push down it.)
1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

LEDSEGC4 (F308H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C4SEG7	C4SEG6	C4SEG5	C4SEG4	C4SEG3	C4SEG2	C4SEG1	C4SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C4SEG7~C4SEG0**: Data display register of COM4 corresponding SEG7~SEG0
0: LED OFF (currently scanned LED and its COM port will pull down voltage level while SEG port will push down it.)
1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

LEDSEGC5 (F309H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C5SEG7	C5SEG6	C5SEG5	C5SEG4	C5SEG3	C5SEG2	C5SEG1	C5SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C5SEG7~C5SEG0**: Data display register of COM5 corresponding SEG7~SEG0

0: LED OFF (currently scanned LED and its COM port will pull down voltage level while SEG port will push down it.)

1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

LEDSEGC6 (F30AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	C6SEG7	C6SEG6	C6SEG5	C6SEG4	C6SEG3	C6SEG2	C6SEG1	C6SEG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **C6SEG7~C6SEG0**: Data display register of COM6 corresponding SEG7~SEG0

0: LED OFF (currently scanned LED and its COM port will pull down voltage level while SEG port will push down it.)

1: LED ON (COM port of currently scanned LED will pull down voltage level while SEG port push up it.)

14. UART

14.1 Overview

TK18 provides 1 set of UART serial port communication and this serial port also support original ports of standard 8051 core. The only difference is that TK18 TXD/RXD port has enhanced flexibility. User is able to use TXDMUX and RXDMUX registers to map ports to any pin from GPIO0~GPIO35 to realize its function.

Note: Although package below LQFP44 will not contain TXD and RXD pins, user can still use TXDMUX and RXDMUX registers to map pin function to any GPIO port. **(Caution: TXD and RXD cannot be configured together.)**

14.2 Block Diagram

User simply saves the data to the serial buffer (SBUF) and TK18 will send the 8 bits data bit by bit. It is the same with receiving serial data. TK 18 will save the received data bit by bit into SBUF. When SBUF is full, an interrupt will be issued and software will retrieve data from the SBUF. When sending data, input all data into SBUF and be sent bit by bit. Receving SBUF and sending SBUF require two different 8-bit registers. There are 4 modes available in the TK18 serial port and Baud rate are different under different modes:

- Mode 0: Baud rate is configured via SCON4[1:0]. Under this mode, Baud rate is fixed (sending or receiving data) and data length is 8 bits, TXD is serial data output/input and RXD is the pulse signal (clock). Therefore when receiving or sending data, RXD sends clock and TXD sends data as shown in diagram 14-1.

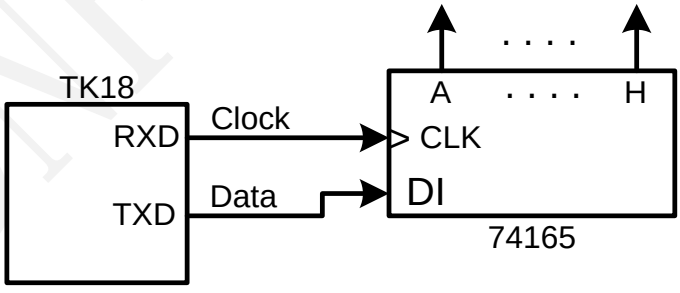
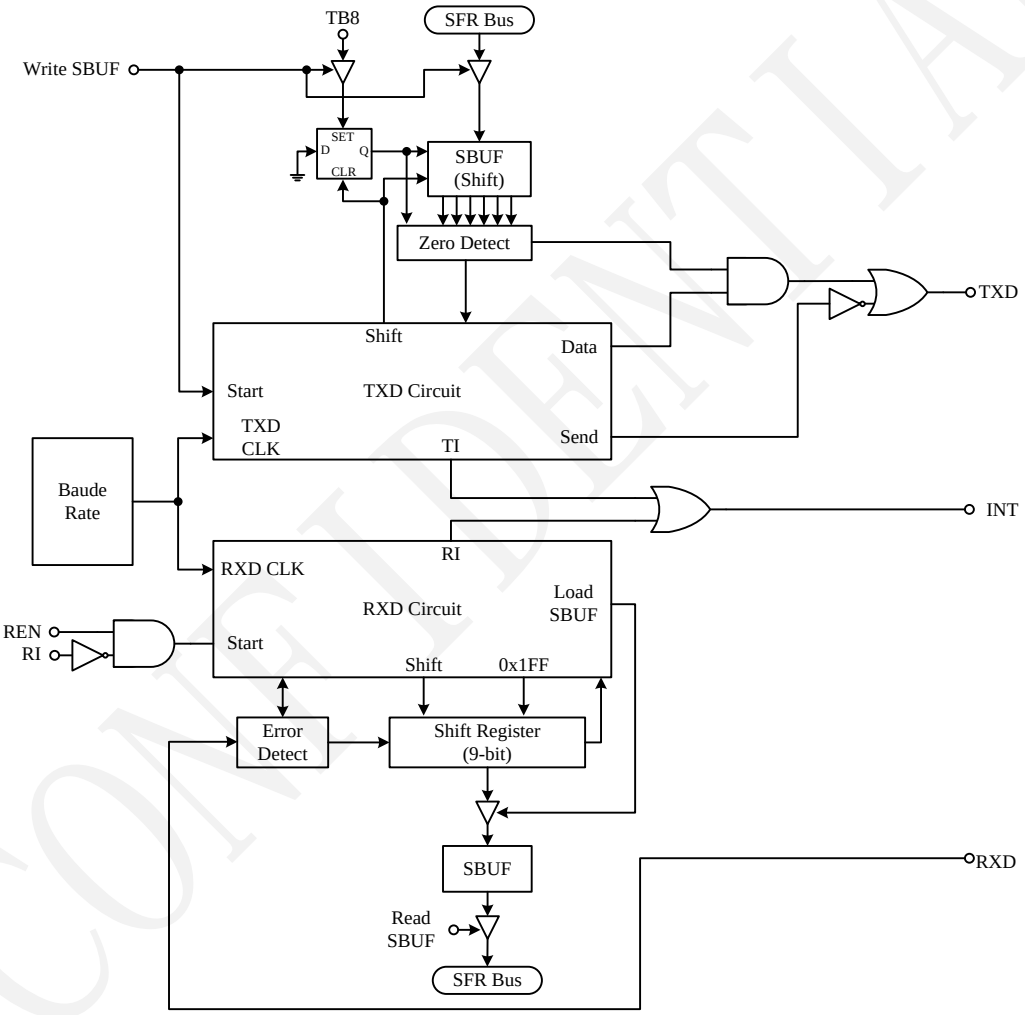


Diagram 14-1 TK18 UART Mode 0 diagram

- Mode 1: Baud rate is configured via SCON2 and SCON3 for both TX and RX. Diagram 14-2 shows the framework of TK18 UART serial port. To place the transmitted data into SBUF, eg “SBUF=0x12”, the write action of 0x12 into SBUF will happen at the second cycle of S6. Place “1” into Flip-flop on the left (the 9th bit) to be the recognition bit for ending transmission and be the signal to initiate TK controller. When TK controller sends output signal 1, TXD pin sends shift pulse and start to send data. Data in SBUF is sent in order through RXD pin and substitute by “0” from the left. When 8 bits are sent, only the far right bit is 1

and rests of the bits are 0. 0 detection circuit (which only detects the left seven bits) will detect signals 0 and drive TX controller. TX controller will immediately issue a TI interrupt and set output signal as 0 to stop transmission. In order to receive data, user needs to set REN bit of SCON register as 1, RI bit as 0 to initiate RX starting signal. RX controller will load “11111110” into shift register. The RX controller issues signal 1, then TXD pin will output shift pulse to start receiving data. When each serial data is sent via RxD pin to the input shift register, RX controller will issue a shift signal that moves the data in the input shift register to the left. When the far left bit is 0, RX will input another bit and issue a RI interrupt signal, and set receiving signal as 0 to stop receiving.



Daigram 14-2 Framework of TK18 Serial port

Under this mode, RXD of TK18 is connected to TXD of the source, and TK18 TXD is connected to the destination RXD. Under Mode 1, each data patch contains 10 bits, including start bit, 8-bits data and stop bit. The first bit is the low start bit, followed by 8-bits data. To send from bit 0 (LSB), followed by bit 7 (MSB), and then the high stop bit. As shown in diagram 14-3:

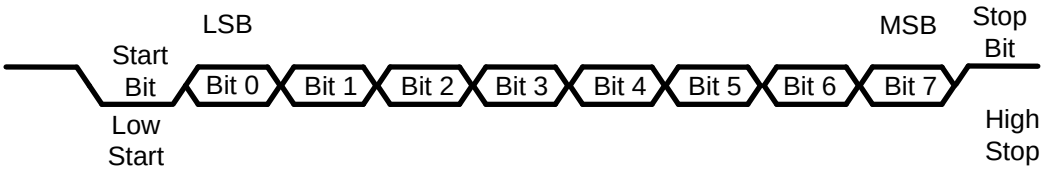


Diagram 14-3 TK18 Serial port Mode 1 data format diagram

- Mode 2: under this mode, Baud rate is decided by SCON2 and SCON3 registers and each data is composed of 11 bits including starting bit, 8 bits data, parity bit and stop bit. The first bit is the starting bit of low, followed by 8 bits data. Send from bit 0 (LSB), and the bit after bit 7 (MSB) is the High stop bit. As shown in Diagram 14-4, when data start transmitted, the 9th bit TB8 (TB8 in SCON register) is parity bit which can be retrieved from the P bit of PSW for the purpose of parity check. When receiving data, the 9th bit will go to RB8 of SCON register directly disregarding the stop bit.

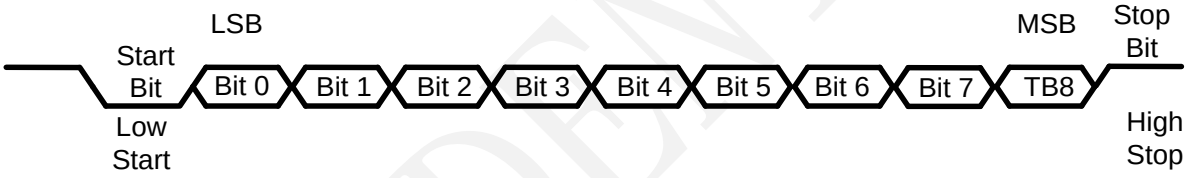


Diagram 14-4 TK18 Serial port Mode 2 data format diagram

14.3 Related Control Registers

TXD_MUX (F001H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	TXD_MUX: select a GPIO for TXD data output.					
Read/write	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0

bit7-6 Reserved

bit5-0 **TXD_MUX**: Select register for TXD channel of UART port communication (from 0 to 35)

000000: Select GPIO0 port as TXD channel output

000001: Select GPIO1 port as TXD channel output

: :

100000: Select GPIO32 port as TXD channel output (default)

: :

100011: Select GPIO35 port as TXD channel output

Others: Reserved

RXD_MUX (F00DH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	RXD_MUX: select a GPIO for RXD data input.					
Read/write	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	1

bit7-6 Reserved

bit5-0 **RXD_MUX**:Select register for RXD channel of UART port communication (from 0 to 35)

000000: Select GPIO0 port as RXD channel input

000001: Select GPIO1 port as RXD channel input

: :

100001: Select GPIO33 port as RXD channel input (default)

: :

100011: Select GPIO35 port as RXD channel input

Others: Reserved

SYSMISC (F010H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	TXCLKEN	TXEN	---	---	---	---
Read/write	---	---	R/W	R/W	---	---	---	---
Default	0	0	0	0	0	1	0	0

bit7-6 Reserved

bit5 **TXCLKEN**: TX clock source for UART mode 0

0: Disable (default)

1: Enable

bit4 **TXEN**: TX module operation
0: Disable (default)
1: Enable. Once this bit is set to "1", TXD port can begin operating.
Bit3-0 Reserved

SCON (98H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	SM1	SM1	---	REN	TB8	RB8	TI	RI
Read/write	R/W	R/W	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-6 **SM1~SM0**: UART operational mode
00: Mode 0, 8 bit shift register mode, and RX port clock frequency is system clock frequency.
01 : Mode 1, 8 bit serial port (variable Baud rate)
10 : Mode 2, 9 bit serial port
11: Mode 3, 9 bit serial port (variable Baud rate)
bit5 Reserved
bit4 **REN**: RX module operation
0: Disable (default)
1: Enable. Once this bit is set to "1", RXD port begins operating.
Bit3 **TB8**: 9th bit data sent by serial port Mode 2 and 3
0: Data 0
1: Data 1
bit2 **RB8**: 9th bit data received by serial port Mode 2 and 3
0: Data 0
1: Data 1
bit1 **TI**: Serial port transmitting TXD interrupt
This bit will not be automatically cleared after response only if this bit is set to "1".
0: Not occur
1: Occured
bit0 **RI:** Serial port receiving RXD interrupt
This bit will not be automatically cleared after response only if this bit is set to "1".
0: Not occur
1: Occured

SBUF (99H) Register

Byte number	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	SBUF							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **SBUF**: UART serial port data buffer zone

SCON2 (9AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	SCON2							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **SCON2**: Upper byte Baud rate configuration register

SCON3 (9BH) Register

Byte number	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	SCON3							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **SCON3**: Lower byte Baud Rate configuration register

Note: SCON2 and SCON3 compose 16 bit counter to configure Baude rate of UART in operationam Mode 2 & 3.

Since the clock source of Baude rate = F_{Sys}, the calculation method of SCON2 & SCON3 is as follows:

Assumed F_{SYS}=14MHz, it is expected to get the Baud rate of 115200, then

Baud Rate= 1 / T

T= (1/ F_{SYS}) * ({SCON2,SCON3} +1)

T= (71.43nS) * ({SCON2,SCON3} +1)

{SCON2,SCON3} +1= 1/ (115200 * 71.43)

{SCON2,SCON3} = 121，then SCON2= 00H，SCON3= 79H

SCON4 (9CH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	M10BR1	M10BR0
Read/write	---	---	---	---	---	---	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-4 Reserved

bit1-0 **SM10BR1~M10BR0**: Baude rate configuration of UART in operational Mode 0 & 1

00: Baude rate = F_{SYS}/2

01: Baude rate = F_{SYS}/4

10: Baude rate = F_{SYS}/8

11: Baude rate = F_{SYS}/16

15. I²C Interface

15.1 Overview

TK18 provides 1 channel communication connectivity for standard I²C bus slave with SCL and SDA port. In transmission speed, they support both 100KHz in Standard Mode and 400KHz in Fast Most. Please refer to Diagram 15-1 for standard application connection of bus.

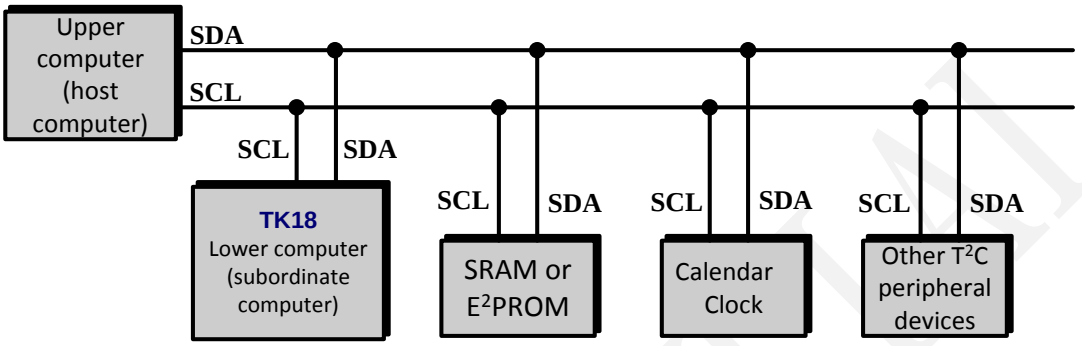


Diagram 15-1: TK18 I²C Slave Application

Note: Although package below LQFP44 will include neither SCL nor SDA pins, user can still map functions of these pins to any GPIO port through I2CCLK_MUX and I2CDAT_MUX registers. **(Caution: SCL and SDA cannot be configured together.)**

15.2 Block Diagram

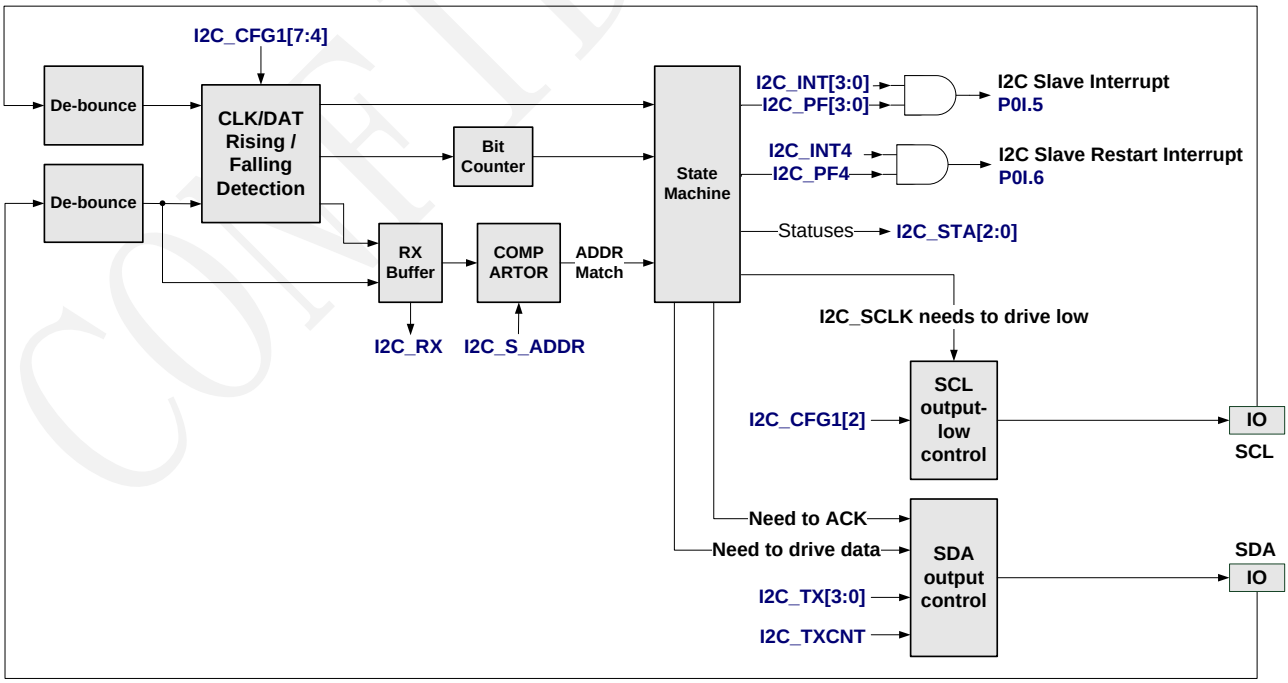


Diagram 15-2: TK18 I²C slave Module Block Diagram

15.3 Related Control Registers

I2CCLK_MUX (F040H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	I2CCLK_IO: select a GPIO for SCL input.					
Read/write	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	0

bit7-6 Reserved

bit5-0 **I2CCLK_IO**: Select register through I^{2}C clock SCL channel mapping (0~35)

000000: Select GPIO0 for SCL input
000001: Select GPIO1 for SCL input
: :
100000: Select GPIO32 for SCL input (default)
: :
100011: Select GPIO35 for SCL input
Others: Reserved

I2CDAT_MUX (F041H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	I2CDAT_IO: select a GPIO for SDA input.					
Read/write	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	1	0	0	0	0	1

bit7-6 Reserved

bit5-0 **I2CDAT_IO**: Select register through I^{2}C data SDA channel mapping (0~35)

000000: Select GPIO0 for SDA input
000001: Select GPIO1 for SDA input
: :
100001: Select GPIO33 for SDA input (default)
: :
100011: Select GPIO35 for SDA input
Others: Reserved

I2C_S_ADDR (F002H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2CS_ADDR: I2S device address							I2CRW
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/-
Default	1	0	0	0	0	0	0	0

bit7-1 **I2C_S_ADDR**: I^{2}C slave devices and ISP SMB bus address register (default: 1000000)

bit0 **I2CRW**: I^{2}C bus R/W

0: Write
1: Read

I2C_S_CTRL (F003H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	I2CSEN	ISPEN	---	---	---	---
Read/Write	---	---	R/W	R/W	---	---	---	---
Default	0	0	0	1	0	1	0	1

bit7-6 Reserved

bit5 **I2CSEN**: I^2C slave devices
0: Disable (default)
1: Enable

bit4 **ISPEN**: SMB bus slave devices for ISP communication
0: Disable
1: Enable (default)

bit3-0 Reserved

I2C_CFG1 (F780H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	NACKI	SCLS	ADDCP	---
Read/write	---	---	---	---	R/W	R/W	R/W	---
Default	0	0	0	0	0	0	0	0

bit7-4 Reserved

bit3 **NACKI**: In Standard Mode, interrupt on receiving NACK
0: Disable (default)
1: Enable

bit2 **SCLS**: I^2C slave mode selection
0: Standard mode (default)
1: Fast mode

bit1 **ADDCP**: I^2C slave device address compare function
0: Disable (default), F/W need compare address by self.
1: Enable

bit0 Reserved

I2C_CFG2 (F781H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	REVST	REVSP	BSDASTIM: Setup time for SDA output in busy mode					
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **REVST**: Select action upon receiving Start signal
0: Turn-around Mode (default)
1: Current state

bit6 **REVSP**: Select action upon receiving Stop signal
0: Turn-around Mode (default)
1: Current state

bit5-0 **BSDASTIM**: In I²C standard mode set up time register for SDA output
000000: 1 system clock F_{SYS}
000001: 2 system clock F_{SYS}
: :
111111: 64 system clock F_{SYS}

I2C_INT (782H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	RSI	STI	ASI	NSI	DNI
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved
bit4 **RSI**: I²C restart interrupt
0: Disable (default)
1: Enable
bit3 **STI**: I²C start interrupt
0: Disable (default)
1: Enable
bit2 **ASI**: I²C abnormal interrupt
0: Disable (default)
1: Enable
bit1 **NSI**: I²C normal stop
0: Disable (default)
1: Enable
bit0 **DNI**: I²C data finish interrupt
0: Disable (default)
1: Enable

I2C_PF (F783H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	RSIF	STIF	ASIF	NSIF	DNIF
Read/write	---	---	---	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 5 Rserved
bit4 **RSIF**: I²C restart interrupt. Once this bit is set to “1”, it can be cleared.
0: Disable (default)
1: Enable
bit3 **STIF**: I²C start interrupt. Once this bit is set to “1”, it can be cleared.
0: Disable (default)
1: Enable
bit2 **ASIF**: I²C abnormal interrupt. Once this bit is set to “1”, it can be cleared.
0: Disable (default)
1: Enable

bit1 **NSIF**: I2C normal stop interrupt. Once this bit is set to "1", it can be cleared.
0: Disable (default)
1: Enable

bit0 **DNIF**: I^2C data finish interrupt. Once this bit is set to "1", it can be cleared.
0: Disable (default)
1: Enable

I2C_STA (F784H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	ACKF	STPF	STRF
Read/write	---	---	---	---	---	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7 – 3 Rserved

bit2 **ACKF**: I^2C slave device acknowledgement signal flag
0: ACK
1: NACK

bit1 **STPF**: I^2C slave device stop condition flag
0: Normal (default)
1: Once stop condition occurs, this bit will be automatically cleared before next start condition occurs.

Bit0 **STRF**: I^2C slave device start condition flag
0: Normal (default)
1: Once stop condition occurs, this bit will be automatically cleared before next stop condition occurs.

I2C_SCR (F785H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	IDLE	---	---	---	---	DR	NDE	SACK
Read/write	R/W	---	---	---	---	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **IDLE**: I^2C slave device forced idling enable
0: Disable (default)
1: Enable

bit6 – 3 Reserved

bit2 **DR**: Data direction control, if ADDCP = 0 DR bit =0 or 1 need I2CRW bit status to set it
0: RX (default), host is write status
1: TX (effective in standard mode), host is read status

bit1 **NDE**: Data effectiveness control
0: Ineffective data (default)
1: Effective data

bit0 **SACK:** Slave acknowledgement control
0: ACK
1: NACK

I2C_RX (F786H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2C_RX: I2C slave receive data							
Read/write	R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **I2C_RX**: I^2C slave receive data register

I2C_TX0 (F787H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2C_TX0: I2C slave transmit data byte0							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
default	0	0	0	0	0	0	0	0

bit7-0 **I2C_TX0**: I2C slave transmit data byte0 register

I2C_TX1 (F788H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2C_TX1: I2C slave transmit data byte1							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **I2C_TX1:** I2C slave transmit data byte1 register

I2C_TX2 (F789H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2C_TX2: I2C slave transmit data byte2							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **I2C_TX2**: I2C slave transmit data byte2 register

I2C_TX3 (F78AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2C_TX3: I2C slave transmit data byte3							
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-0 **I2C_TX3**: I2C slave transmit data byte3 register

I2C_TXCNT (F78BH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	I2CTX1	I2CTX0
Read/write	---	---	---	---	---	---	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 2 Rserved

bit1-0 **I2CTX1~I2CTX0**: I^2C slave transmit byte counter

00: Transmit I2C_TX0 (byte0) data (default)

01: Transmit I2C_TX1 (byte1) data (default)

10: Transmit I2C_TX2 (byte2) data (default)

11: Transmit I2C_TX3 (byte3) data (default)

Note: When TK18 I^2C slave runs in Fast Mode, if slave is busy, it will pull SCL voltage to low level until busy mode relieved. This slave operation is mainly to inform master to delay communication preventing slave from missing any data; Above description is defined as "clock extending" in "I2C-Bus Specification" (TK18 is fully compatible with this spec). The I2C master has to support "clock extending" if operates in Fast Mode. Otherwise, unexpected abnormal conditions may occur.

16. ADC

16.1 Overview

TK18 provides up to 6 channels 10-bit ADC with ports of AD0, AD1, AD2, AD3, AD4 and AD5. User can apply procedure query or interrupt to process data converted by ADC.

Note: Since ADC eference voltage is VCC, if it is concerned that VCC fluctuation many cause instability in ADC converted data, user can average each converted data through running procedure.

16.2 Block Diagram

Simulation input channel of TK18 ADC shares the same sample and hold circuit. Output of Sample and hold circuit is connected to the input end of ADC. ADC adopts successive approximation method to produce a 10 bits binary result, and save in the ADC registers (ADC_DAT0 and ADC-DAT1). Each of the 6 channels is able to input independent analog signal, but only one channel can be activated at a time.

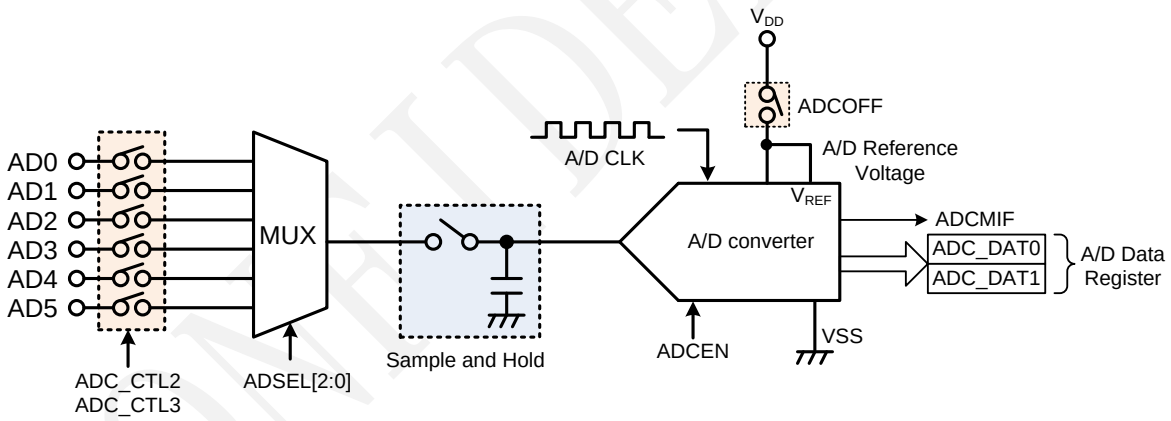


Diagram 16-1 Framework of TK18 ADC module

ADCEN signals control analog conversion, ADCMIF indicates the conversion is completed. Configure the ADCMIF bit from ADC_CTL1 register to issue an interrupt (if ADC interrupt is permitted).

Diagram 16-2 is the block diagram of TK18 A/D, configuration instructions are:

1. Configure ADC_CTL2 ~ ADC_CTL3, to decide which channels are for conversion
2. Condigure ADSEL[2:0] to decide the priority of channels for conversion
3. Set ADCOFF = ADCINI = ADCMI =1
4. Set ADCEN =1, A/D starts to convert
5. ADCMIF-1 indicates the completion of conversion, user can read the data from ADC_DAT0 & ADC_DAT1.

16.3 Related Control Registers

ADC_CTL1 (F035H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	ADWC3	ADWC2	ADWC1	ADWC0	---	ADCOFF	ADCINI	ADCMI
Read/write	R/W	R/W	R/W	R/W	---	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7-4 **ADWC3~ADWC0**: Delay time from ADC hardware module enable to sampling
0000: Delay time is 0 ADC clock (default)
0001: 1 system clock (F_{SYS}) delay time
: :
1111: 15 system clock (F_{SYS}) delay time

bit3 Reserved

bit2 **ADCOFF**: ADC hardware module power off
0: ADC hardware module power on (default)
1: ADC hardware module power off

bit1 **ADCINI**: ADC hardware module power on and initialize
0: ADC hardware module power on (default)
1: ADC hardware module power off

bit0 **ADCMI**: ADC hardware module interrupt
To ensure that ADC Occureds for interrupt on finishing converting operation and interrupt responds successfully, both ADCI bit and this hardware module interrupt enable bit have to be set to “1” beforehand. Otherwise, interrupt cann’t respond.
0: Disable (default)
1: Enable

ADC_CTL2 (F036H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	AD3EN	AD2EN	AD1EN	AD0EN	ADSEL2	ADSEL1	ADSEL0	ADCEN
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 **AD3EN**: AD3 channel
0: Disable (default)
1: Enable

bit6 **AD2EN**: AD2 channel
0: Disable (default)
1: Enable

bit5 **AD1EN**: AD1 channel
0: Disable (default)
1: Enable

bit4 **AD0EN**: AD0 channel
0: Disable (default)
1: Enable

bit3-1 **ADSEL2~ADSEL0**: ADC chanlel selection register
000: 0 select AD0 for channel (default)
001: 1 select AD1 for channel
010: 2 select AD2 for channel
011: 3 select AD3 for channel
100: 4 select AD4 for channel
101: 5 select AD5 for channel
Others: Reserved

bit0 **ADCEN**: ADC hardware module sampling
Once ADC channel is configured and started, and module is powered, this bit needs to be set to "1" before ADC begins to sample analog data.
0: Disable (default)
1: Enable, ADC begins to sample analog data

ADC_PF (F037H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	---	ADCMIF
Read/write	---	---	---	---	---	---	---	R/W
Default	0	0	0	0	0	0	0	0

bit7 – 1 Rserved

bit0 **ADCMIF**: ADC hardware module interrupt. Once this bit is set to "1", it can be cleared.
0: Not trigger
1: Trigger

ADC_DAT0 (F038H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	---	---	---	ADCD9	ADCD8
Read/write	---	---	---	---	---	---	R/-	R/-
Default	0	0	0	0	0	0	0	0

bit7 – 2 Rserved

bit1-0 **ADCD9~ADCD8**: ADC upper bit data register for 9~8 bit sampled data

ADC_DAT1 (F039H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	ADCD7	ADCD6	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
Read/write	R/-	R/-	R/-	R/-	R/-	R/-	R/W	R/-
Default	0	0	0	0	0	0	0	0

bit7-0 **ADCD7~ADCD0**: ADC lower bit data register for 7~0 bit sampled data

ADC_CTL3 (F03AH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	---	CHEN	---	---	AD5EN	AD4EN
Read/write	---	---	---	R/W	---	---	R/W	R/W
Default	0	0	0	1	0	0	0	0

bit7 – 2 Rserved

bit4 **CHEN**: AD all channel enable bit
0: Disable
1: Enable (default)

bit1 **AD5EN**: AD5 channel
0: Disable (default)
1: Enable

bit0 **AD4EN**: AD4 channel
0: Disable (default)
1: Enable

17. Electronic Characteristics

17.1 Absolute Rating

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Operating Temperature	-40	--	85	℃
T_{STG}	Storage Temperature	-55	--	125	℃
VCC	DC Power Voltage	2.7	---	6.0	V
GND	Power Ground	-0.3	0	0.3	V
IDD	Max. IDD	---	---	200	mA
ESD	Human Body Mode	--	--	8K	V
EFT	--	--	--	4K	V
CS	--	--	--	10	V

17.2 Normal Operating Range

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Working Environment Temperature	-40	25	85	℃
VCC	DC Power Voltage	4.5	5.0	5.5	V
V_{IH1}	Input High Voltage	0.7VCC	--	VCC	V
V_{IH2}	Input Low Voltage	0	--	0.3VCC	V

17.3 DC Characteristics (TA=25℃, LIRC= 32KHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC	Operating Voltage	--	2.7	--	5.5V	V
V_{POR}	Reset Voltage	--	1.9	2.1	2.3	V
I_{OP1}	Operating Current @Normal Mode (F_{SYS} = 14 MHz, all ADC disable)	VCC = 5.0V	--	4.0	6.0	mA
		VCC = 3.3V	--	3.0	4.5	
R_{PH1}	Port Pull-up Resistor (PUEN = 4.7KΩ)	VCC = 5.0V	1.8	3.0	4.0	KΩ
		VCC = 3.3V	2.7	4.5	6.3	
R_{PH2}	Port Pull-up Resistor (PUEN = 40KΩ)	VCC = 5.0V	15.9	26.5	37.2	KΩ
		VCC = 3.3V	25.0	41.8	58.5	
I_{std}	Standby Current @Sleep Mode (I/O noload, F_{SYS} stop)	VCC = 5.0V	--	150	180	μA
		VCC = 3.3V	--	100	150	

(Continuance 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL1}	Input Low Voltage	VCC = 5.0V	-0.3	--	2.1	V
		VCC = 3.3V	-0.3	--	1.1	
V_{IH2}	Input High Voltage	VCC = 5.0V	--	3.49	5.3	V
		VCC = 3.3V	--	2.17	3.6	
I_{OL1}	GPIO & COM Port Sink Current (turn off GPIO strong drive)	VCC = 5.0V, VOL = 0.7V	11.2	14	16.8	mA
		VCC = 3.3V VOL = 0.7V	8	10	12	
		VCC = 5.0V VOL = 0.4V	6.4	8	9.6	
		VCC = 3.3V VOL = 0.4V	4.8	6	7.2	
I_{OH1}	GPIO & SEG Port Source Current (turn off GPIO strong drive)	VCC = 5.0V VOH = 4.5V	4	5	6	mA
		VCC = 3.3V VOH = 2.8V	3.2	4	4.8	
I_{OL2}	GPIO port & COM6 Sink Current (turn on GPIO strong drive)	VCC = 5.0V VOL = 0.7V	32	40	48	mA
		VCC = 3.3V VOL = 0.7V	28	35	42	
		VCC = 5.0V VOL = 0.4V	20	25	30	
		VCC = 3.3V VOL = 0.4V	17.6	22	26.4	
I_{OH2}	GPIO Port Source Current (turn on GPIO strong drive)	VCC = 5.0V VOH = 4.5V	15.2	19	22.8	mA
		VCC = 3.3V VOH = 2.8V	10.4	13	15.6	mA
I_{OL3}	COM0-COM5 Port Sink Current (turn on GPIO strong drive)	VCC = 5.0V VOL = 0.4V	117	146	175	mA
I_{OH3}	SEG0-SEG7 Port Source Current (turn on GPIO strong drive)	VCC = 5.0V VOH = 4.5V	21.6	27	32.4	mA

17.4 AC Characteristics (TA = -40 ~ 85℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{HOSC}	HIRC oscillator frequency	VCC = 4.5 ~ 5.5V	27.2	28.0	28.8	MHz
T_{SYSCLK}	Oscillator Startup Time	VCC = 5V F_{SYS} = 14MHz	--	--	1.5	µs

17.5 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADI}	Supply Voltage		3.0	-	5.5	V
V_{AIN}	ADC Input Voltage	VCC= 5V	0.2	-	VCC-0.2	V
R_{ADC}	Accuracy	VCC= 5V	-	10	-	bit
D_{NL}	Differential Non-linear Error	VCC= 5V	-2	-	2	LSB
I_{NL}	Integral Non-linear Error	VCC= 5V	-8	-	8	LSB
E_{ADC}	Total Absolute Error	VCC= 5V	-8	-	8	LSB
I_{ADC1}	ADC Operation Current1	VCC= 5V, ADCCLK = 1MHz	-	-	1.5	mA
I_{ADC2}	ADC Operation Current2	VCC= 3V, ADCCLK = 1MHz	-	-	1.0	mA
T_{ADC}	ADC Conversion Time	ADCCLK = 1MHz	-	-	15	µS

17.6 I^2C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
---	I^2C Slave Bus Speed	-	100K	-	400K	b/s
t_{HDSTR}	Repeated Startup Condition Holding Time	4.0	-	0.6	-	µS
t_{LOW}	SCL Low Level Cycle	4.7	-	1.3	-	µS
t_{HIGH}	SCL High Level Cycle	4.0	-	0.6	-	µS
t_{HDDAT}	Data Hold Time	0	3.45	0	0.9	µS
t_{SUDAT}	Data Setup Time	250	-	100	-	nS
t_{SUSTP}	Stop Condition Setup Time	4.0	-	0.6	-	µS
t_{BUF}	Idle Time between Stop and Startup Condition	4.7	-	1.3	-	µS
t_R	SCL & SDA Signal Rising Time	-	1	-	0.3	µS
t_F	SCL & SDA Signal Falling Time	-	0.3	-	0.3	µS

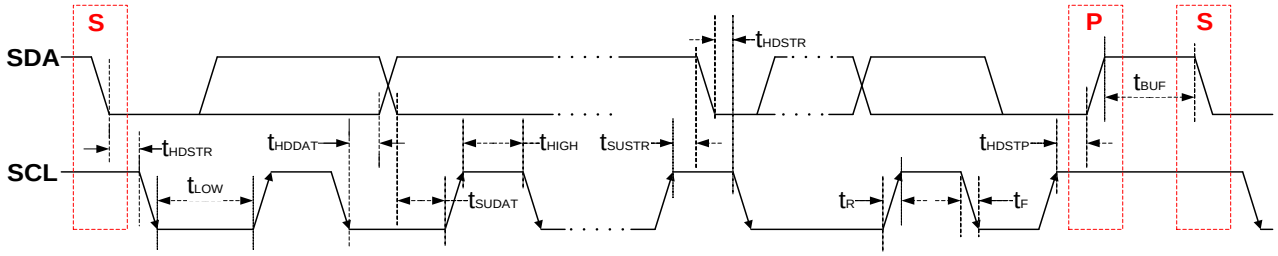


Diagram17-1 I²C sequence

17.7 EEPROM (Data Flash) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
DF_{SIZE}	Data Flash Capacity	--	128	--	Bytes
	Data retention	--	10	--	Years
t_{WR}	Write Cycle (Note 1)	2.2	-	6	mS
N_{END}	Erase Life Span (Note 2)	100K	-	6.4M	Write Cycles

Note 1: It's the needed write cycle whenever X-LIB flash write API functin is called.

Note 2: Erase life span is related with the used data flash size DF_{USE}, and its calculation formula is as follows:

$\mathbf{N_{END}}$= [(DF_{SIZE}) / (DF_{USE}+1)] * 100K

(if 63 ＜ DF_{USE} ＜ DF_{SIZE}，then $\mathbf{N_{END}}$= 100K)

Assumed DF_{USE}= 1 byte in the project, the erase life span $\mathbf{N_{END}}$ is as follows:

$\mathbf{N_{END}}$= [(128) / (1+1)] * 100K= 6.4M write cycles

17.8 Power-on Reset Characteristics (TA=25℃, VCC = 5V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PORS}	Reset Voltage	-	1.9	2.1	2.3	V
T_{POR_MIN}	Power-on Low Level Time after Power-off	F_{SYS} = 14MHz	1.0	-	-	mS
T_{POR_RST}	Conversion Time for Reeset to Normal Operating Mode	F_{SYS} = 14MHz	250	-	-	mS

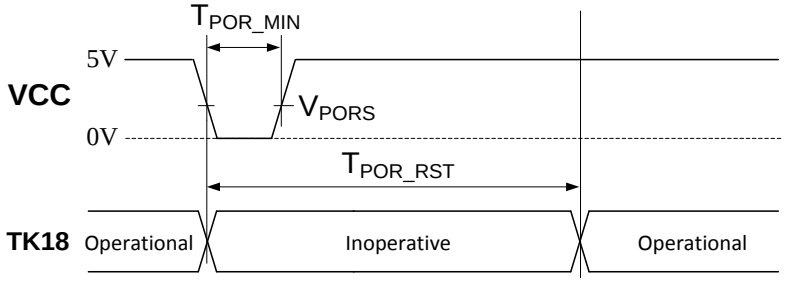
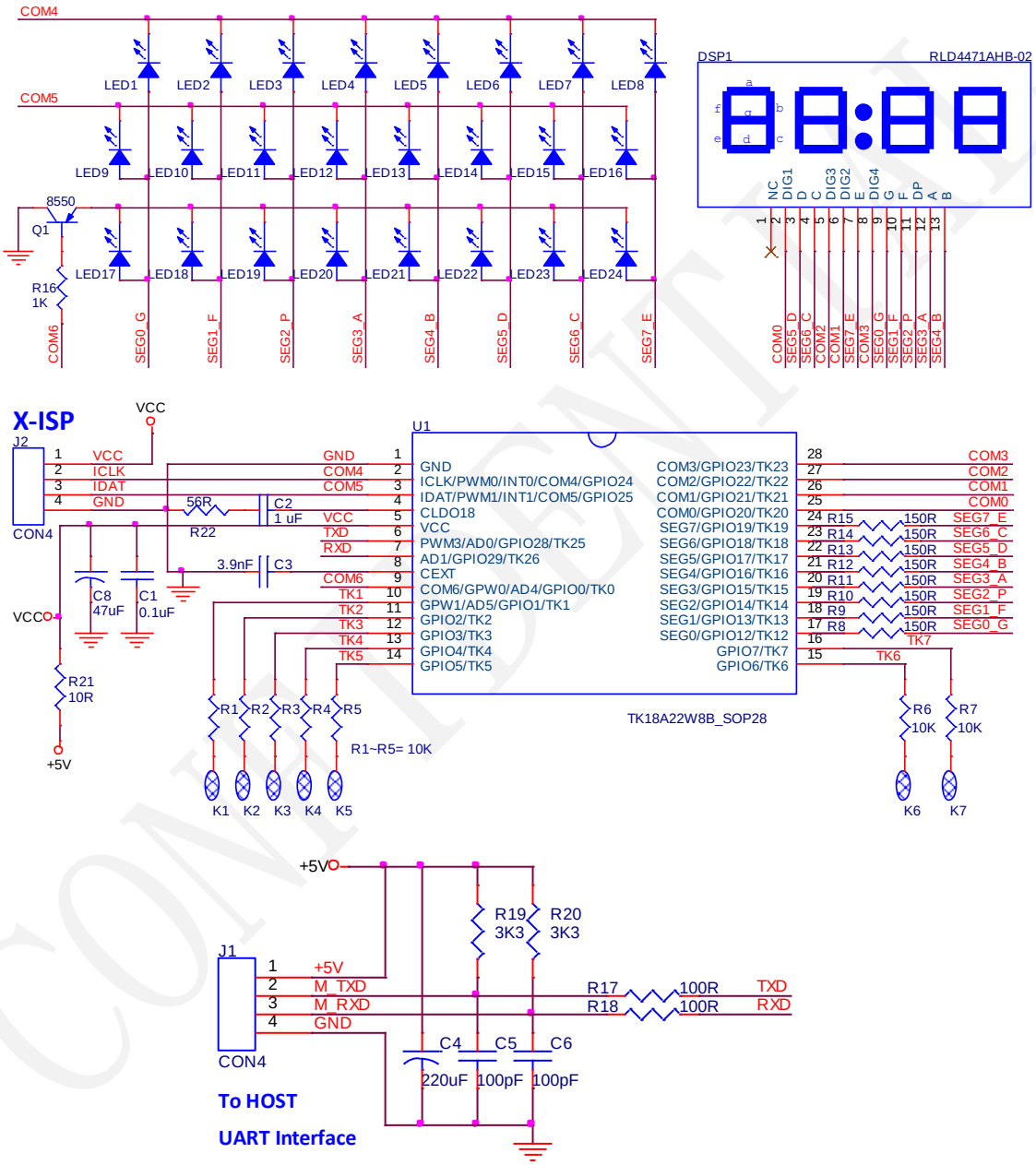


Diagram 17-2: Reset Sequence

18. Application Circuits

18.1 Reference Applicaiton Circuits

The following application is that TK18A22 28SOP communicate as slave with master through UART TXD/RXD. Slave functions include: UART, 7TK, 7COM x 8SEG LED drive.



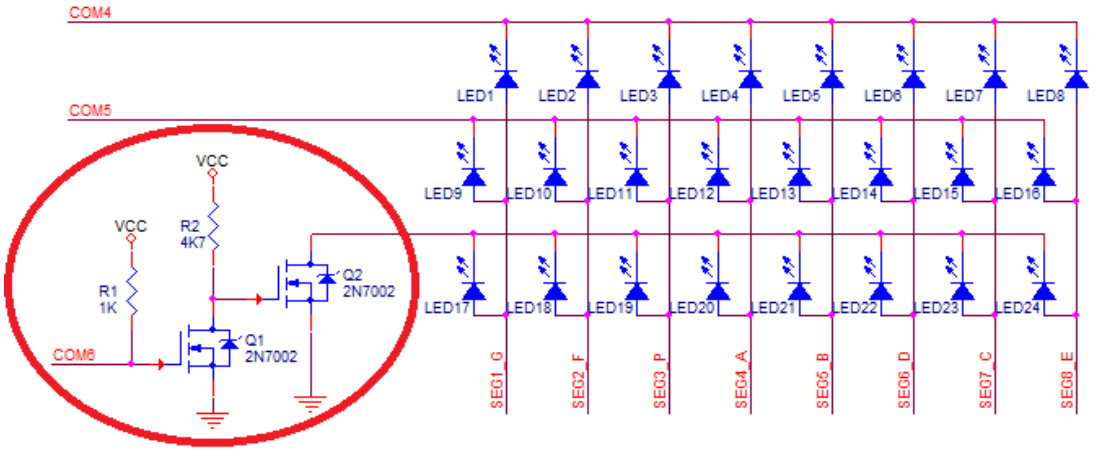
Note: J2 is used to connect with **X-ISP** debugging tools and doesn't belong to this project functions. However, it shall reserve soldering pad for future debugging.

18.2 Circuit Elements Parameters

Component	Range	Suggested Value	Description
R1~R7	3.3K~10KΩ	10KΩ	TK1~TK7 TK protective resistor. The larger the resistance is, the higher the anti-interference capability will be (however, sensitivity will be reduced comparatively). User can select this resistor based on actual needs.
R8~R15	0~330Ω	150Ω	SEG driving current-limiting resistance. User can select this value based on actual luminance requirements. However, since SEG current is not permanent, user shall be aware of non-uniform LED luminance when no current-limiting resistor is applied (0Ω).
R16	1KΩ	1KΩ	Q1 current-limiting resistor
R17~R18	0~1KΩ	100Ω	Serial port communication pin current-limiting protective resistor. User can select the resistance based on actual communicational speed.
R19~R20	3.3K~10KΩ	3.3KΩ	Serial port communication pin pull-up resistor. User can select this resistance based on actual communication speed.
R21	0~10Ω	10Ω	Chip input current-limiting protective resistor
R22	0~100Ω	56Ω	High anti-interference capability require.
C1	0.1μF	0.1μF	Chip filter capacitor (chip capacitor available)
C2	1μF	1μF	Chip internal 1.8V regulator capacitor (chip capacitor available)
C3	3.9nF	3.9nF	Reference capacitor input pin (**it shall be chip capacitor made of 10% high-accuracy NPO or X7R.**)
C4	100~220μF	220μF	Input power regulator electrolytic capacitor
C5~C6	100~470pF	100pF	Serial port communication pin filter capacitor (chip capacitor available). User can select this capacitance based on actual communication speed.
C7	22~47μF	47μF	Chip power regulator electrolytic capacitor
Q1	8550/PNP	8550	COM6 triode driver

Note: 1. The above reference circuit is used where high anti-interference capability is required. If user doesn't ask for high anti-interference capability, it is recommended to use 3.3KΩ R1~R7, R17/R18/R21 without connecting to short-circuit and save C5~C7.

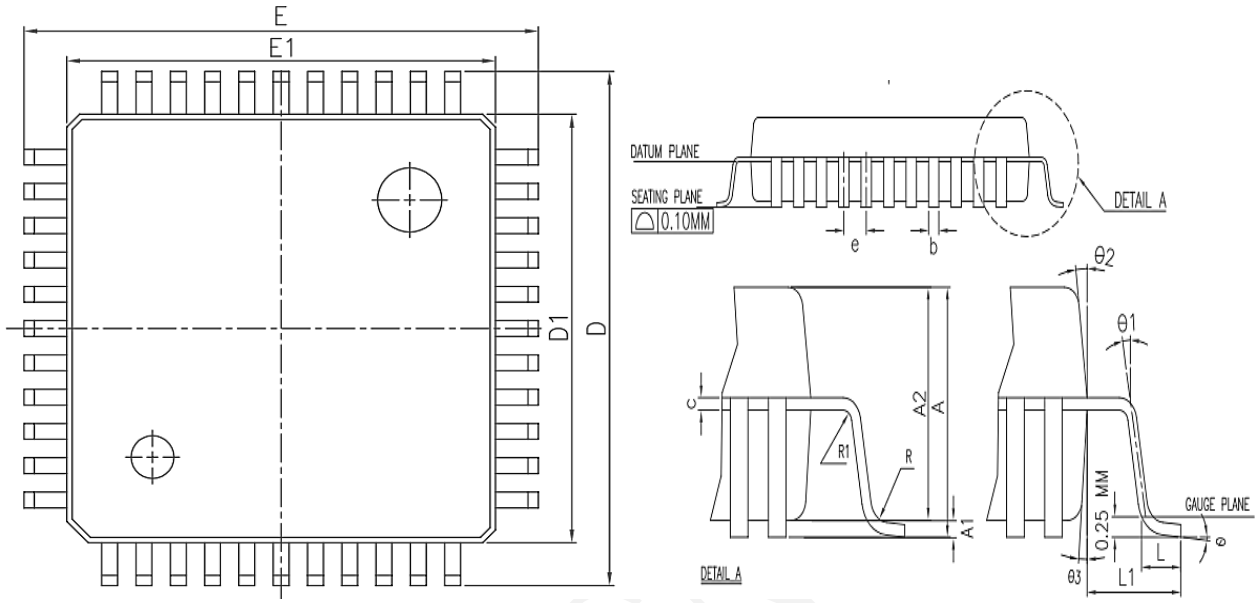
2. Since COM6 doesn't have high-current driving capability, a PNP triode driver is required. Although being cheap, triode will produce comparatively large voltage difference (V_{EC}) in conducting. If user wants to prevent it from affecting COM6-driving LED luminance, please refer to the connection in the following red circle,that is, use 2 N-MOSs for improvement.



19. Packaging Information

19.1 Dimensions

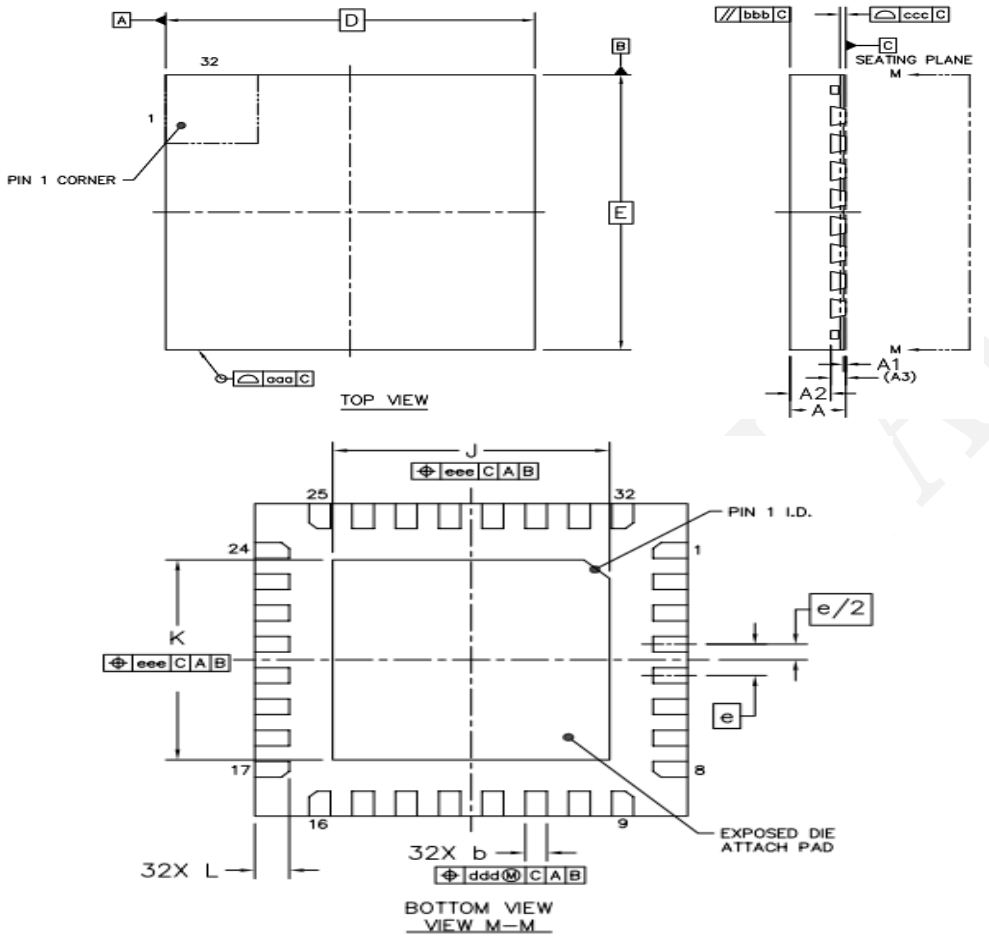
44-LQFP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.09	---	0.16	0.004	---	0.006
e	0.80 BASIC			0.031 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	---	---	0.003	---	---
R	0.08	---	0.20	0.003	---	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ	0°	---	---	0°	---	---
θ	11°	12°	13°	11°	12°	13°
θ	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BCB)					

Diagram 19-1: 44-LQFP Dimensions

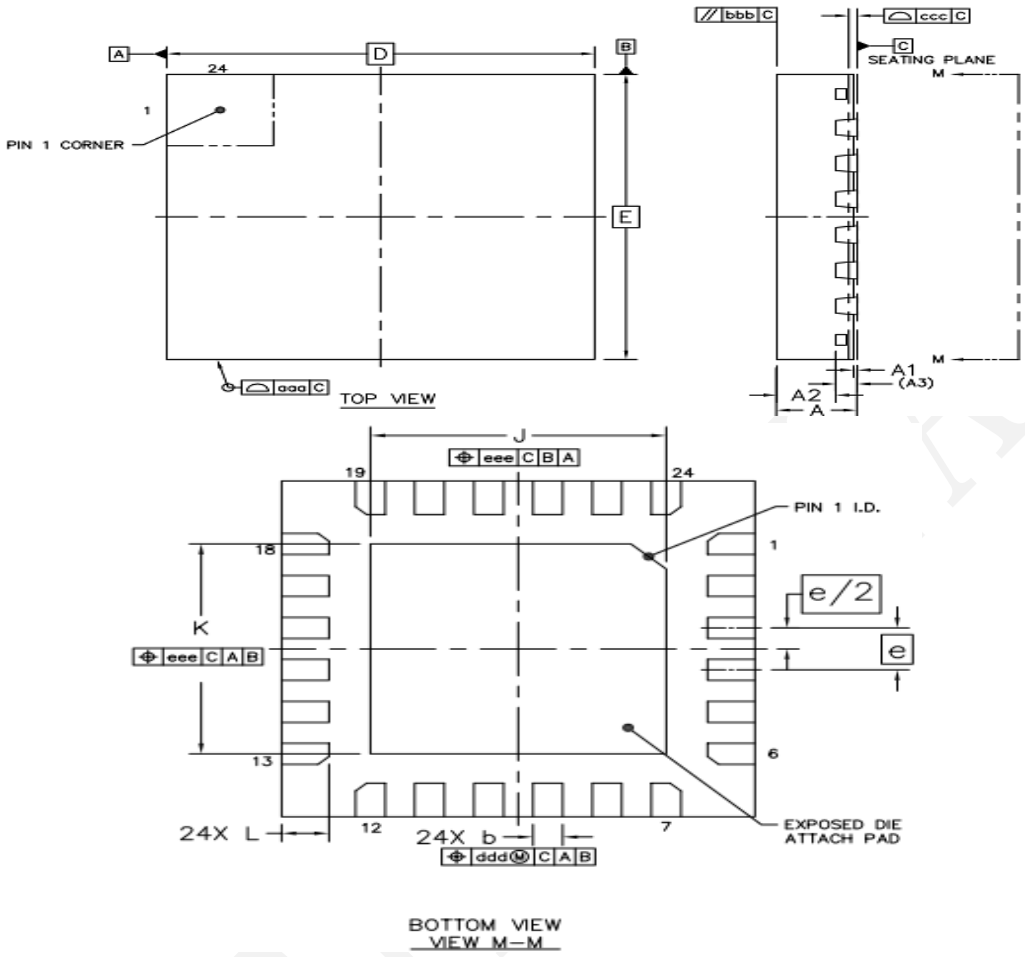
32-QFN



		SYMBOL	DIMENSION IN MM		
			MIN.	NOM.	MAX.
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	5 BASIC		
	Y	E	5 BASIC		
LEAD PITCH		e	0.5 BASIC		
EP SIZE	X	J	3.1	3.2	3.3
	Y	K	3.1	3.2	3.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

Diagram 19-2: 32-QFN Dimensions

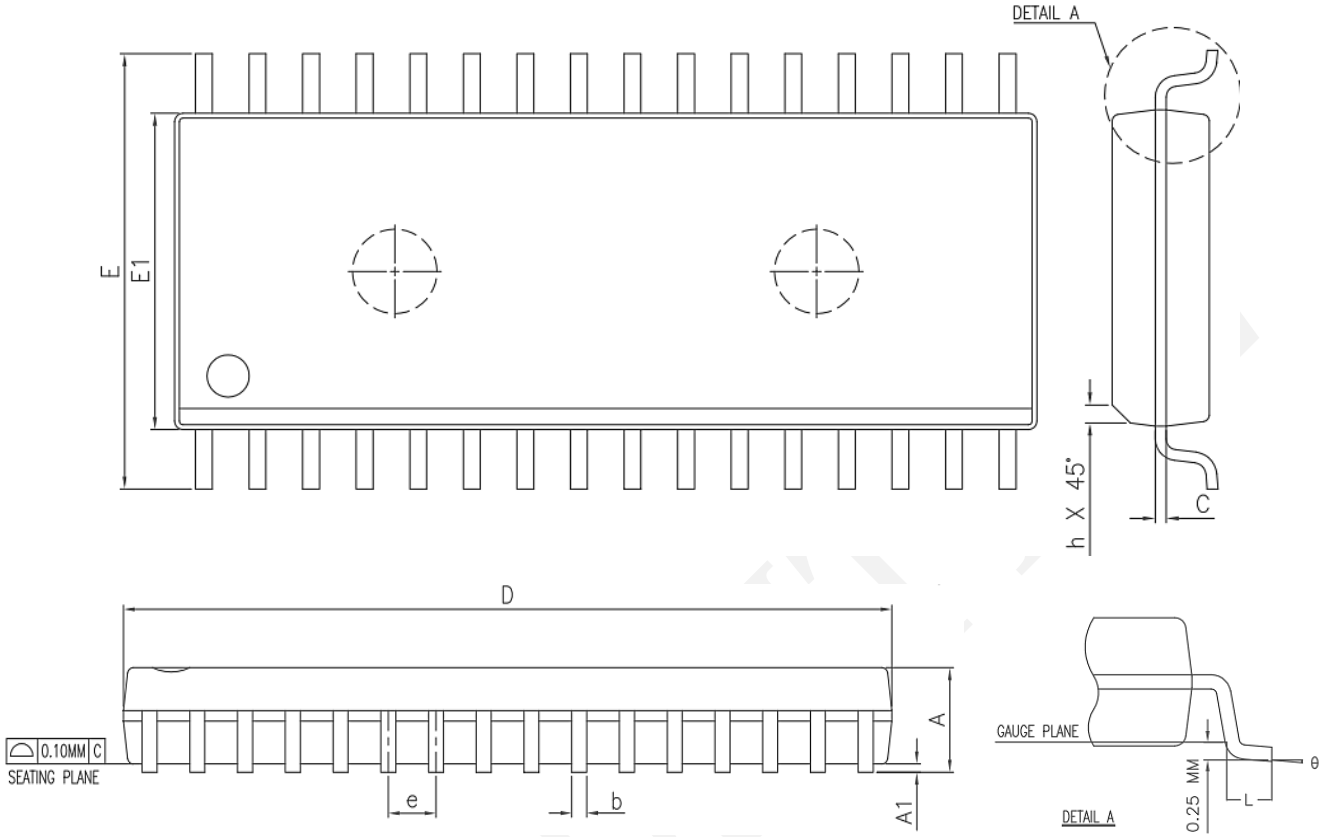
24-QFN



		SYMBOL	DIMENSION IN MM		
			MIN.	NOM.	MAX.
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BASIC	
	Y	E		4 BASIC	
LEAD PITCH		e		0.5 BASIC	
EP SIZE	X	J	2.4	2.5	2.6
	Y	K	2.4	2.5	2.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Diagram 19-3: 24-QFN Dimensions

20/24/28/32-SOP(300mil)

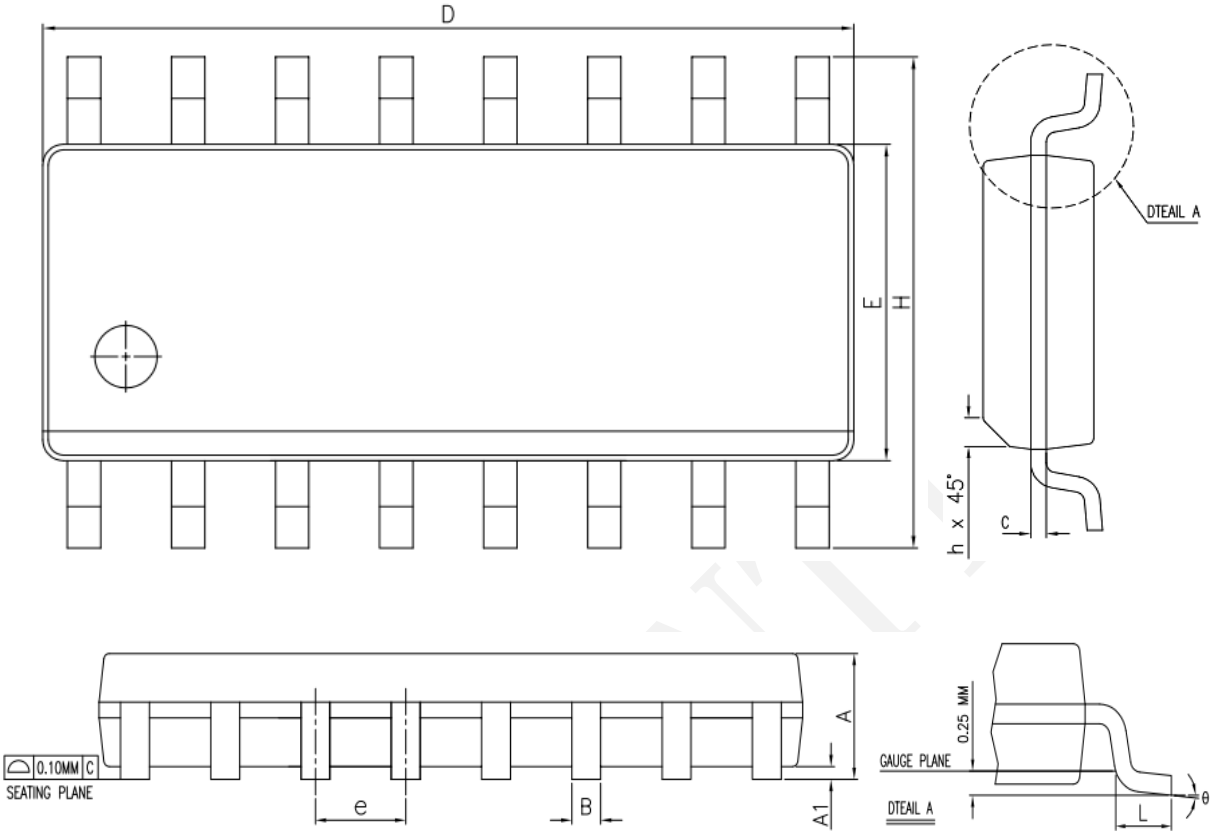


SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.0091	0.0125
e	1.27 BSC		0.050 BSC	
E1	7.40	7.60	0.2914	0.2992
E	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

N	D DIMENSION IN MM		D DIMENSION IN INCH		JEDEC
	MIN.	MAX.	MIN.	MAX.	
20	12.60	13.00	0.4961	0.5118	MS-013(AC)
24	15.20	15.60	0.5985	0.6141	MS-013(AD)
28	17.70	18.10	0.6969	0.7125	MS-013(AE)
32	20.32	20.73	0.8000	0.8160	MS-013

Diagram 19-4: 32-SOP Dimensions

16-NSOP(150mil)



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
e	1.27 BASIC		0.050 BASIC	
D	9.80	10.00	0.3859	0.3937
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.0160	0.0500
h	0.25	0.50	0.0099	0.0196
θ	0°	8°	0°	8°
JEDEC	MS-012(AC)			

Diagram 19-5: 16-NSOP Dimensions

19.2 Manual Soldering Temperature Limitations

Part Number	Package	Typical Soldering Temperature and Duration
TK18A26W2B	SOP32	350℃, 3~5sec
TK18A22W8B	SOP28	
TK18A18W4B	SOP24	
TK18A14W0B	SOP20	
TK18A28Q4B	LQFP44	350℃, 3~5sec
TK18A26U2B	QFN32	285℃, 3~5sec
TK18A18U4B	QFN24	
TK18A10W6B	NSOP16	350℃, 3~5sec

19.3 Part Number Descriptions

Part Number	Package Size	Lead Free Process	Status
TK18A26W2B	32-SOP 300mil	Lead Free	Mass Production
TK18A22W8B	28-SOP 300mil		
TK18A18W4B	24-SOP 300mil		
TK18A14W0B	20-SOP 300mil		
TK18A28Q4B	44-LQFP 10mm x 10mm x 1.6mm		
TK18A26U2B	32-QFN 5mm x 5mm x 0.75mm		
TK18A18U4B	24-QFN 4mm x 4mm x 0.75mm		
TK18A10W6B	16-NSOP 150mil		

19.4 Processing Technique Data

No.	Process Requirements	Note				
1	Materials and surface coating of elements and tubes	Tin				
2	Base materials and CTE of elements	Package	Molding compound		Conductive adhesive		Unit
			C1	C2	C1	C2	
		LQFP44	9	35	50	130	ppm/℃
		QFN32	9	35	80	200	
		SOP32	9	35	50	130	
		SOP28	8	32	80	200	
		QFN24	9	35	80	200	
		SOP24	8	32	80	200	
		SOP20	8	32	80	200	
		NSOP16	9	35	50	130	
3	Elements coplanarity QFP	< 0.076mm				
4	Operating temperature	Normally room temperature				
5	Soldering temperature (preheating, baking soldering, including maximum soldering temperature and supportable repair times	260℃（+0，-5）/3time				
6	Solder , soldering process curve description is as follows.	Please follow Jedec standard: J-STD-020D				
7	Heat durability	< 260℃				
8	Dimensions and weight	Package	Dimension (unit: mm)			Weight
			Length	Width	Heigth	(unit: g)
		LQFP44	10	10	1.4	0.36
		QFN32	5	5	0.75	0.063
		SOP32	20.53	7.5	2.5	0.89
		SOP28	17.9	7.5	2.5	0.78
		QFN24	4	4	0.75	0.031
		SOP24	15.4	7.5	2.5	0.66
		SOP20	12.8	7.5	2.5	0.55
		NSOP16	9.9	3.9	1.55	0.15
9	Humidity sensitivity level	MSL3				

No.	Process Requirements	Note
10	Electrostatic sensitivity level	HBM : ≦8000 V
11	Device package and storage life	1 year, or 168 hours after unpacking sealed package Environmental temperature < 30℃, humidity 60% RH

Reflow Soldering Temperature Curve

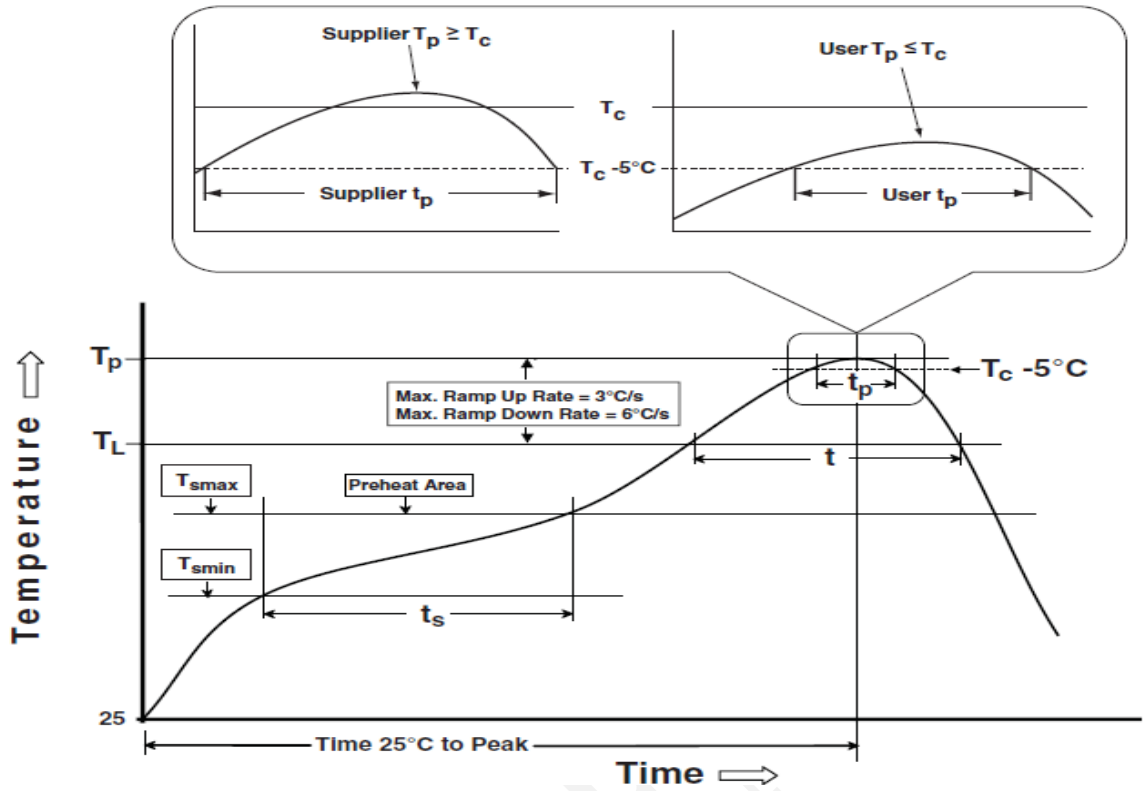


Diagram 19-7: Reflow Soldering Temperature Curve

Reflow Soldering Temperature Distribution

Temperature Distribution Characteristics	Lead-free solder
Average ramp up rate (T1-Tp)	Maximum 3℃/S
Preheat/prewatering - Temperature Min (TS min) - Temperature Max (TS max) - Duration (from TS min to TS max)	 150℃ 200℃ 60~120S
Hold time: - Temperature (**TL**) - Time (**tL**)	 217℃ 60~150S
Time within peak/category temperature (**tP**) 5℃	Refer to Figure 1
Time within actual peak temperature (**tP**) 5℃	30S
Ramp up rate	Maximum 6℃/S
Time 25℃ to peak	Maximum 8 minutes

Figure 1: Lead-free Soldering Process--Packaging Reflow Soldering Temperature

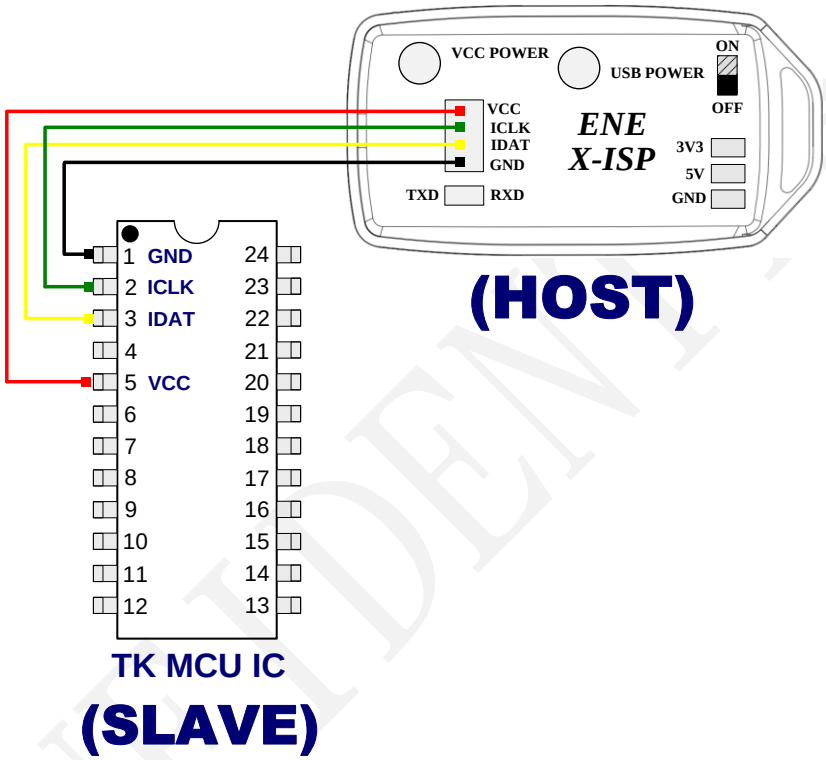
Package thickness	Volume mm3 < 350	Volume mm3 350-2000	Volume mm3 > 2000
＜1.6mm	260+0℃	260+0℃	260+0℃
1.6mm-2.5mm	260+0℃	250+0℃	245+0℃
≧2.5mm	250+0℃	245+0℃	245+0℃

Figure 19-1: Lead-free Soldering Process-Packaging Reflow Soldering Temperature

Appendix 1: ISP (In-System Programming) Overview

Overview

TK18 provides 1 channel ISP serial port communication. This communication protocol applies standard hardware SMB bus protocol. Its ports are respectively ICLK and IDAT. TK18 functions of Online System Updata ISP, Online Circuit Updata ICp and Online TK Signal Debugging can be realized through ISP ports of VCC, ICLK, IDAT and GND. The application connection of TK18 ISP is as follows:



Appendix Diagram 1-1: ISP Standard Application Connection

Note:

1. Appendix Diagram 1-1 shows the standard application connection of **slave** TK MCU IC with **master** X-ISP tools. Certainly, slave ISP outlet can be led out directly from both bare chip IC and IC pin soldered on circuit board; while master can be connected to both ene X-ISP tools and X-WRITER.
2. The ICLK and IDAT is pin share GPIO, and when the multiplexed GPIO is used to simultaneously drive other peripherals (such as LED COM, BUZZER etc ...), it may affect the ICLK and IDAT can not communicate; If this problem occurs, the GPIO Pin is disconnected the peripheral and reconnected ISP.

Related Control Registers

I2C_S_ADDR (F002H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	I2CS_ADDR: I2S device address							I2CRW
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/-
Default	1	0	0	0	0	0	0	0

bit7-1 **I2C_S_ADDR**: I^{2}C slave device and ISP SMB slave address register (default: 1000000)

bit0 **I2CRW**: I^{2}C bus R/W
0: Write
1: Read

I2C_S_CTRL (F003H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	I2CSEN	ISPEN	---	---	---	---
Read/write	---	---	R/W	R/W	---	---	---	---
Default	0	0	0	1	0	1	0	1

bit7-6 Reserved

bit5 **I2CSEN**: I^{2}C slave device
0: Disable (default)
1: Enable

bit4 **ISPEN**: ISP SMB slave device
0: Disable
1: Enable (default)

bit3-0 Reserved

Note: Since TK18 ISP SMB bus address register and I^{2}C slave device address register are the same one (I2C_S_ADDR), only of of them can be enable; Whenever TK18 is power-on reset, ISP SMB bus (default) is enable while I^{2}C slave device is disable. If user wants to enable I^{2}C slave device after the system enters normal operating mode after power-on reset, please remember to disable ISP SMB.

ISPCLK_MUX (F00EH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	ISPCLK_MUX: select a GPIO for ICLK input.					
Read/write	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	0	0	0

bit7-6 Reserved

bit5-0 **ISPCLK_MUX**: Select register for ICLK channel port of ISP serial port communication (0~35)

000000: Select GPIO0 for ICLK channel input

000001: Select GPIO1 for ICLK channel input

: :

100000: Select GPIO24 for ICLK channel input (default)

: :

100011: Select GPIO35 for ICLK channel input

Others: Reserved

ISPDAT_MUX (F00FH) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	---	---	ISPDAT_MUX: select a GPIO for IDAT input.					
Read/write	---	---	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	0	0	1

bit7-6 Reserved

bit5-0 **ISPDAT_MUX**: Select register for IDAT channel port of ISP serial port communication (0~35)

000000: select GPIO0 for IDAT input

000001: select GPIO1 for IDAT input

: :

100001: select GPIO25 for IDAT input (default)

: :

100011: select GPIO35 for IDAT input

Others: Reserved

Note: GPIO24 and GPIO25 are assigned in default to TK18 ICLK and IDAT channel. However, users can map this pin function to any GPIO port to realize through ISPCLK_MUX and ISPDAT_MUX registers.(**Caution: ICLK and IDAT port cann't be configured together)**

Applications and Instructions

TK18 provides Online System Updata ISP, Online Circuit Update ICP, Online TK Signal Debugging and other functions through ISP SMB bus. Please respectively refer to X-ANA, X-ISP and X-WRITER manual for application and realizaiton.

Appendix 2: Procedure self-Defined Function Register

TK18 provide 1 bit "Procedure self-Defined Function Register (F018H)), which is used to provide user with a 8 bit flag bit that can be self-defined and used with permanent address. Its configuration is as follows:

FWREG (F018H) Register

Bit No.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Name	FWREG7	FWREG6	FWREG5	FWREG4	FWREG3	FWREG2	FWREG1	FWREG0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

bit7 - 0 **FWREG7~FWREG0**: Procedure self-defined function

Note: Partial TK18 registers are applied by system firmware, which are not open to user. Therefore, they are not included in this reference manual. When user applies library files or software package provided by ene, please do not alter these registers at will avoiding system malfunction.

Appendix 3: Instruction Set

8501 support all the following instructions:

OpCode: in Hexadecimal format and \ (b) means Binary.

Byte: stands for byte number of the instruction.

Cycle: stands for number of cycle needed to complete the instruction.

Arithmetic				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
ADD A, #data	24	2	2	Add immediate data to Accumulator
ADD A, direct	25	2	2	Add direct byte to Accumulator
ADD A, @ R_N	26~27	1	2	Add indirect RAM to Accumulator (@R0~R1, OP 0x26~0x27)
ADD A, R_N	28~2F	1	2	Add register to Accumulator (R0~R7, OP 0x28~0x2F)
ADDC A, #data	34	2	2	Add immediate data to Accumulator with Carry
ADDC A, direct	35	2	2	Add direct byte to Accumulator with Carry
ADDC A, @ R_N	36~37	1	2	Add indirect RAM to Accumulator with Carry (@R0~R1, OP 0x26~0x27)
ADDC A, R_N	38~3F	1	2	Add register to Accumulator with Carry (R0~R7, OP 0x38~0x3F)
SUBB A, #data	94	2	2	Subtract immediate data from ACC with Borrow
SUBB A, direct	95	2	2	Subtract direct byte from ACC with Borrow
SUBB A, @ R_N	96~97	1	2	Subtract indirect RAM from ACC with Borrow (R0~R1, OP 0x96~0x97)
SUBB A, R_N	98~9F	1	2	Subtract register from Accumulator with Borrow (R0~R7, OP 0x98~0x9F)
INC A	04	1	2	Increment Accumulator
INC direct	05	2	2	Increment direct byte
INC @ R_N	06~07	1	2	Increment indirect RAM (R0~R1, OP 0x06~0x07)
INC R_N	08~0F	1	2	Increment Register (R0~R7, OP 0x08~0x0F)
DEC A	14	1	2	Decrement Accumulator
DEC direct	15	2	2	Decrement direct byte
DEC @ R_N	16~17	1	2	Decrement indirect RAM (R0~R1, OP 0x16~0x17)
DEC R_N	18~1F	1	2	Decrement Register (R0~R7, OP 0x18~0x1F)

Arithmetic				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
INC DPTR	A3	1	2	Increment Data Pointer
MUL AB	A4	1	2	Multiply A & B
DIV AB	84	1	2	Divide A by B
DA A	D4	1	2	Decimal Adjust Accumulator

Logic & Byte Operation				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
ANL direct, A	52	2	2	AND Accumulator to direct byte
ANL direct, #data	53	3	2	AND immediate data to direct byte
ANL A, #data	54	2	2	AND immediate data to Accumulator
ANL A, direct	55	2	2	AND direct byte to Accumulator
ANL A, @ R_N	56~57	1	2	AND indirect RAM to Accumulator (R0~R1, OP 0x56~0x57)
ANL A, R_N	58~58	1	2	AND Register to Accumulator (R0~R7, OP 0x58~0x5F)
ORL direct, A	42	2	2	OR Accumulator to direct byte
ORL direct, #data	43	3	2	OR immediate data to direct byte
ORL A, #data	44	2	2	OR immediate data to Accumulator
ORL A, direct	45	2	2	OR direct byte to Accumulator
ORL A, @ R_N	46~47	1	2	OR indirect RAM to Accumulator (R0~R1, OP 0x46~0x47)
ORL A, R_N	48~4F	1	2	OR Register to Accumulator (R0~R7, OP 0x48~0x4F)
XRL direct, A	62	2	2	XOR Accumulator to direct byte
XRL direct, #data	63	3	2	XOR immediate data to direct byte
XRL A, #data	64	2	2	XOR immediate data to Accumulator
XRL A, direct	65	2	2	XOR direct byte to Accumulator
XRL A, @ R_N	66~67	1	2	XOR indirect RAM to Accumulator (R0~R1, OP 0x66~0x67)
XRL A, R_N	68~6F	1	2	XOR Register to Accumulator (R0~R7, OP 0x68~0x6F)
CLR A	E4	1	2	Clear Accumulator
CPL A	F4	1	2	Complement Accumulator

Logic & Byte Operation				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
RL A	23	1	2	Left rotate Accumulator
RLC A	33	1	2	Left rotate Accumulator through Carry
RR A	03	1	2	Right rotate Accumulator
RRC A	13	1	2	Right rotate Accumulator through Carry
SWAP A	C4	1	2	Swap Accumulator Nibbles

Data Movement				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
MOV A, R_N	E8~EF	1	2	Move Register to Accumulator (R0~R7, OP 0xE8~0xEF)
MOV A, direct	E5	2	2	Move direct byte to Accumulator
MOV A, @ R_N	E6~E7	1	2	Move indirect RAM to Accumulator (R0~R1, OP 0xE6~0xE7)
MOV A, #data	74	2	2	Move immediate data to Accumulator
MOV R_N, A	F8~FF	1	2	Move Accumulator to Register (R0~R7, OP 0xF8~0xFF)
MOV R_N, direct	A8~AF	2	2	Move direct byte to Register (R0~R7, OP 0xA8~0xAF)
MOV R_N, #data	78~7F	2	2	Move immediate data to Register (R0~R7, OP 0x78~0x7F)
MOV direct, A	F5	2	2	Move Accumulator to direct byte
MOV direct, @ R_N	86~87	2	2	Move indirect RAM to direct byte (R0~R1, OP 0x86~0x87)
MOV direct, R_N	88~8F	2	2	Move Register to direct byte (R0~R7, OP 0x88~0x8F)
MOV direct, #data	75	3	2	Move immediate data to direct byte
MOV direct, direct	85	3	2	Move direct byte to direct byte
MOV @ R_N, direct	A6~A7	2	2	Move direct byte to indirect RAM (R0~R1, OP 0xA6~0xA7)
MOV @ R_N, A	F6~F7	1	2	Move Accumulator to indirect RAM (R0~R1, OP 0xF6~0xF7)
MOV @ R_N, #data	76~77	2	2	Move immediate to indirect RAM (R0~R1, OP 0x76~0x77)
MOV DPTR,#data16	90	3	2	Load Data Pointer with a 16bit constant
MOVC A,@ A+PC	83	1	>33	Move Code byte relative to PC to Accumulator
MOVC A,@ A+DPTR	93	1	>33	Move Code byte relative to DPTR to Accumulator
MOVX A, @ DPTR	E0	1	>=5	Move External RAM to Accumulator
MOVX A, @ R_N	E2~E3	1	>=5	Move External RAM to Accumulator (R0~R1, OP 0xE2~0xE3)
MOVX @ DPTR, A	F0	1	>=4	Move Accumulator to External RAM
MOVX @ R_N, A	F2~F3	1	>=4	Move Accumulator to External RAM (R0~R1, OP 0xF2~0xF3)

Data Movement				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
POP direct	D0	2	2	POP direct byte from Stack
PUSH direct	C0	2	2	Push direct byte to Stack
XCH A, direct	C5	2	2	Exchange direct byte with Accumulator
XCH A, @ R_N	C6~C7	1	2	Exchange indirect RAM with Accumulator (R0~R1, OP 0xC6~0xC7)
XCH A, R_N	C8~CF	1	2	Exchange Register with Accumulator (R0~R7, OP 0xC8~0xCF)
XCHD A, @ R_N	D6~D7	1	2	Exchange low order nibble of indirect RAM with Accumulator (R0~R1, OP 0xD6~0xD7)

Bit Operation				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
SETB bit	D2	2	2	Set direct bit
SETB C	D3	1	2	Set Carry
CLR bit	C2	2	2	Clear direct bit
CLR C	C3	1	2	Clear Carry
CPL bit	B2	2	2	Complement direct bit
CPL C	B3	1	2	Complement Carry
ANL C, bit	82	2	2	AND direct bit to Carry
ANL C, /bit	B0	2	2	AND complement of direct bit to Carry
ORL C, bit	72	2	2	OR direct bit to Carry
ORL C, /bit	A0	2	2	OR complement of direct bit to Carry
MOV C, bit	92	2	2	Move direct bit to Carry
MOV bit, C	A2	2	2	Move Carry to direct bit
JC relative	40	2	2	Jump if Carry is set
JNC relative	50	2	2	Jump if Carry is NOT set
JB bit, relative	20	3	2	Jump if direct bit is set
JBC bit, relative	10	3	2	Jump if direct bit is set & clear bit
JNB bit, relative	30	3	2	Jump if direct bit is NOT set

Program Branching				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
ACALL address11	bbb1 0001	2	3	Absolute sub-routine call
AJMP address11	bbb0 0001	2	2	Absolute jump
LCALL address16	12	3	3	Long sub-routine call
LJMP address16	02	3	2	Long jump
SJMP relative	80	2	2	Short jump (relative address)
JMP @ A+DPTR	73	1	2	Jump indirect relative to the DPTR
JNZ relative	70	2	2	Jump if Accumulator is NOT zero
JZ relative	60	2	2	Jump if Accumulator is zero
CJNE A, #data, relative	B4	3	2	Compare immediate to Accumulator and Jump if NOT equal
CJNE A, direct, relative	B5	3	2	Compare direct byte to Accumulator and Jump if NOT equal
CJNE @R_N,#data, relative	B6~B7	3	2	Compare immediate to indirect and Jump if NOT equal (R0~R1, OP 0xB6~0xB7)
CJNE R_N, #data, relative	B8~BF	3	2	Compare immediate to Register and Jump if NOT equal (R0~R7, OP 0xB8~0xBF)
DJNZ direct, relative	D5	3	2	Decrement direct byte and Jump if NOT zero
DJNZ R_N, relative	D8~DF	2	2	Decrement register and Jump if NOT zero (R0~R7, OP 0xD8~0xDF)
RET	22	1	3	Return from sub-routine
RETI	32	1	3	Return form interrupt

Special Instruction				
Mnemonic	**OP code**	**Byte**	**Cycle**	**Description**
NOP	00	1	2	No Operation