SWITCHED CAPACITOR VOLTAGE CONVERTER WITH REGULATOR

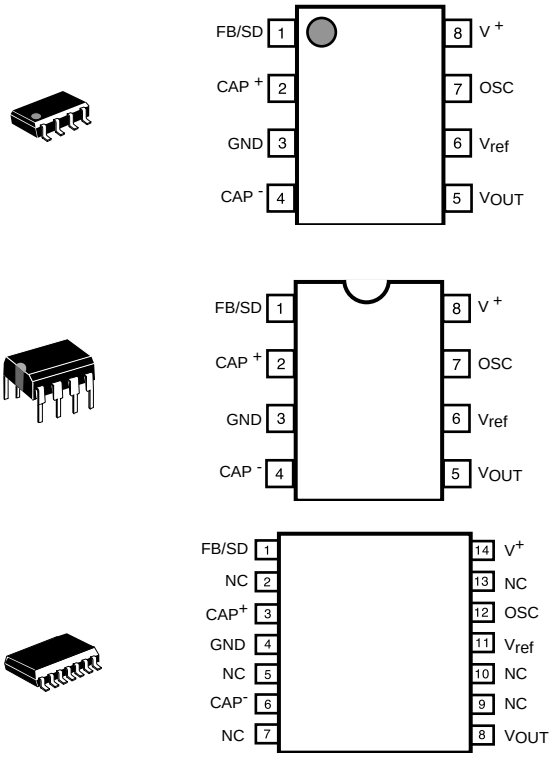
FEATURES

- **35 mA (typ.) Output Current**
- **Operating Range 3.5 to 7 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synch**

APPLICATIONS

- **Voltage Inverter**
- **Negative Voltage Doubler**
- **Voltage Regulator**
- **Positive Voltage Doubler**

TK75018



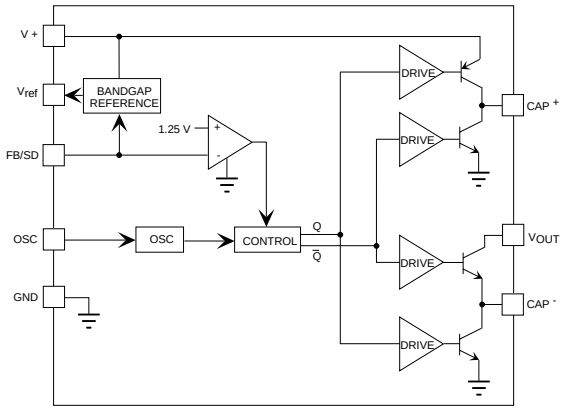
DESCRIPTION

The TK75018 is a monolithic switched capacitor converter with feedback control. With just two capacitors, the TK75018 can create a negative voltage supply which tracks a positive supply. As an alternative, the feedback pin can be used to establish regulation at a desired voltage, and it can also be used as a shutdown signal input. A single TK75018 can also be configured as a non-inverting step-up converter or dual output voltage doubler.

With no external timing elements, the converter will self-oscillate at 25 kHz, nominal. This frequency can also be user adjusted with a small capacitor or synchronized to another oscillator.

Quiescent current is typically 2.5 mA. Standby current is guaranteed less than 200 µA over the full operating temperature and input voltage ranges.

BLOCK DIAGRAM



ORDERING INFORMATION

TK75018 □C□□

Package Code

Tape/Reel Code

Temp. Range

PACKAGE CODE	TEMPERATURE RANGE	TAPE/REEL CODE
D: DIP-8	C: -20 TO 80 °C	TL: Tape Left
M: SOP-8		
V: TSSOP-14		

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{IN} For Doubler Conf. ..... 7 V
Supply Voltage V_{IN} For Regulating Conf. ..... 8 V
Power Dissipation TK75018M (Note 1) ..... 600 mW
Power Dissipation TK75018D (Note 2) ..... 1000 mW
Power Dissipation TK75018V (Note 3) ..... 950 mW
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -20 to 80 °C
Junction Temperature ..... 150 °C
Lead Soldering Temperature (10 s) ..... 235 °C

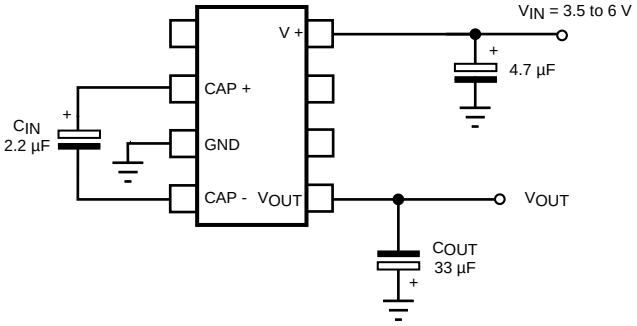
TK75018 ELECTRICAL CHARACTERISTICS

Test conditions: V_{IN} = 5.0 V, $T_A = T_j$ = Operating Temperature Range, Note 6 Configuration, unless otherwise specified.

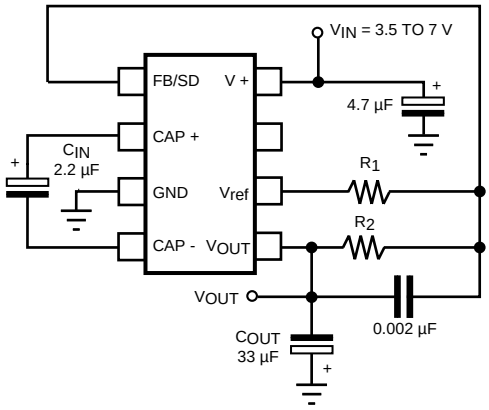
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC(Reg)}$	Supply Current Regulating	I_{LOAD} = 0 mA, (Note 6)		2.5	3.5	mA
$I_{CC(Inv)}$	Supply Current Inverting Mode	I_{LOAD} = 0 mA		3.5	4.5	mA
V_{CC}	Supply Voltage Range	Under Note 6 Conditions	3.5		7	V
V_{LOSS}	Voltage Loss (V_{IN} - V_{OUT})	I_{OUT} = 1 mA, (Note 4)		0.35	0.55	V
		I_{OUT} = 20 mA, (Note 4)		1	1.5	V
R_{OUT}	Output Resistance	ΔI_{OUT} = 1 mA to 20 mA, (Notes 4,5)		32	54	Ω
f_{OSC}	Oscillator Frequency	3.5 V ≤ V_{IN} ≤ 7 V, (Note 6)	15	25	35	kHz
V_{ref}	Reference Voltage	$T_A = T_j$ = 25 °C	2.35	2.50	2.65	V
		$T_A = T_j$ = Operating Temp. Range	2.25		2.75	V
V_{OUT}	Regulated Voltage	T_j = 25 °C, I_L = 1 mA, (Note 6)	-2.8	-3.0	-3.2	V
Line Reg	Line Regulation	3.5 V ≤ V_{IN} ≤ 7 V, I_L = 1 mA, (Note 6)		15	80	mV
$LoadReg_1$	Load Regulation @ 20 mA	1 mA ≤ I_{OUT} ≤ 20 mA, (Note 6)		20	150	mV
$LoadReg_2$	Load Regulation @ 35 mA	1 mA ≤ I_{OUT} ≤ 35 mA, (Note 6)		60	300	mV
I_{STBY}	Standby Current	V_{PIN1} = 0 V, (Note 6)		60	200	µA
$R_{OUT(Ref)}$	Reference Output Resistance	V_{ref} ≤ 80 µA		350		Ω

Note 1: Power dissipation is 600 mW when mounted as recommended. Derate at 4.8 mW/°C for operation above 25 °C.
Note 2: Power dissipation is 1000 mW when mounted as recommended. Derate at 8 mW/°C for operation above 25 °C
Note 3: Power dissipation is 950 mW when mounted as recommended. Derate at 7.6 mW/ °C for operation above 25 °C.
Note 4: Device is connected as an inverter, with pins 1, 6, and 7 unconnected; C_{IN} = 2.2 µF tantalum, C_{OUT} = 33 µF tantalum.
Note 5: Output resistance means the slope of the ΔV_{OUT} vs. ΔI_{OUT} curve, for output currents of 1 to 20 mA. This represents a linear approximation of the curve.
Note 6: Device is connected as a positive to negative converter/regulator with R_1 = 44.2 k, R_2 = 154 k, C_1 = 4.7 nF, C_{VIN} = 4.7 µF tantalum, C_{IN} = 2.2 µF tantalum, C_{OUT} = 33 µF tantalum.

TEST CIRCUITS



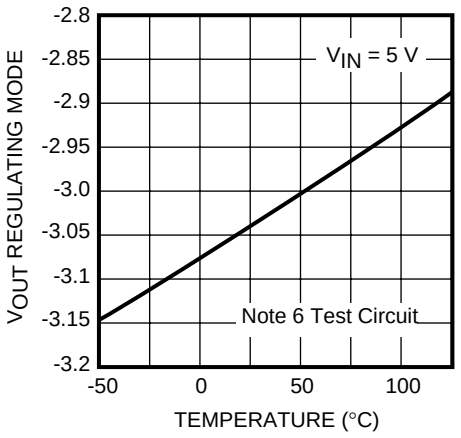
NOTE 4 TEST CIRCUIT (Non Regulating)



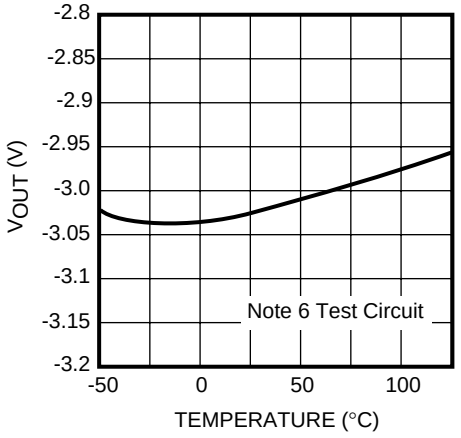
NOTE 6 TEST CIRCUIT (Regulating)

TYPICAL PERFORMANCE CHARACTERISTICS

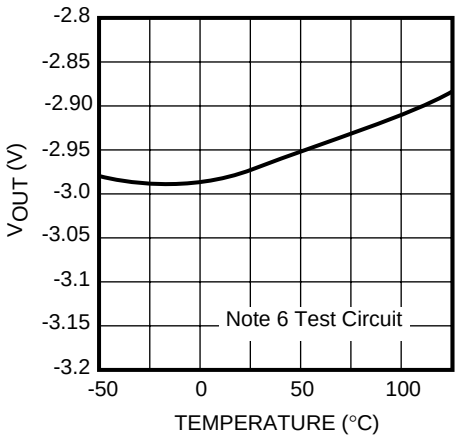
OUTPUT VOLTAGE REGULATING @ 0 mA LOAD vs. TEMPERATURE



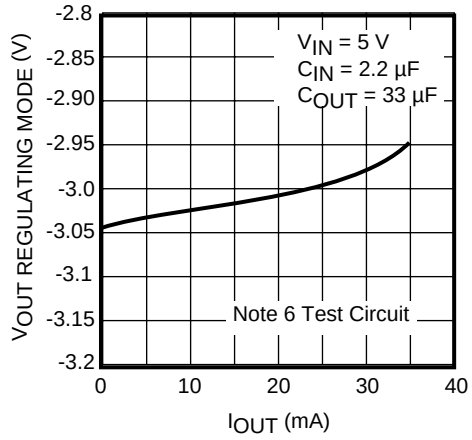
OUTPUT VOLTAGE REGULATING @ 20 mA LOAD vs. TEMPERATURE



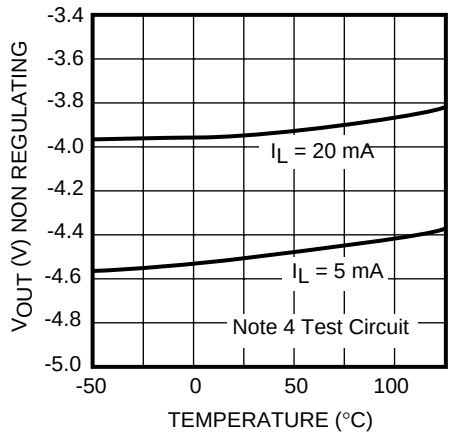
OUTPUT VOLTAGE REGULATING @ 35 mA LOAD vs. TEMPERATURE



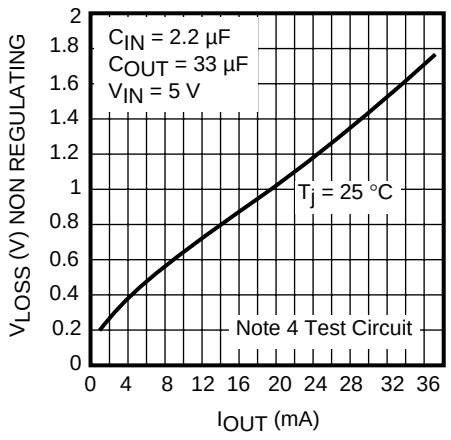
OUTPUT VOLTAGE vs. OUTPUT CURRENT



OUTPUT VOLTAGE vs. TEMPERATURE

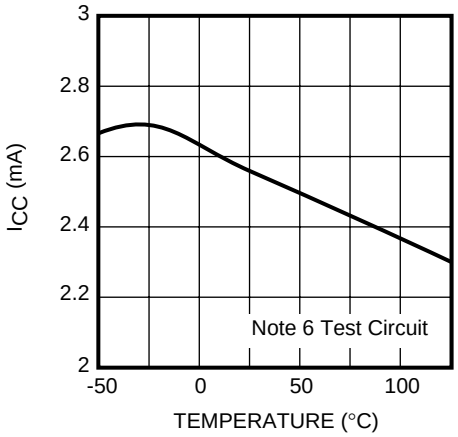


VOLTAGE LOSS vs. OUTPUT CURRENT

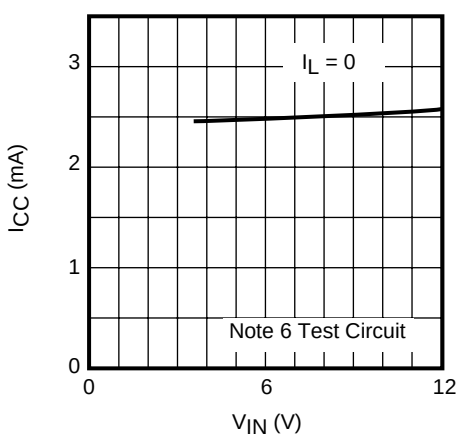


TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

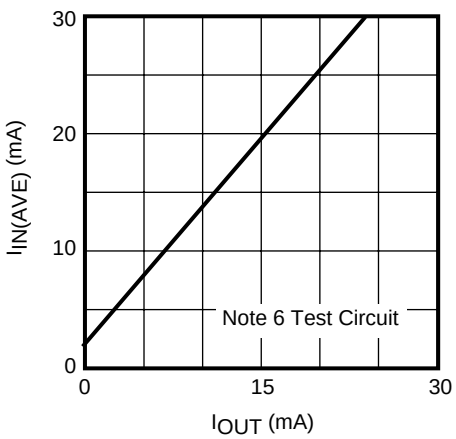
SUPPLY CURRENT vs. TEMPERATURE @ 5 V



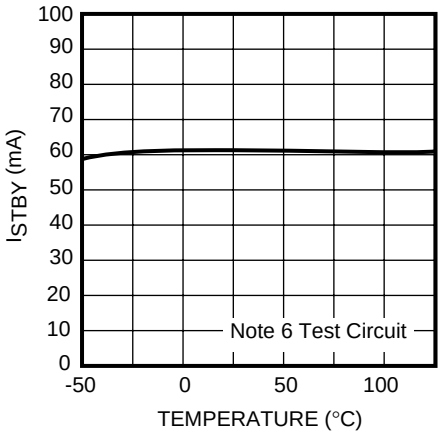
SUPPLY CURRENT vs. INPUT VOLTAGE



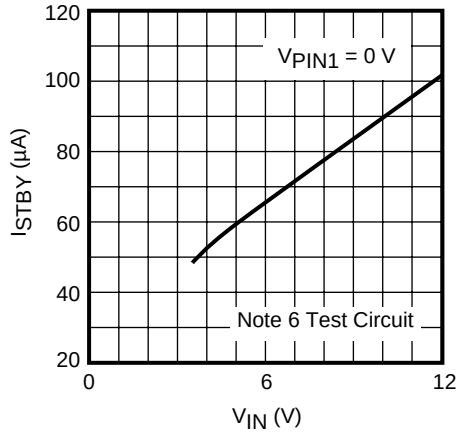
AVERAGE INPUT CURRENT vs. OUTPUT CURRENT



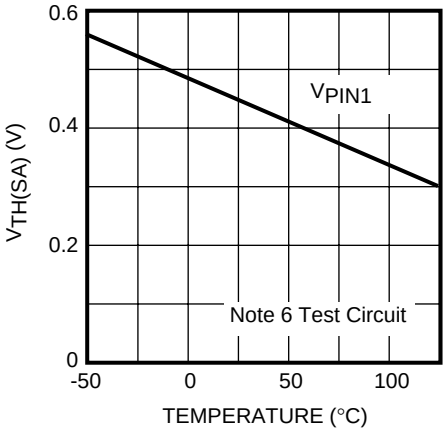
STANDBY CURRENT vs. TEMPERATURE



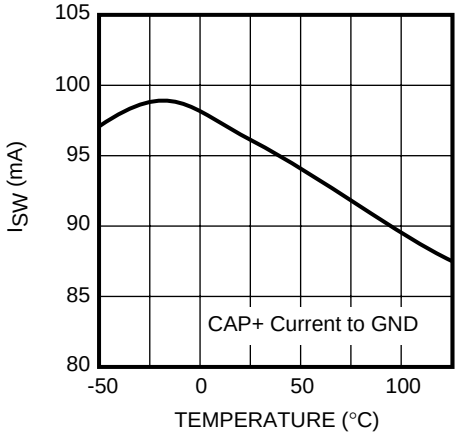
STANDBY CURRENT vs. INPUT VOLTAGE



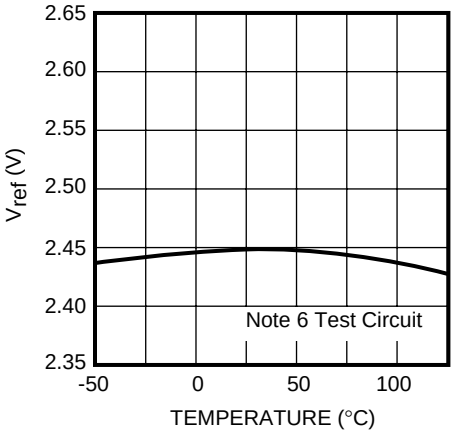
STANDBY THRESHOLD vs. TEMPERATURE



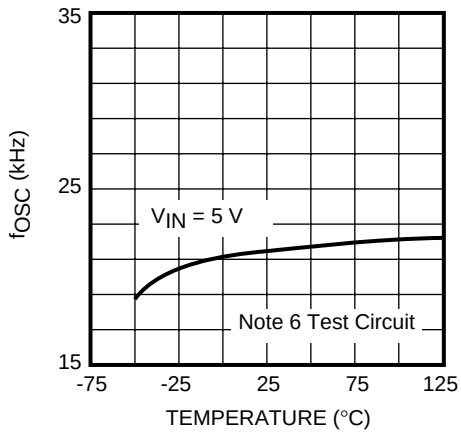
MAXIMUM SWITCH CURRENT vs. TEMPERATURE



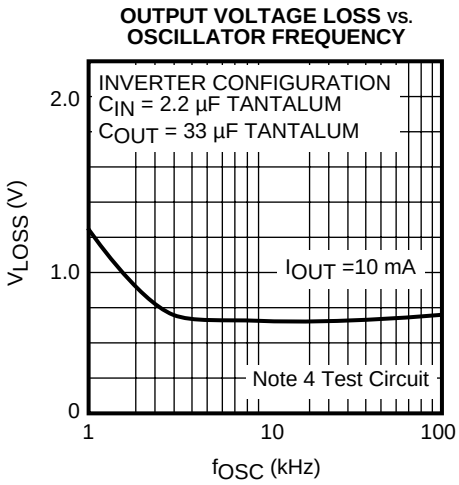
REFERENCE VOLTAGE vs. TEMPERATURE

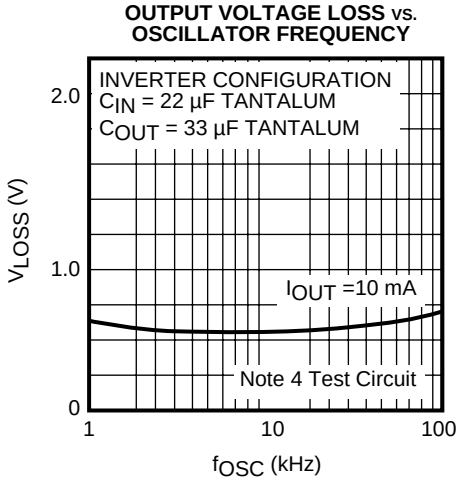


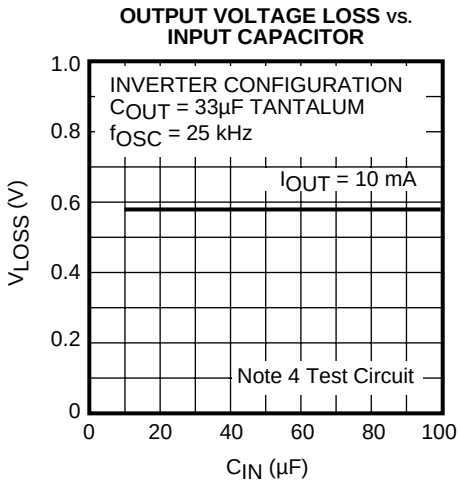
OSCILLATOR FREQUENCY vs. TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)







THEORY OF OPERATION

As in any switched capacitor converter, the means of conveying energy from input to output is done by charging a capacitor between two potentials and then switching one end of the capacitor to a different potential. By some means of rectification, the other end of the capacitor is then forced to dump charge into another capacitor at the converter output, thereby conveying energy.

In a simple example shown in Figure 1, a capacitor C_1 has one side tied to ground and another side charged by a voltage source of potential V_1. The non-grounded side of C_1 is then switched over to be connected to one side of a capacitor C_2, which is at potential V_2 and referenced to ground. V_2 represents the output of the converter. The initial charge on C_1 is:

$$q_1 = C_1 \times V_1$$

When the switch changes over to the V_2 side, C_1 is discharged from potential V_1 to potential V_2. After discharge has occurred the charge on C_1 is then:

$$q_2 = C_1 \times V_2$$

This means that the net transfer of charge which has occurred is:

$$\Delta q = q_1 - q_2 = C_1 (V_1 - V_2)$$

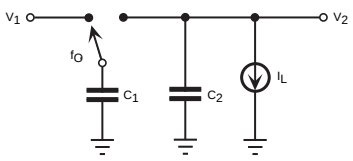


FIGURE 1: SWITCHED CAPACITOR CIRCUIT

If the potential V_2 is sourcing a current I_L, the charge will have to be delivered at a rate:

$$f_O = I_L / \Delta q = I_L / C_1(V_1 - V_2)$$

Thus, the higher the frequency, the more current that can be supported by the converter output.
All else being ideal, the effective losses in the converter in the energy conveyance process is identical to that of a circuit consisting of a resistor between the potentials V_1 and V_2, with the same load at the output side. This equivalent resistor is simply:

$$R_{EQUIV} = (V_1 - V_2) / I_L = 1 / (f_O \times C_1)$$

THEORY OF OPERATION (CONT.)

The illustration in Figure 2 represents an equivalent circuit to the basic example of a switched capacitor circuit in Figure 1.

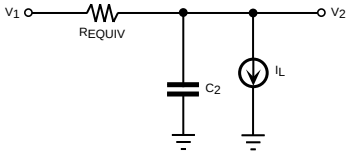


FIGURE 2: SWITCHED CAPACITOR EQUIVALENT CIRCUIT

The efficiency of the ideal converter is given by the output power divided by the input power. Since the same current flows out of each potential, the efficiency, η, is equal to the ratio of V_2 to V_1.

Using equalities established above we find:

$\eta = V_2 / V_1 = \{V_1 - [I_L / (f_O \times C_1)]\} / V_1 = 1 - [I_L / (f_O \times C_1 \times V_1)]$

The last term in the equality string shows that efficiency can be improved by increasing frequency or the value of C_1. Limitations of the circuit and components tend to cause losses which increase with increasing frequency. Therefore, at some point in the frequency spectrum losses will be minimized. Hence, the oscillator of the TK75018 is designed to run in the frequency band where losses are minimized. Since the user will primarily be interested in maintaining a given output voltage, losses are characterized in terms of the voltage loss.

PIN DESCRIPTIONS

FEEDBACK AND SHUTDOWN (FB/SD)

By configuring an error voltage divider into the FB/SD pin, the TK75018 can be used to regulate the output voltage. It is recommended that the parallel combination of the divider resistors be greater than approximately 16 kΩ due to the limited current available from the reference. The Error Amplifier compares the FB/SD pin against an internal 1.25 V reference and limits the charge rate of C_{IN}, thereby limiting its peak charged voltage over a given clock period and, thus, lowering the charge delivery rate to the output. The characteristic frequency response of the converter can be tailored by adjusting the ratio of C_{OUT}:C_{IN}, but it is recommended to keep it around 10:1. A "lead" capacitor from the negative output to the feedback input is required to maintain good light-load regulation; 2000 pF is recommended, regardless of output voltage. For standard configurations, the magnitude of the regulated voltage must be less than that which can be achieved without regulation, $|V_{OUT}| - V_{LOSS}$. Higher regulated output voltages can be achieved by configuring a voltage doubler, at the expense of maximum available output current.

When the FB/SD pin is pulled below the shutdown threshold of ~0.45 V (e.g., via an open collector of an NPN transistor), the reference is shut off and the switching action is terminated. The drivers are set to allow both C_{IN} and C_{OUT} to discharge into the output load. The quiescent supply current will drop to ~ 60 µA. If an error voltage divider is not being used, the TK75018 will automatically restart when the shutdown signal is removed. If such a divider is being used, the current through the divider may be sufficient to keep the device in shutdown until C_{OUT} is fully discharged, since the reference to the amplifier has collapsed during the shutdown. Although C_{OUT} is discharged fairly quickly (allowing a quick restart), this recycling delay may not be acceptable in some applications. This recycling delay can be bypassed by injecting a positive start-up pulse into the SD/FB pin (see Figure 3). This might be readily configured, for example, as a TTL level signal which is diode coupled into the divider. A resistor should be chosen to limit the voltage pulse injection magnitude to 0.7 to 1.1 V. A pulse width of ≥ 100 µs is required to guarantee a successfully coupled start-up signal.

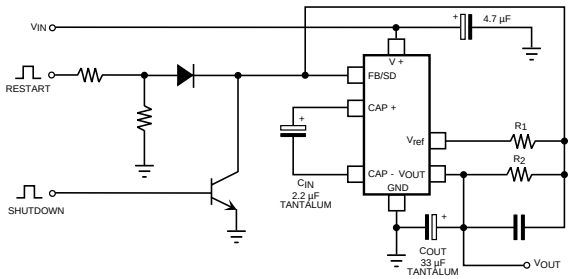


FIGURE 3: FEEDBACK AND SHUTDOWN

PIN DESCRIPTIONS (CONT.)

INPUT CAPACITOR CHARGING PINS (CAP^+/CAP^-)

The positive driving pin of C_{IN} (CAP +) charges the positive node of the capacitor to V_{IN} during t_{CH} and pulls it down to ground during t_{DIS}. The negative driving pin of C_{IN} (CAP -) pulls the negative node of the capacitor to ground during t_{CH} and is driven into the output during t_{DIS}.

CIRCUIT GROUND (GND)

All potentials are referenced to this ground unless otherwise noted.

OUTPUT VOLTAGE (V_{OUT})

In most applications, a capacitor must be placed from this pin to ground to integrate the charge pulses delivered by C_{IN}. A minimum of ten times C_{IN} is recommended. Since the output voltage serves as the substrate inside the IC, the design must ensure that this pin is never raised to a higher potential than ground. This phenomenon will tend to occur when a positive-supply-to-negative-supply load is present at the converter output. A circuit, such as the one shown in Figure 4, is recommended. Under normal operation, the transistor will appear as a short circuit. But the sink current will be cut off from the output pin if the voltage starts to approach ground. The resistor is chosen to keep the transistor saturated under all steady-state operating conditions.

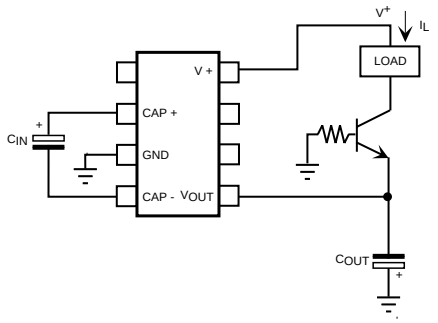


FIGURE 4: POSITIVE REFERENCED LOAD

The equation below can be used to calculate the values of the feedback resistors (R1 and R2) needed to achieve a desired output voltage.

$$R_2 = R_1 \left(\frac{|V_{OUT}|}{1.2\ V} + 1 \right) \text{ where } R_1 \geq 24\ k\Omega$$

REFERENCE VOLTAGE (V_{ref})

This pin provides a nominal 2.5 V buffered reference for external use. Normal output current should be kept below ~160 µA.

OSCILLATOR PROGRAMMING (OSC)

This pin can be used to alter the nominal 25 kHz frequency of the internal oscillator. An internal timing capacitor of ~150 pF is alternately charged during t_{CH} and discharged during t_{DIS} with a 7 µA current source to fixed threshold levels. Adding an external capacitor from the OSC pin to ground will parallel the 150 pF capacitor to slow down the clock period. Adding a small external capacitor from the OSC pin to the CAP^+ pin will source/sink extra charge into/out-of the internal timing capacitor to speed up the transition between thresholds and thereby raise the oscillator frequency. It is recommended that, in the latter configuration, the capacitor be kept below ~30 pF.

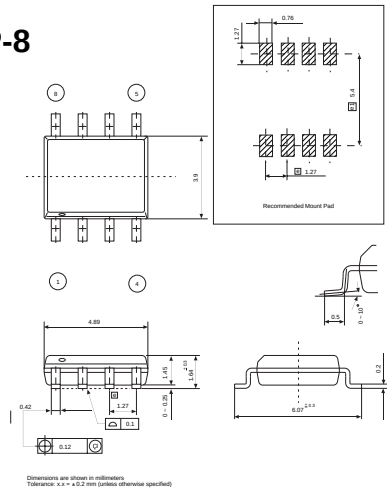
Synchronization of multiple TK75018s can be accomplished by adding pull-up resistors from the OSC pin to the reference voltage and using an open collector from an NPN transistor to provide the discharge. The NPN is then driven by a clocking pulse, and the same pulse can be used to drive multiple devices in the same configuration. It is not recommended to pull the OSC pin high with a low-impedance source. To synchronize and regulate with multiple devices, an external reference can be used as the reference point for the error voltage divider, thus allowing the internal reference to be used as the pull-up point for the OSC pin.

INPUT VOLTAGE (V^+)

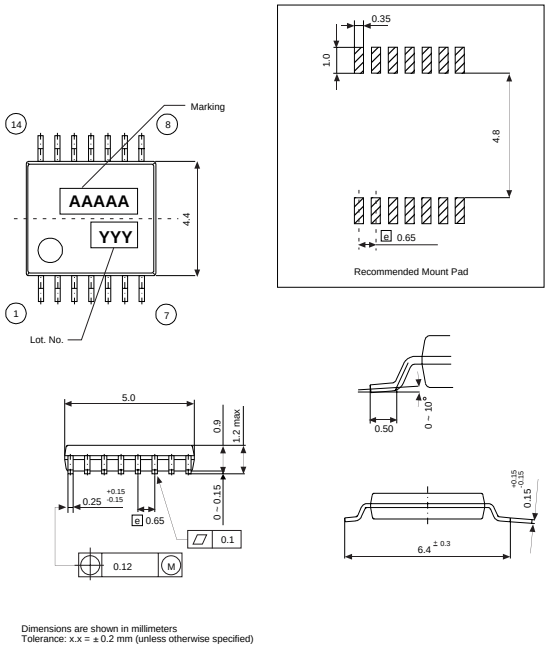
The input voltage is used to charge C_{IN} during the time t_{CH} during each clock period. C_{IN} is then discharged into the output capacitor during time t_{DIS}. During t_{CH}, the input current will be approximately 2.2 times the output current. During t_{DIS}, the input current will be approximately 0.2 times the output current. A low ESR bypass capacitor will average out the varying current seen by the input supply - yielding an average input current of approximately 1.1 times the output current. The bypass capacitor should be placed as near to the TK75018 as possible to disallow inductive spikes on the supply rail of the IC. A minimum of 2 µF is recommended.

PACKAGE OUTLINE

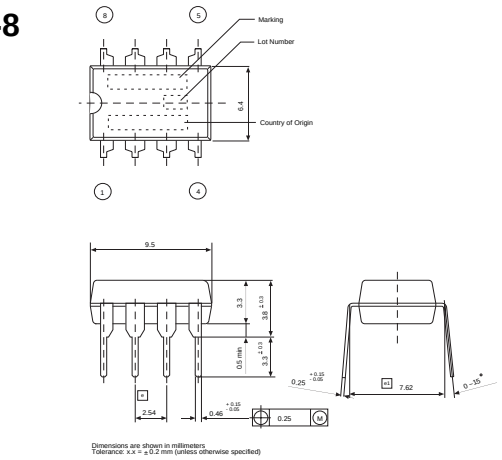
SOP-8



TSSOP-14



DIP-8



Marking Information

Product Code	TK75018

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