TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U−MOSⅧ-H)

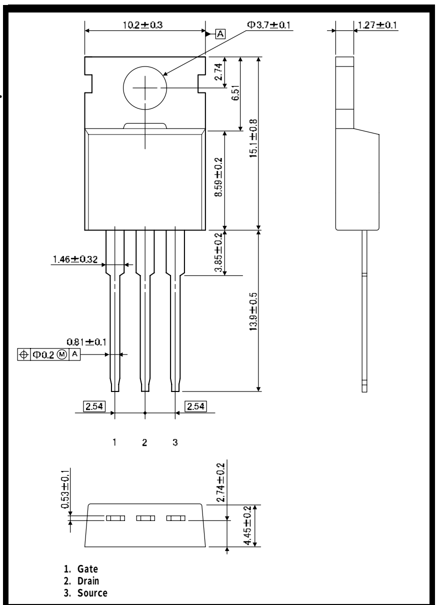
TK80E07NE

■ E-Bike/UPS/Inverter

Note : This product is designed for E-Bike / UPS / Inverter in China / India market.

- Low drain−source on-resistance : $R_{DS(ON)}$ = 6.9 mΩ (typ.)
- Low leakage current : I_{DSS} = 10 μA (max) (V_{DS} = 70 V)
- Enhancement mode : V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 0.3 mA)

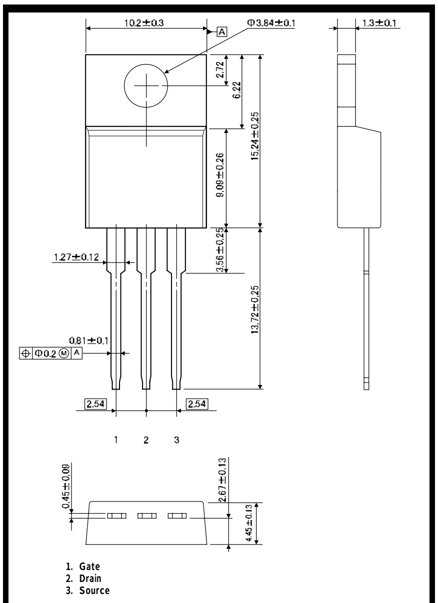
Unit: mm



JEDEC	TO-220AB
JEITA	SC-46
TOSHIBA	-

Weight: 1.93g (typ)

Unit: mm



JEDEC	TO-220AB
JEITA	SC-46
TOSHIBA	-

Weight: 1.9 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	70	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	70	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	80	A
	DC (Note 1,4)	I_D	58	A
	Pulse (Note 1)	I_{DP}	240	A
Drain power dissipation (Tc = 25°C)		P_D	87	W
Single pulse avalanche energy (Note 2)		E_{AS}	16.4	mJ
Avalanche current		I_{AR}	40	A
Repetitive avalanche energy (Note 3)		E_{AR}	8.7	mJ
Peak diode recovery dv/dt (Note 5)		dv/dt	11.5	V/ns
Channel temperature (Note 4)		T_{ch}	175	°C
Storage temperature range (Note 4)		T_{stg}	−55~175	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.72	°C/W
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	°C/W

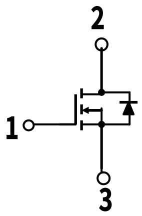
Note 1: Ensure that the channel temperature does not exceed 175°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25°C (initial), L =14.9μH, R_G = 25 Ω, I_{AR} = 40A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: Tc = 100°C

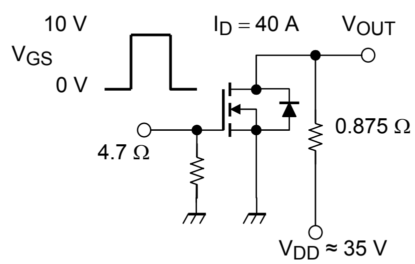
Note 5: $I_{DR} \leqq$ 80 A, di/dt $\leqq$ 160 A/μs, Tch $\leqq$ Tch max., V_{DS} peak < V_{DSS}



This transistor is an electrostatic-sensitive device. Please handle with caution.

Note :Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).Thermal Characteristics

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut−off current		I_{DSS}	V_{DS} = 70 V, V_{GS} = 0 V	—	—	10	μA
Drain−source breakdown voltage		$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	70	—	—	V
		$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V (Note 5)	45	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 0.3 mA	2.0	—	4.0	V
Drain−source ON resistance		$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 40 A	—	6.9	8.5	mΩ
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	2270	—	pF
Reverse transfer capacitance		C_{rss}		—	230	—	
Output capacitance		C_{oss}		—	1390	—	
Switching time	Rise time	t_r		—	12	—	ns
	Turn−on time	t_{on}		—	31	—	
	Fall time	t_f		—	17	—	
	Turn−off time	t_{off}	Duty ≤ 1%, t_w = 10 μs	—	47	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 56 V, V_{GS} = 10 V, I_D = 80 A	—	42	—	nC
Gate−source charge		Q_{gs}		—	28	—	
Gate−drain (“miller”) charge		Q_{gd}		—	14	—	

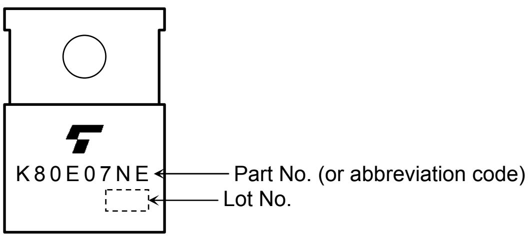
Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	80	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	240	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 80 A, V_{GS} = 0 V	—	—	−1.5	V
Reverse recovery time (Note 6)	t_{rr}	I_{DR} = 80 A, V_{GS} = 0 V, dI_{DR}/dt = 50 A/μs	—	60	—	ns
Reverse recovery charge(Note 6)	Q_{rr}		—	45	—	nC

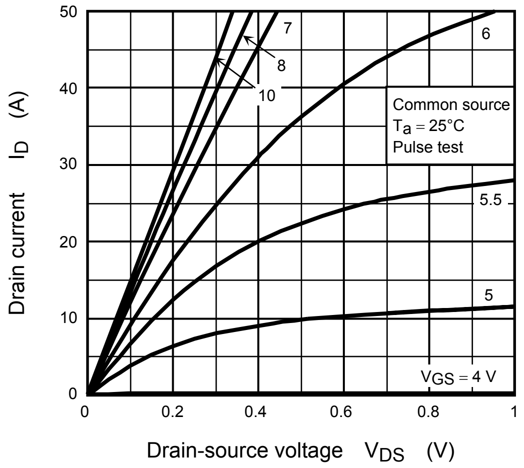
Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode.
Note that the drain-source breakdown voltage is lowered in this mode.

Note 6: Ensure that V_{DS} peak does not exceed V_{DSS}.

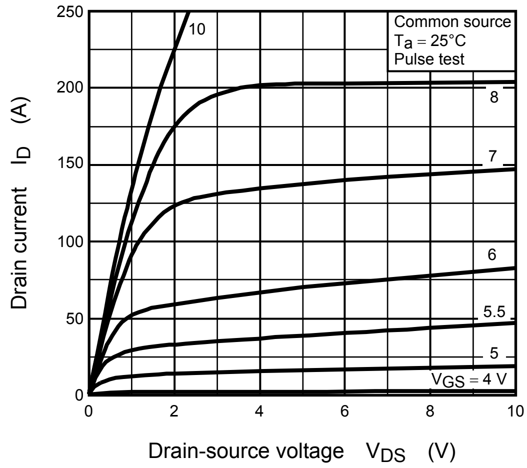
Marking



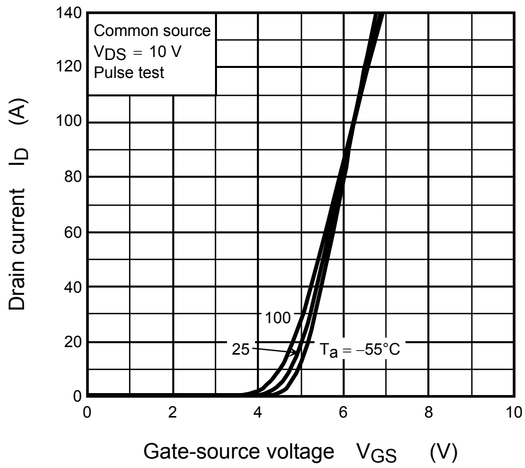
I_D – V_{DS}



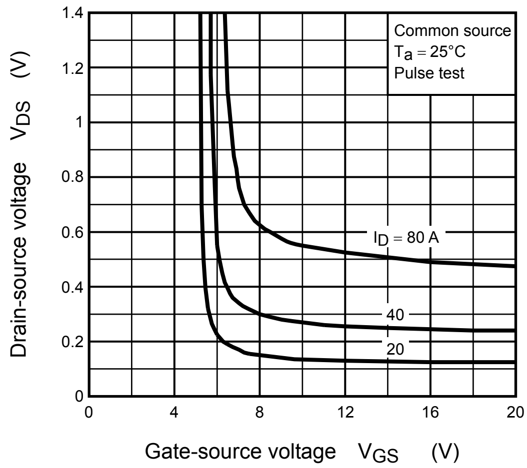
I_D – V_{DS}



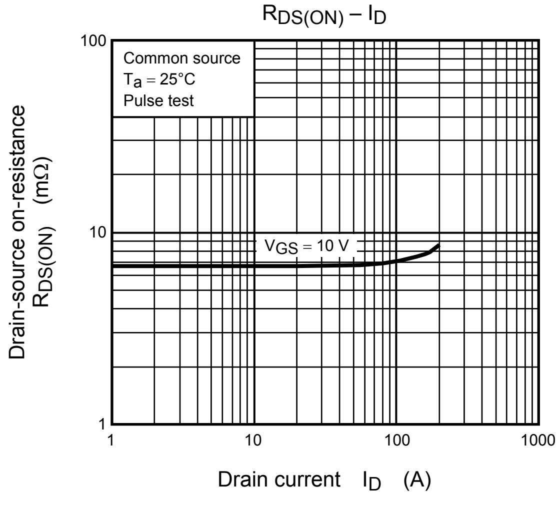
I_D – V_{GS}

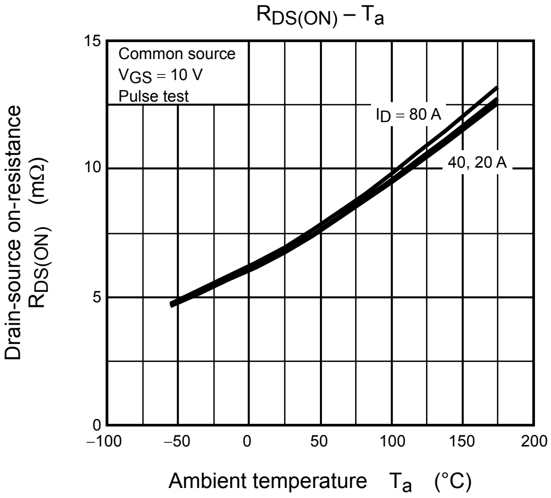


V_{DS} – V_{GS}

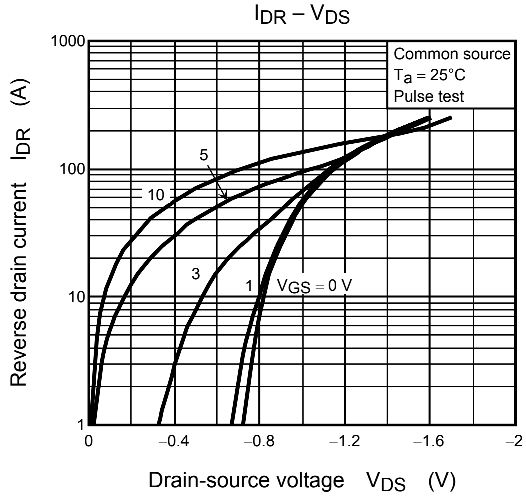


$R_{DS(ON)}$ – I_D

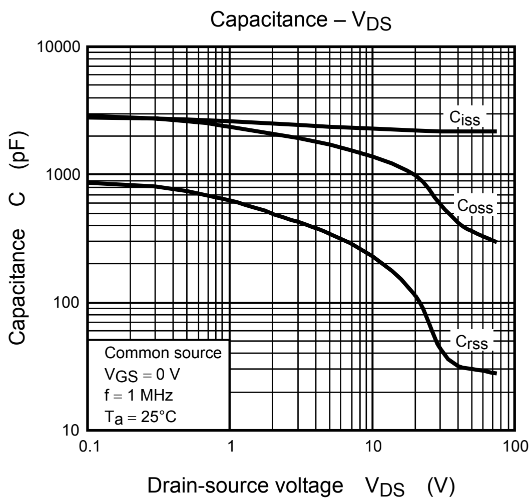




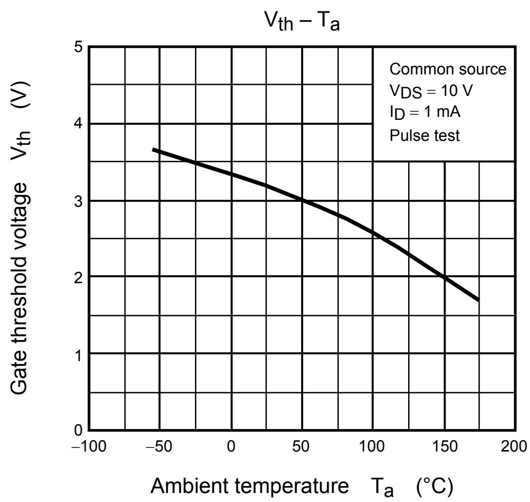
$R_{DS(ON)}$ – T_a
Common source
V_{GS} = 10 V
Pulse test
I_D = 80 A
40, 20 A
Drain-source on-resistance $R_{DS(ON)}$ (mΩ)
Ambient temperature T_a (°C)



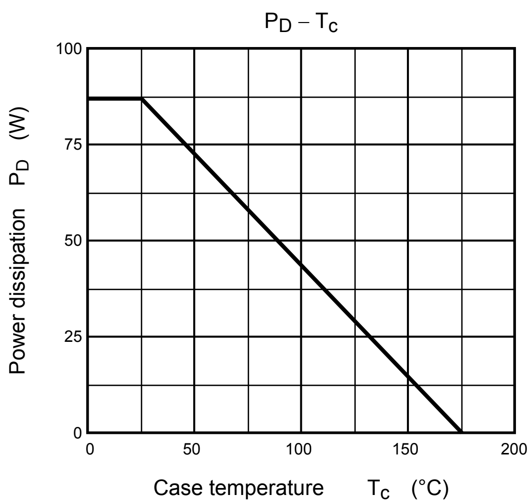
I_{DR} – V_{DS}
Common source
T_a = 25°C
Pulse test
10
5
3
1
V_{GS} = 0 V
Reverse drain current I_{DR} (A)
Drain-source voltage V_{DS} (V)



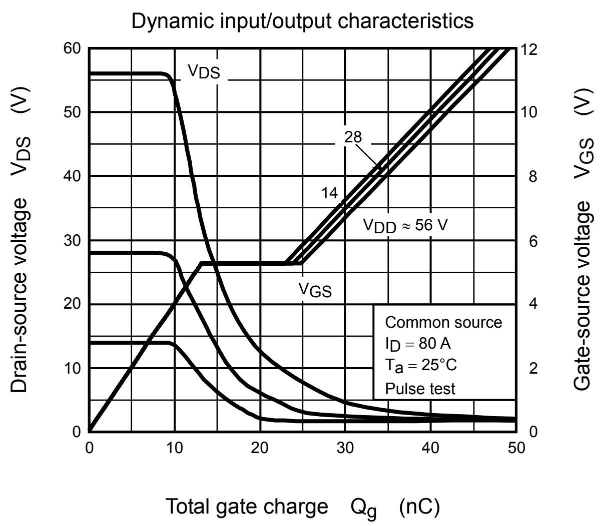
Capacitance – V_{DS}
C_{iss}
C_{oss}
C_{rss}
Common source
V_{GS} = 0 V
f = 1 MHz
T_a = 25°C
Capacitance C (pF)
Drain-source voltage V_{DS} (V)



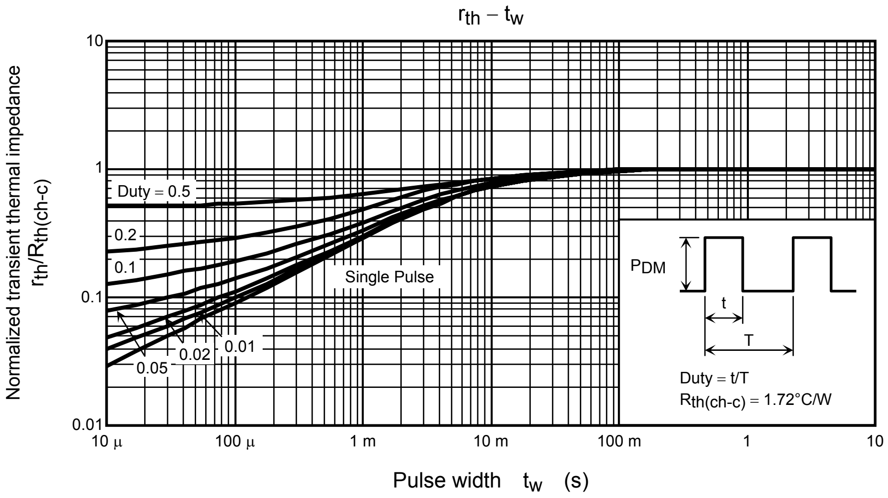
V_{th} – T_a
Common source
V_{DS} = 10 V
I_D = 1 mA
Pulse test
Gate threshold voltage V_{th} (V)
Ambient temperature T_a (°C)

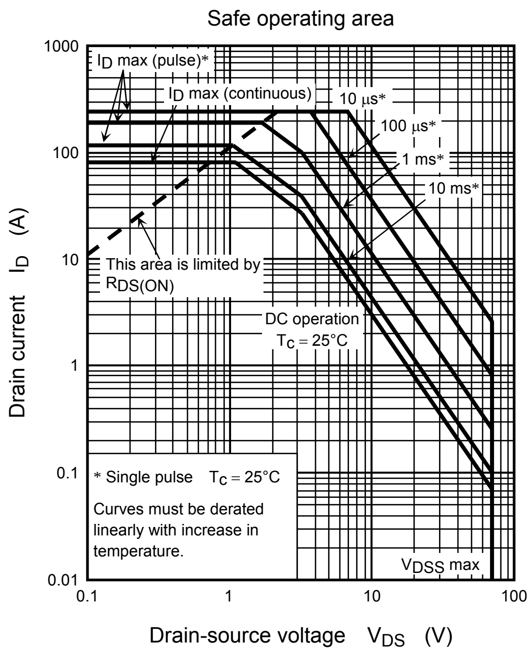


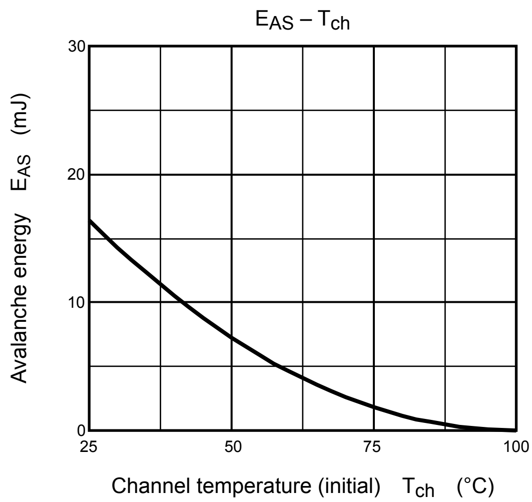
P_D – T_c
Power dissipation P_D (W)
Case temperature T_c (°C)

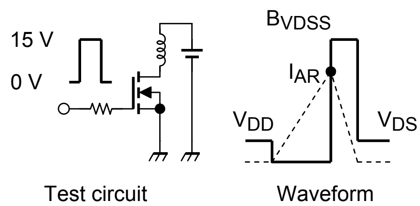


Dynamic input/output characteristics
V_{DS}
28
14
V_{DD} ≈ 56 V
V_{GS}
Common source
I_D = 80 A
T_a = 25°C
Pulse test
Drain-source voltage V_{DS} (V)
Gate-source voltage V_{GS} (V)
Total gate charge Q_g (nC)









$R_G = 25\ \Omega$
$V_{DD} = 25$ V, $L = 14.9\ \mu$H

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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