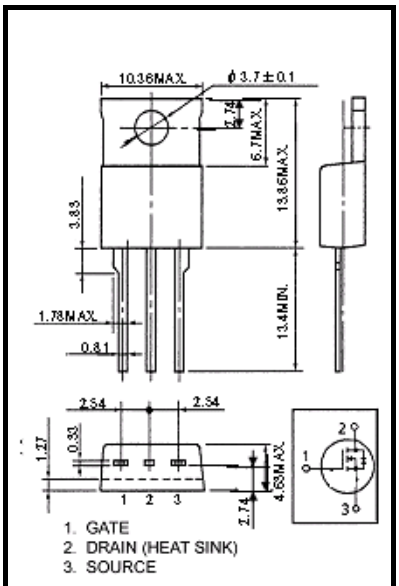
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U−MOS**IV**)

TK80E08K3

■ E-Bike/UPS/Inverter

- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 7.5 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 135 S (typ.)
- Low leakage current : I_{DSS} = 10 μA (max) (V_{DS} = 75 V)
- Enhancement mode : V_{th} = 2.0~4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



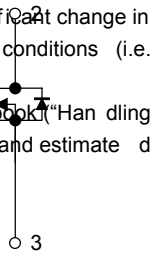
JEDEC	TO-220AB
JEITA	SC-46
TOSHIBA	

Weight: 1.9 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics S		ymbol	Rating	Unit
Drain−source voltage		V_{DSS} 75		V
Drain−gate voltage (R_{GS} = 20 kΩ) V		DGR 75		V
Gate−source voltage		V_{GSS} ±20		V
Drain current	DC (Note 1)	I_D 80		A
	DC (Note 1,4)	I_D 70		A
	Pulse (Note 1)	I_{DP} 240		A
Drain power dissipation (Tc = 25°C)		P_D 200		W
Single pulse avalanche energy (Note 2)		E_{AS} 107		mJ
Avalanche current		I_{AR} 40		A
Repetitive avalanche energy (Note 3)		E_{AR} 20		mJ
Peak diode recovery dv/dt (Note 5)		dv/dt	12	V/ns
Channel temperature (Note 4)		T_{ch} 175		°C
Storage temperature range (Note 4)		T_{stg}	−55~175	°C

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).Thermal Characteristics



Characteristics S	ymbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	0.75	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	83.3	°C / W

Note 1: Ensure that the channel temperature does not exceed 175°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 100 μH, R_G = 25 Ω, I_{AR} = 40A

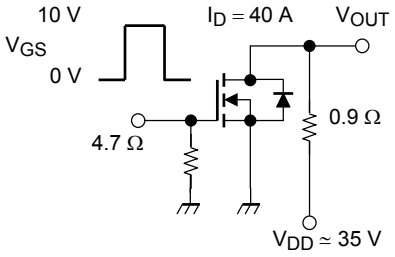
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: Tc=100℃

Note 5: IDR≦80A,di/dt≦160A/μs, Tch≦Tch max.

This transistor is an electrostatic-sensitive device.
Please handle with caution.

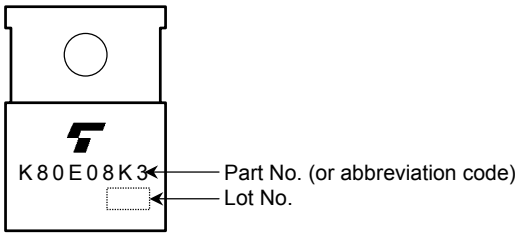
Electrical Characteristics (Ta = 25°C)

Characteristics S		ymbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut−off current		I_{DSS}	V_{DS} = 75 V, V_{DS} = 0 V	—	—	10	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	75	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = -20 V	45	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	2.0	—	4.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 40 A	—	7.5	9.0	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 40 A	67	135	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		3600	—	pF
Reverse transfer capacitance		C_{rss}			350	—	
Output capacitance		C_{oss}		— 500		—	
Switching time	Rise time	t_r			95	—	ns
	Turn−on time	t_{on}			135	—	
	Fall time	t_f			85	—	
	Turn−off time	t_{off}	Duty ≦ 1%, t_w = 10 μs	— 220		—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ 75 V, V_{GS} = 10 V, I_D = 80 A		75	—	nC
Gate−source charge		Q_{gs}			44	—	
Gate−drain (“miller”) charge		Q_{gd}		— 31		—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics S	ymbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	80	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	240	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 80 A, V_{GS} = 0 V	—	—	−1.5	V
Reverse recovery time	t_{rr}	I_{DR} = 80 A, V_{GS} = 0 V dI_{DR} / dt = 100 A / μs	—	45	—	ns
Reverse recovery charge	Q_{rr}		— 72		—	μC

Marking



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