T-52-33-43

TKD8001 ADVANCE DATA SHEET

Trident

TKD8001
Clock Synthesizer and Display DAC

Features

- Combines a Triple Display DAC, Color Look-up Table (256x24), and Dual Frequency Synthesizer
- Supports 4/8/15/16/24-bit per pixel modes
- Supports gamma corrected or CLUT bypass versions of the 15/16/24-bit per pixel modes
- Anti-sparkle circuitry
- VGA, Super VGA, VESA, and 8514/A compatible
- Supports XGA, TARGA+®, and HiCOLOR formats
- 16 selectable video clock frequencies (VCLK) up to 80 MHz
- 16 software selectable or eight hardware selectable memory clock frequencies(MCLK) up to 90 MHz
- Standard MPU interface
- RS-343A and RS-170 compatible outputs
- Power-on reset
- Power-down mode for extended battery life
- 0.8 µm low power CMOS technology
- 52-pin, PLCC package
- Complete Super VGA subsystem requires only 5 active components: graphics controller, BIOS, memory (2 each), and TKD8001

General Description

Trident has developed a combination true-color display DAC and dual frequency synthesizer which can be used with VGA, Super VGA, GUI, 8514/A, etc. color graphics systems. The chip has three 8-bit display DACs, a 256x24 Color Look-up Table, and two clock synthesizers.

The display DACs can generate RS-343A compatible red, green, and blue signals into a doubly terminated 75Ω load without external buffering. RS-170 compatible video signals may also be generated into a singly terminated 75Ω load without external buffering. The DAC output may be set by using an internal or external voltage reference.

The Color Look-up Table (CLUT) may be programmed with 256 8-bit RGB values. The CLUT table may be directly accessed or bypassed in 15 or 16-bit per pixel color, and 24-bit true color modes.

Each of the clock synthesizers has sixteen selectable clock frequencies. One clock synthesizer provides a video dot clock (VCLK). The other provides a video memory interface clock (MCLK).

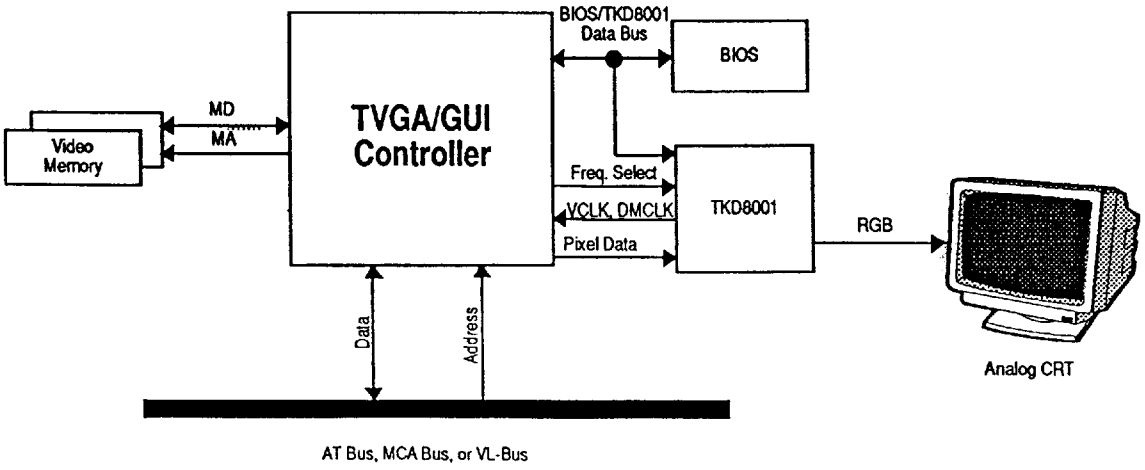

Figure 1. TKD8001 Application Diagram

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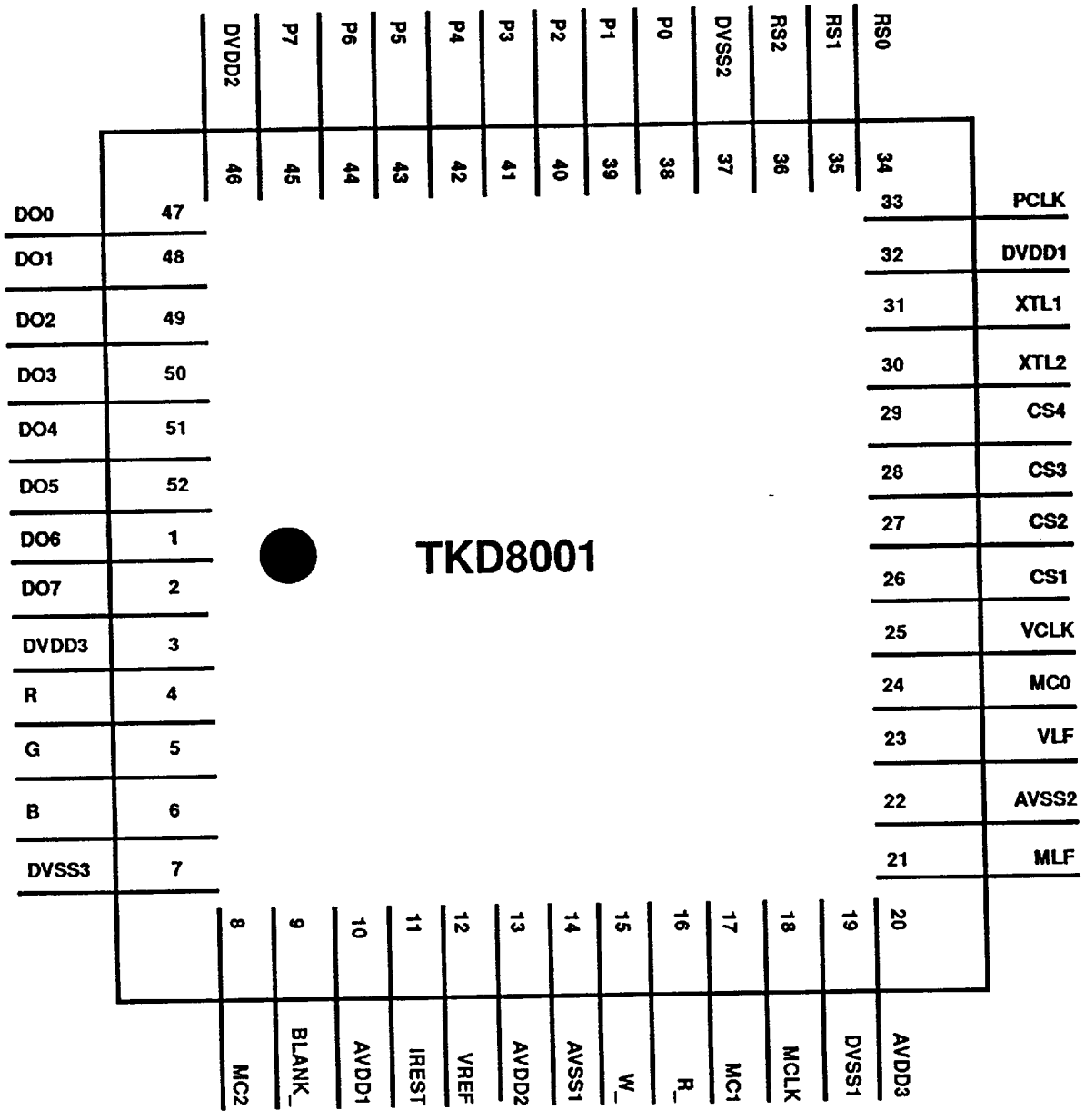


Figure 1. TKD8001 Pinout Diagram

Table 1. TKD8001 Pin Description

Pin	Pin Type	Pin Number	Description
Video DAC Signals			
$\overline{\text{BLANK}}$	I	9	Display blanking control input. $\overline{\text{BLANK}}$ is latched at the rising edge of PCLK. When $\overline{\text{BLANK}}$ is a logical 1, pixel data P7-P0 will be processed and sent to the DACs. When $\overline{\text{BLANK}}$ is a logical 0, the data on P7-P0 is ignored and DAC outputs will be forced to the blanking level. The pin is TTL compatible.
IREST	I	11	The full scale outputs of the TKD8001's DACs are determined by a resistor from IREST to AVSS. The value of the resistor is determined by the following equation: [TBD]
P7-P0	I	45-38	Pixel address. P7-P0 are used as either an address to the RAM look-up table or as direct data to the DAC. These pins are latched at the rising edge of PCLK with the exception of Hi COLOR™ Mode 1. In the HiCOLOR™ Mode 1 case, P7-P0 are latched at both the rising and falling edges of PCLK. These pins are TTL compatible. Connect unused inputs to digital ground.
R, G, B	O	4-6	Analog video output signals. These signals are the outputs of the three video DACs inside the TKD8001. R, G, B are capable of directly driving a doubly-terminated 75 ohm coaxial cable.
$\overline{\text{WR}}$	I	15	Write control input. $\overline{\text{WR}}$ controls the data transfer from the DAC data bus to the selected internal register. Data bits D7-D0 are latched at the rising edge of $\overline{\text{WR}}$. The Register Select bits are latched at the falling edge of $\overline{\text{WR}}$. The pin is TTL compatible.
$\overline{\text{RD}}$	I	16	Read control input. $\overline{\text{RD}}$ controls the data transfer from the selected internal register to the DAC data bus. When $\overline{\text{RD}}$ is a logical 0, data is transferred from the selected internal register to the DAC data bus. The Register Select bits are latched at the falling edge of $\overline{\text{RD}}$. The pin is TTL compatible.
PCLK	I	33	Pixel clock input to the video DAC module. P7-P0 and $\overline{\text{BLANK}}$ are latched at the rising edge of PCLK. Note: In the HiCOLOR™ Mode 1 case, P7-P0 are latched at both the rising and falling edges of PCLK.
Frequency Synthesizer Signals			
CS4-CS1	I	29-26	Video clock frequency select inputs. These pins select a set of PLL parameters that correspond to one of sixteen video clock frequencies. The logic values from these pins are not latched, but are passed directly to the VCLK PLL control circuitry.
MC2-MC0	I	8,17,24	Memory clock frequency select inputs. These pins select eight of sixteen memory clock frequencies listed in the TKD register. The logic values from these pins are not latched, but are passed directly to the MCLK PLL control circuitry.

Table 1. TKD8001 Pin Description - Continued

Pin	Pin Type	Pin Number	Description
MCLK	O	18	Memory clock output. Typically used as a VGA controller or frame buffer refresh clock. Sixteen possible frequencies selectable via the TKD register. Eight possible frequencies selctable via MS2-MS0. Default frequency is 48 MHz.
MLF	I	21	Memory PLL filter node. A 0.1 µF capacitor to AVDD3 is required.
VLF	I	23	Video PLL filter node. A 120 pF capacitor to AVDD3 is required.
VCLK	O	25	Video clock output. Typically used for driving the pixel clock input of the VGA controller.
XTL1	I	31	Reference clock input for the VCLK and MCLK PLL synthesizers. This input may come from an external TTL reference clock (e.g. from the motherboard) or from a series-resonant crystal connected between XTL2 and XTL1. Please note, the reference clock must originate from a stable frequency source.
XTL2	O	30	Crystal output. XTL2 drives a series-resonant crystal from the internal oscillator to generate the synthesizer reference clock. XTL2 is left open if an external TTL reference clock signal is used to drive XTL1.
Common Signals			
RS2-RS0	I	36-34	Register select inputs. RS2-RS0 specify which internal register is to be accessed. RS2-RS0 are sampled at the falling edge of $\overline{WR}$ or $\overline{RD}$. The signals are TTL compatible.
D7-0	I/O	2,1,52-47	Data bus pins. For an MPU write operation, data is latched at the rising edge of $\overline{WR}$. For a read operation, data is read onto D7-0 when $\overline{RD}$ is at a logical 0. The rising edge of $\overline{RD}$ terminates a read operation.
Power Signals			
AVDD2-1	PWR	13,10	Analog +5V power pins. Pins provide power for the DAC portion of the device. These pins are separated from the other power pins to reduce noise.[1]
AVDD3	PWR	20	Analog +5V power pin. Pin provides power for the VCOs, PLL filters, and VCLK and MCLK outputs.[1]
AVSS1	GND	14	Analog ground for the DAC portion of the device. It is separated from the other ground pins to reduce noise.[1]
AVSS2	GND	22	Analog ground for the VCOs, PLL filters, and VCLK and MCLK outputs.[1]
DVDD3-1	PWR	3,46,32	Digital +5V power pins. Pins provide power for the digital portions of the device.[1]
DVSS3-1	GND	7,37,19	Digital ground pins. Pins provide ground for the digital portions of the device.[1]

[1]All power pins should be tied to the same power plane. All ground pins should be tied to the same ground plane.

TKD8001 Register Information

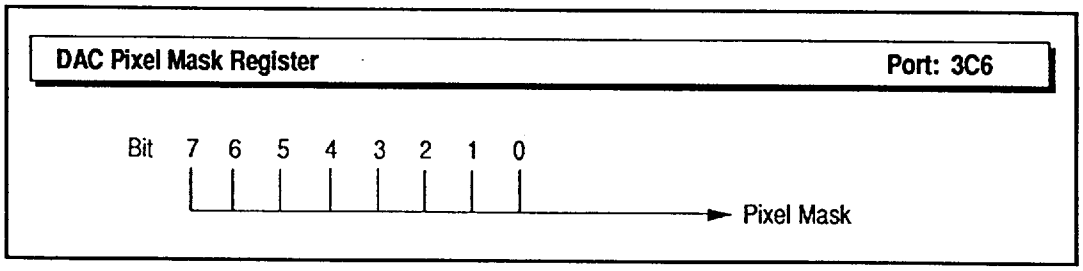
The registers of the TKD8001 may be selected by programming the RS2-RS0 input pins. The registers may be alternatively addressed via their given I/O port. A summary of the TKD8001's registers and detailed discussion of each register follows.

Register Selection Summary

RS2	RS1	RS0	Register	Port
0	0	0	DAC Write Data Address Register	3C8
0	0	1	DAC Data Register	3C9
0	1	0	DAC Pixel Mask Register	3C6
0	1	1	DAC Read Data Address Register/ DAC Status Register	3C7
1	0	0	Reserved	N/A
1	0	1	Test Register	3C9
1	1	0	TKD Register	3C6
1	1	1	Command Register[1]	3C7

[1]This register may also be accessed by reading the Pixel read master register four times consecutively. The next write to the Pixel mask register will be directed to the Command register.

DAC Pixel Mask Register

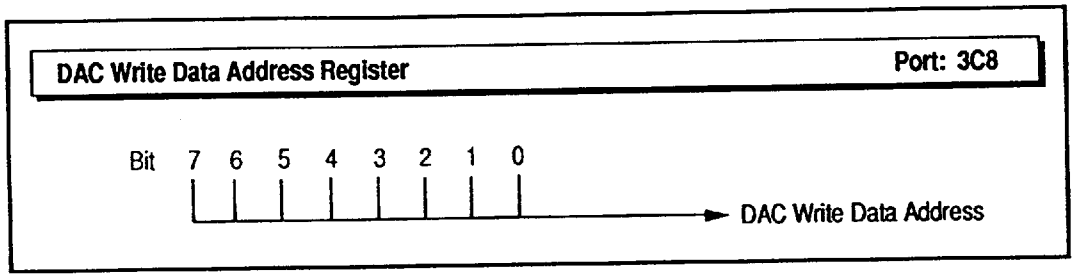


Register Type : Read/Write
Read/Write Port : hex 3C6

Bits 7 - 0: Pixel Mask. The Pixel Mask register is used to mask selected bits of the output from the AttributeController portion of the given TVGA controller. The contents of this register is logically "ANDed"with the pixel data to produce an address which indexes into the video DAC color look-up table. This address determines the resulting analog red, green, and blue signals output by the display DAC portion of the TDK8001.

Provided the color look-up table is initialized properly, animation can be achieved through use of the Pixel Mask register. A value of hex FF should be written to this register for normal operation. The DAC Pixel Mask does not effect Read/Write operations from the DAC color look up table.

DAC Write Data Address Register

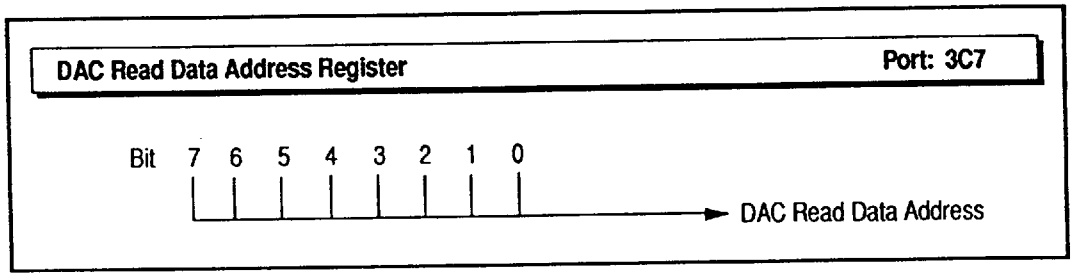


Register Type : Read/Write
Read/Write Port : hex 3C8

Bits 7 - 0: DAC Write Address Bits. A binary address of the palette (Color Look-up Table) location which is to receive data written to the DAC Data Register.

Note : This register is loaded with the address of the color look-up table location which is to receive color data written to the DAC Data Registers. The Write Data Address Register is automatically incremented to the address of the next palette location at the completion of one processor write. A series of color look-up table contents can be loaded by writing the first address to be filled to the DAC Write Data Address Register, followed by writing different red, green, and blue data values for each location. The auto-increment capability for writing data is interrupted by either a write to the DAC Read Data Address register or a read from the DAC Data Register. If the auto-increment operation is interrupted, the DAC Write Data Address Register must be reinitialized before valid DAC Data writes can continue.

DAC Read Data Address Register



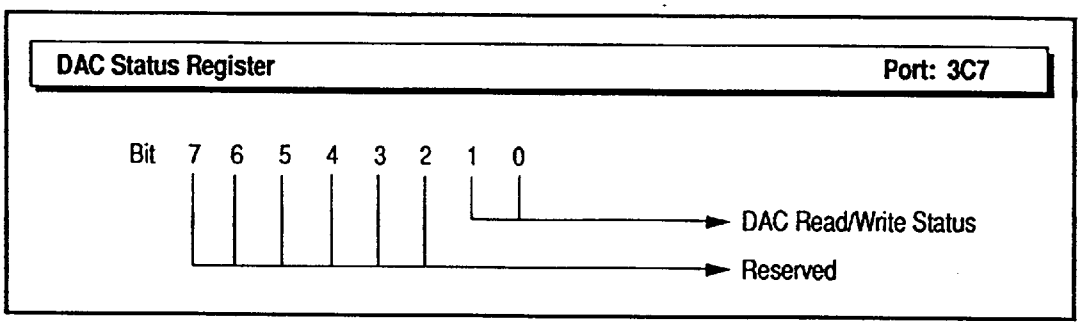
Register Type : Write only
Write Port : hex 3C7

Bits 7 - 0: DAC Read Address Bits. A binary address of the palette (Color Look-up Table) location from which data is produced for reads to the DAC Data Register.

Note : This register is loaded with the address of the Color Look-up Table location from which color data is to be read for the DAC Data Register. The value written to this register can be determined by reading the DAC Write Data Address Register. The value is automatically incremented to the address of the next palette location at the completion of the three processor reads from the DAC Data register. A series of color look-up table contents can be obtained by writing the first

address to be read to the DAC Read Data Address Register, followed by reading the different red, green, and blue data values for each location. The auto-increment capability for reading color data is interrupted by either a write to the DAC Write Data Address Register to the DAC Data Register. If the auto-increment operation is interrupted, the DAC Read Data Address Register must be reinitialized before valid DAC Data reads can continue.

DAC Status Register



Register Type : Read only
Read Port : hex 3C7

Bits 1, 0 : DAC Read/Write Status.

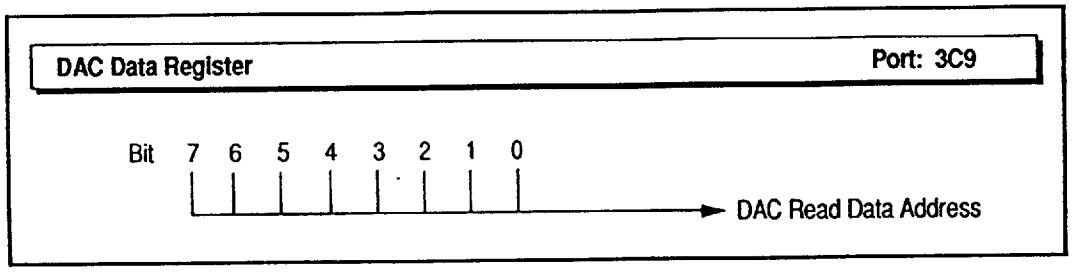
Bits 1 0

0 0 : Indicates the last DAC Data Register operation was a processor write. The value obtained by reading processor port hex 3C8 should be written to the DAC Write Data Address Register (hex 3C8).

1 1 : Indicates the DAC Read Address Register was the last DAC Address Register initialized and the last DAC Data Register operation was a processor read. The valueobtained by reading processor port hex 3C8 should be written to the DAC Read Data Address Register (hex 3C7).

Note : The DAC Status Register contains the Read/Write data state of the DAC's Color Look-up Table. This register is unaffected by read or write operations to the DAC Pixel Mask Register. The value of this register can be used to determine which DAC Address Register needs to be reinitialized if auto- increment is in use and the data Read/Write sequence is interrupted. This register cannot be used to determine the state of the three byte read/write sequences to the DAC Data Registers (red, green, and blue color data). If this three byte sequence is interrupted before all three values have been read or written, the state of the video DAC cannot be restored. Any DAC Data Register operations performed without first reinitializing the corresponding DAC Address register will produce unpredictable results. Interrupts should be disabled during the DAC Data Register read/write sequence.

DAC Data Register

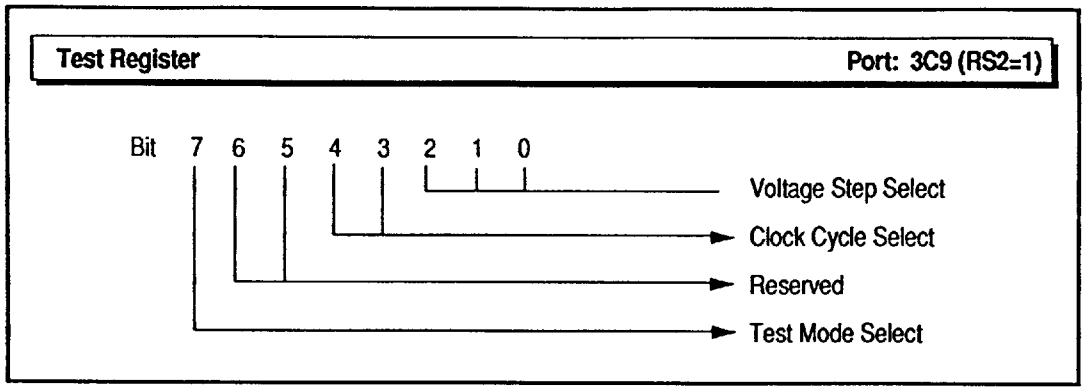


Register Type : Read/Write
Read/Write Port : hex 3C9

Bits 7 - 0: DAC Data Bits. A binary value of the data written to or read from the DAC palette location specified by the corresponding DAC Address Register. A separate processor I/O must be performed, in sequence, for each byte of red, green, and blue color data. The value written determines the level of the analog signal to be output for that color, with a value of hex 00 being the lowest level. A value of hex 3F written to the red, green, and blue data registers in the Color-look-up Table would result in maximum intensified white being output for that particular DAC address. After the three processor I/O's have been performed for the red, green, and blue data, the corresponding DAC Address Register is automatically incremented. Interrupting the video DAC during the three processor data sequence and when the auto-increment capability is in use, will cause the video DAC to enter an unknown state and data integrity cannot beguaranteed. To continue read or write operations the corrsponding DAC Address must be reinitialized. When writing to the DAC Data Register, bits 6 and 7 should be set to zero.

Note : This register is used in conjunction with the DAC Write Address Register and the DAC ReadAddress Register.

Test Register



Register Type: Read/Write
Port: 3C9 (RS2=1)

Bit 7: Test Mode Select.
Logical 0: Selects Test Mode 1. Bits 4-0 of this register are used to generate the test pattern.
Logical 1: Selects Test Mode 2. External test vectors are used to generate test pattern.

Bits 6-5: Reserved

Bits4-3: Determines the number of clock cycles before the next voltage increment.

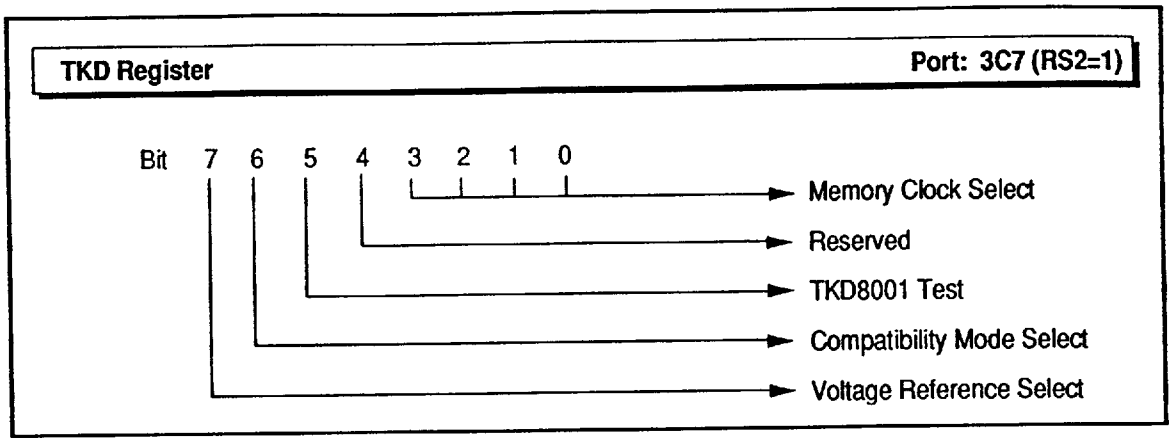
Bit 4	Bit 3	Clock Cycles
0	0	1
0	1	2
1	0	4
1	1	Incremented for each read cycle

Bits 2-0: Determines the number of voltage steps (out of 256) for each voltage increment.

Bit 2	Bit 1	Bit 0	Voltage Steps
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16

All other combinations reserved.

TKD Register



Register Type: Read/Write
Port: 3C7 (RS2=1)

Bit 7: Voltage Reference Select
Logical 0: Selects internal voltage reference.
Logical 1: Selects external voltage reference.

Bit 6: Compatibility mode select for Modes 6 and 7 (see bits 2-0 in Command Register).
Logical 0: Selects Sierra compatibility mode.
Logical 1: Selects AT&T compatibility mode.

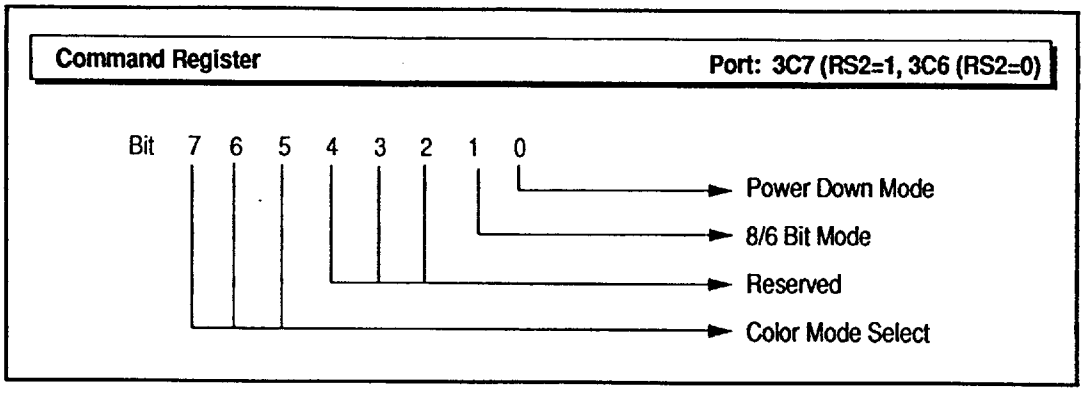
Bit 5: Enable/Disable DAC test mode.
Logical 0: Disables DAC test mode.
Logical 1: Enables DAC test mode.

Bit 4: Reserved.

Bits 3-0: Memory Clock Select Bits

Bit 3	Bit 2	Bit 1	Bit 0	Memory Clock Frequency (MHz)
0	0	0	0	80.0
0	0	0	1	Reserved
0	0	1	0	75.0
0	0	1	1	90.0
0	1	0	0	58.8
0	1	0	1	50.4
0	1	1	0	67.2
0	1	1	1	42.0
1	0	0	0	61.6
1	0	0	1	52.8
1	0	1	0	70.4
1	0	1	1	44.0
1	1	0	0	56.0
1	1	0	1	48.0
1	1	1	0	64.0
1	1	1	1	40.0

Command Register



Register Type: Read/Write
Port: 3C7 (when RS2=1), 3C6(when RS2=0), see Note 1 of Register Selection Summary table on page 2 for additional details

Bit 7-5: Color Mode Select.

Bit 7	Bit 6	Bit 5	Description	Gamma Corrected	Clocks/ Pixel	Pixel Format	Compatibility
0	0	0	Mode 0, 8-bit pseudo	Yes	1	---	Default
0	0	1	Mode 1, 15-bit true	Yes	2	5:5:5	
0	1	0	Mode 2, 24-bit true	Yes	3	8:8:8	
0	1	1	Mode 3, 16-bit true	Yes	2	5:6:5	
1	0	0	Mode 4, 15-bit bypass	No	1	5:5:5	HiColor1
0	1	1	Mode 5, 15-bit bypass	No	2	5:5:5	HiColor2
1	1	0	Mode 6, 24-bit bypass	No	3	8:8:8	Sierra
1	1	1	Mode 7, 16-bit bypass	No	2	5:6:5	Sierra, XGA2
1	1	0	Mode 6, 16-bit bypass	No	2	5:6:5	AT&T, XGA2
1	1	1	Mode 7, 24-bit bypass	No	3	8:8:8	AT&T

Bits 4-2: Reserved

Bit 1: 8/6-bit Mode.
Logical 0: Selects 6-bit mode.
Logical 1: Selects 8-bit mode.

Bit 0: Power Down Mode.
Logical 0: Disables power down mode.
Logical 1: Enables power down mode.

Table 2. Hardware Selectable VCLK Frequencies for the TKD8001

CS4	CS3	CS2	CS1	Frequency (MHz)
0	0	0	0	25.175
0	0	0	1	28.322
0	0	1	0	44.900
0	0	1	1	36.000
0	1	0	0	57.270
0	1	0	1	65.000
0	1	1	0	50.350
0	1	1	1	40.000
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	72.000
1	1	0	1	77.000
1	1	1	0	80.000
1	1	1	1	75.000

Table 3. Hardware Selectable MCLK Frequencies for the TKD8001

MC2	MC1	MC0	Frequency (MHz)
0	0	0	75.000
0	0	1	90.000
0	1	0	80.000
0	1	1	Reserved
1	0	0	64.000
1	0	1	40.000
1	1	0	56.000
1	1	1	48.000

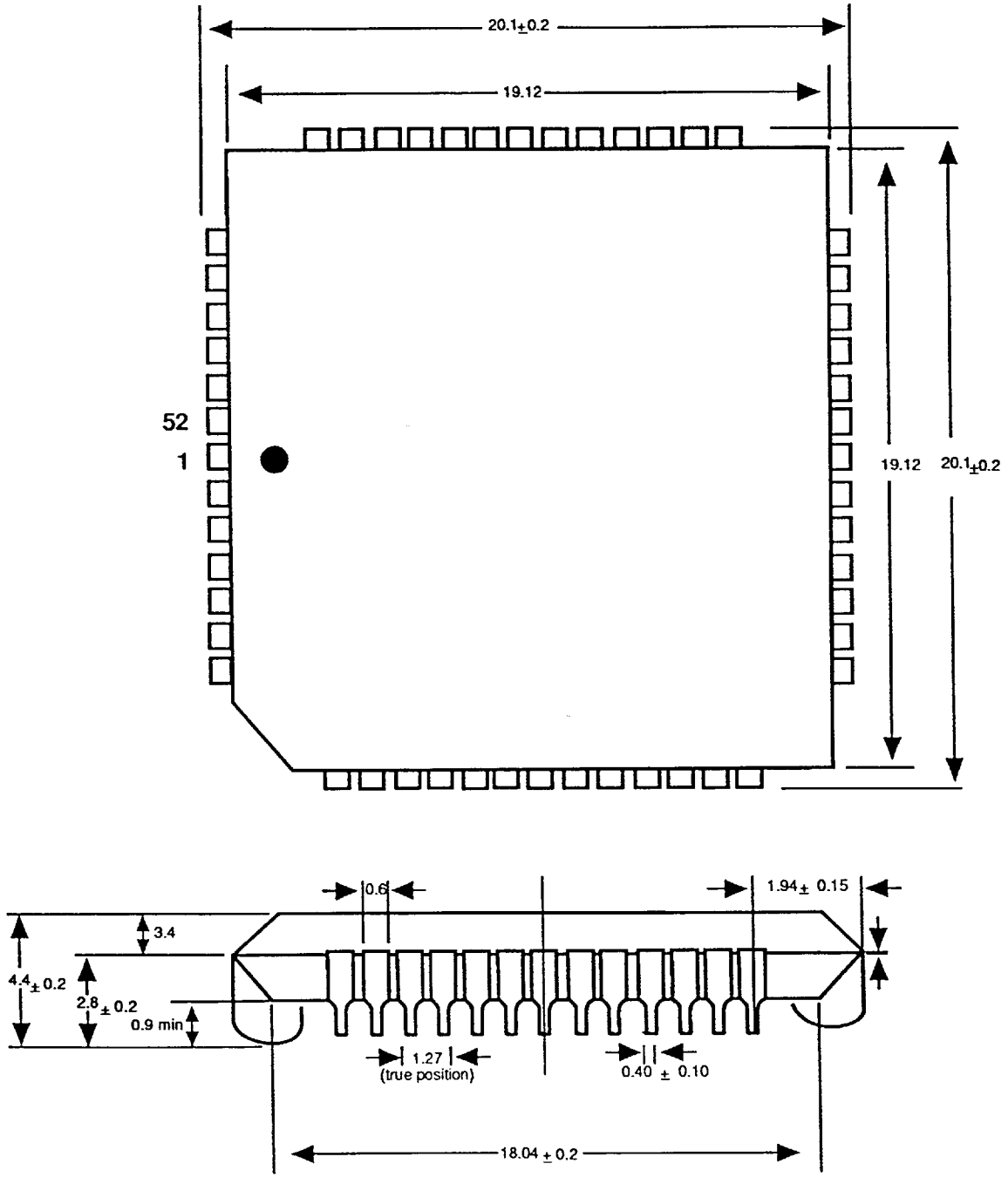


Figure 2. TKD8001 Packaging Diagram
(dimensions in mm)