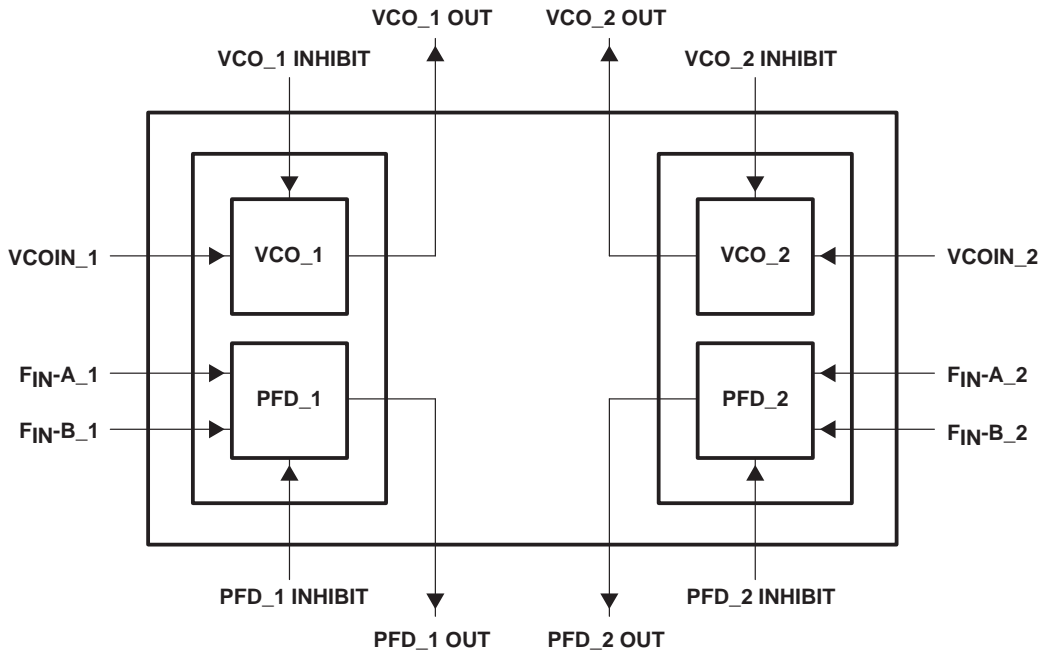


TLC2943 HIGH-PERFORMANCE DUAL PHASE-LOCKED BUILDING BLOCK

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functional block diagram



TLC2943

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	8, 31		Common GND for chip 1
	12, 27		Common GND for chip 2
F _{IN-A_1} , F _{IN-B_1}	4 5	I	Reference frequency signal input and comparison frequency signal input for PFD ₁ . f _{REF-IN_1} inputs to F _{IN-A_1} , and comparison frequency input from external counter logic to F _{IN-B_1} , for a lag-lead filter use as LPF.
F _{IN-A_2} , F _{IN-B_2}	16 17	I	Reference frequency signal input and comparison frequency signal input for PFD ₂ . f _{REF-IN_2} inputs to F _{IN-A_2} , and comparison frequency input from external counter logic to F _{IN-B_2} , for a lag-lead filter use as LPF.
LOGIC ₁ GND	7		Ground for the internal logic of chip 1
LOGIC ₂ GND	19		Ground for the internal logic of chip 2
LOGIC ₁ V _{DD}	1		Power supply for the internal logic of chip 1. This power supply should be separate from VCO V _{DD} to reduce cross-coupling between supplies.
LOGIC ₂ V _{DD}	13		Power supply for the internal logic of chip 2. This power supply should be separate from VCO V _{DD} to reduce cross-coupling between supplies.
NC	9, 10, 11, 20, 28, 29, 30, 32		No internal connection
PFD ₁ INHIBIT	33	I	PFD inhibit control for chip 1. When PFD ₁ INHIBIT is high, PFD ₁ OUT is in the high-impedance state, see Table 2.
PFD ₂ INHIBIT	21	I	PFD inhibit control for chip 2. When PFD ₂ INHIBIT is high, PFD ₂ OUT is in the high-impedance state, see Table 2.
PFD ₁ OUT	6	O	PFD output of chip 1. When the PFD ₁ INHIBIT is high, PFD ₁ OUT is in the high-impedance state.
PFD ₂ OUT	18	O	PFD output of chip 2. When the PFD ₂ INHIBIT is high, PFD ₂ OUT is in the high-impedance state.
R _{BIAS_1}	37	I	Bias supply for VCO ₁ . An external resistor (R _{BIAS}) between VCO ₁ V _{DD} and BIAS ₁ supplies bias for adjusting the oscillation frequency range of VCO ₁ .
R _{BIAS_2}	25	I	Bias supply for VCO ₂ . An external resistor (R _{BIAS}) between VCO ₂ V _{DD} and BIAS ₂ supplies bias for adjusting the oscillation frequency range of VCO ₂ .
TEST ₁	2		Test terminal. TEST connects to LOGIC ₁ GND for normal operation.
TEST ₂	14		Test terminal. TEST connects to LOGIC ₂ GND for normal operation.
VCO ₁ GND	35		GND for VCO ₁
VCO ₂ GND	23		GND for VCO ₂
VCO ₁ INHIBIT	34	I	VCO inhibit control for chip 1. When VCO ₁ INHIBIT is high, VCO ₁ OUT is low (see Table 1).
VCO ₂ INHIBIT	22	I	VCO inhibit control for chip 2. When VCO ₂ INHIBIT is high, VCO ₂ OUT is low (see Table 1).
VCO ₁ OUT	3	O	VCO output of chip 1. When VCO ₁ INHIBIT is high, VCO ₁ OUT is low.
VCO ₂ OUT	15	O	VCO output of chip 2. When VCO ₂ INHIBIT is high, VCO ₂ OUT is low.
VCO ₁ V _{DD}	38		Power supply for VCO ₁ . This power supply should be separate from LOGIC V _{DD} to reduce cross-coupling between supplies.
VCO ₂ V _{DD}	26		Power supply for VCO ₂ . This power supply should be separate from LOGIC V _{DD} to reduce cross-coupling between supplies.
VCOIN ₁	36	I	VCO ₁ control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCOIN ₂	24	I	VCO ₂ control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.

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detailed description

MCM (multichip module) technology for TLC2943

The TLC2943 is a multichip module (MCM) product that uses two TLC2933 chips. Inside the package, two chips are completely isolated by a special formed lead-frame. Therefore, when using the TLC2943 in two asynchronous PLL circuits, there is no performance degradation by electrical interference between chips inside the package. So, the same performance as TLC2933 can be easily expected by using TLC2943.

The NC terminals in the middle on both sides of the package are to achieve complete isolation inside the package. To get the best performance from this MCM technology, it is better to make a careful board layout of the external power supply, ground, and signal lines.

voltage controlled oscillator (VCO)

VCO_1 and VCO_2 have the same typical characteristics. Each VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depend on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 2.2 k Ω with $V_{DD} = 3.3$ V and nominally 2.4 k Ω with $V_{DD} = 5$ V. For the lock frequency range, refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

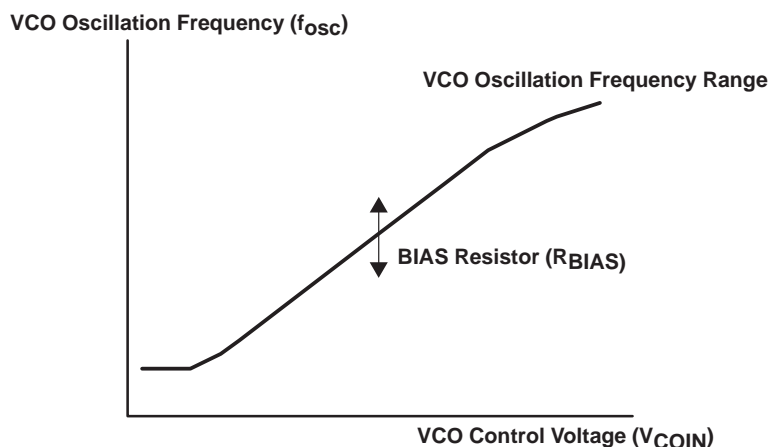


Figure 1. VCO_1 and VCO_2 Oscillation Frequency

VCO inhibit function

Each VCO has an externally controlled inhibit function that inhibits the VCO output. The VCO oscillation is stopped during a high level on VCOINHIBIT, so the high level can also be used as the power-down mode. The VCO output maintains a low level during the power-down mode (see Table 1 and Table 2).

Table 1. VCO_1 Inhibit Function

VCO_1 INHIBIT	VCO_1 OSCILLATOR	VCO_1 OUT	VCO_1 I_{DD}
Low	Active	Active	Normal
High	Stop	Low	Power down

Table 2. VCO_2 Inhibit Function

VCO_2 INHIBIT	VCO_2 OSCILLATOR	VCO_2 OUT	VCO_2 I_{DD}
Low	Active	Active	Normal
High	Stop	Low	Power down

detailed description (continued)

phase frequency detector (PFD)

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to F_{IN-A} and F_{IN-B} as shown in Figure 2. Nominally the reference is supplied to F_{IN-A} , and the frequency from the external counter output is fed to F_{IN-B} . For clock recovery PLL systems, other types of phase detectors should be used.

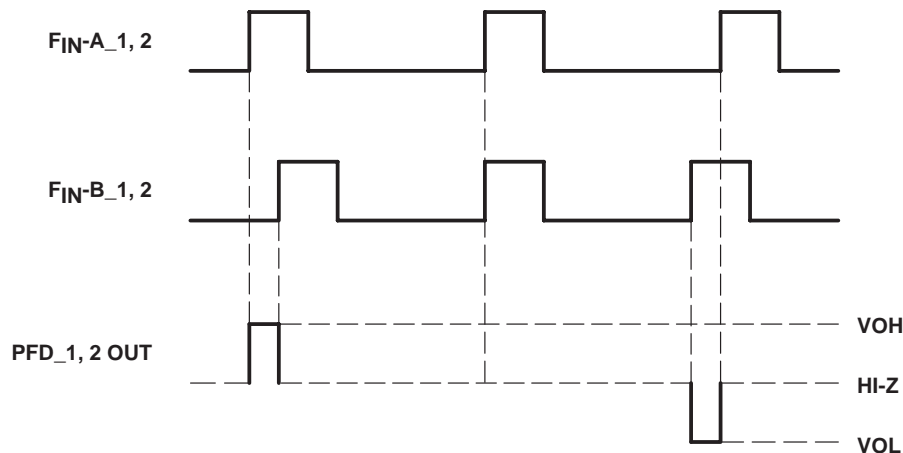


Figure 2. PFD Function Timing Chart

PFD output control

A high level on PFD INHIBIT places the PFD OUT in the high impedance state and the PFD stops phase detection as shown in Table 3 and Table 4. A high level on PFD inhibit also can be used as the power-down mode for the PFD.

Table 3. PFD_1 Inhibit Function

PFD_1 INHIBIT	PFD_1	PFD_1 OUT	PFD_1 I _{DD}
Low	Active	Active	Normal
High	Stop	Hi-Z	Power down

Table 4. PFD_2 Inhibit Function

PFD_2 INHIBIT	PFD_2	PFD_2 OUT	PFD_2 I _{DD}
Low	Active	Active	Normal
High	Stop	Hi-Z	Power down

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internal function block diagram

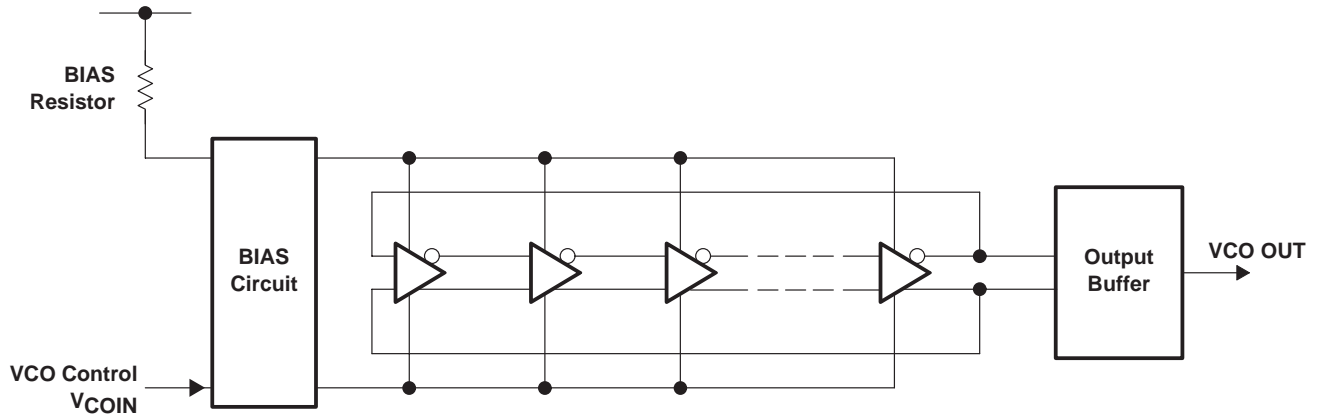


Figure 3. VCO Block Schematic (VCO_1, VCO_2)

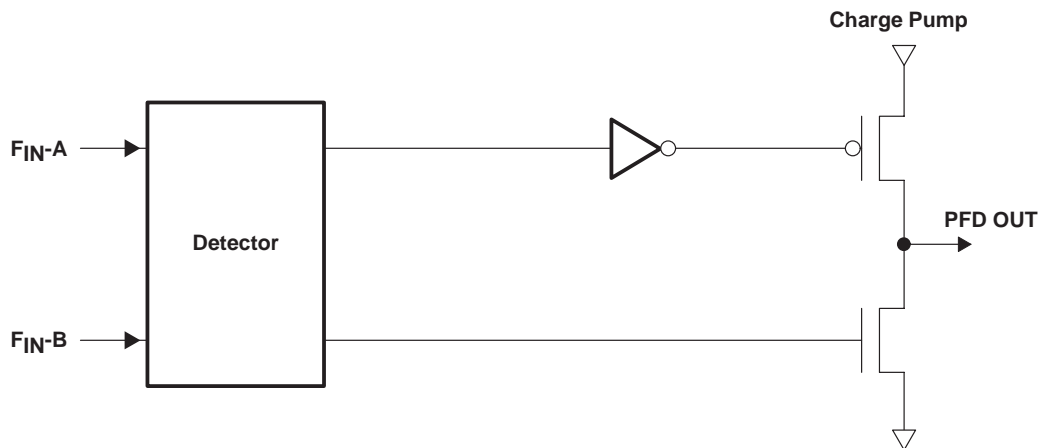


Figure 4. PFD Block Schematic (PFD_1, PFD_2)

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_I (see Note 1)	-0.5 to $V_{DD} + 0.5$ V
Input current (each input), I_I	± 20 mA
Output current (each output), I_O	± 20 mA
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$ (see Note 2)	1160 mW
Operating free-air temperature range, T_A	-20°C to 75°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.
 2. For operation above 25°C free-air temperature, derate linearly at the rate of $9.3\text{ mW}/^\circ\text{C}$.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage (each supply, see Notes 3 and 4), V_{DD}	$V_{DD} = 3\text{ V}$	2.85	3	3.15	V
	$V_{DD} = 3.3\text{ V}$	3.15	3.3	3.45	
	$V_{DD} = 5\text{ V}$	4.75	5	5.25	
Input voltage range (input except for VCOIN_1, 2), V_I		0		V_{DD}	V
Output current (each output), I_O		0		± 2	mA
Control voltage, VCOIN		1		V_{DD}	V
Clock frequency, f	$V_{DD} = 3\text{ V}$	37		55	MHz
	$V_{DD} = 3.3\text{ V}$	37		60	
	$V_{DD} = 5\text{ V}$	43		100	
Oscillation frequency range set resistor (each RBIAS), R_{BIAS} VCO	$V_{DD} = 3\text{ V}$	1.8		2.7	k Ω
	$V_{DD} = 3.3\text{ V}$	1.8		3.0	
	$V_{DD} = 5\text{ V}$	2.2		3.0	
Top operating temperature range		-20		75	$^\circ\text{C}$

- NOTES: 3. It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) be at the same voltage and separated from each other.
 4. Insert bypass capacitors locating the nearest point to each power supply terminal.



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electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.3	V
$V_{(TH+)}$	Positive input threshold voltage		0.9	1.5	2.1	V
I_I	Input current	$V_I = V_{DD}$ or GND			± 1	μA
$Z_{(VCOIN)}$	VCOIN input impedance	$V_{COIN} = 1/2V_{DD}$		10		$\text{M}\Omega$
$I_{DD(INH)}$	VCO supply current (inhibit) (for one chip)	See Note 5		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current (for one chip)	See Note 6		5.1	15	mA

NOTES: 5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.

6. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 2.4\text{ k}\Omega$, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	2.7			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, $V_O = V_{DD}$ or GND			± 1	μA
V_{IH}	High-level input voltage at F_{IN-A} , F_{IN-B}		2.1			V
V_{IL}	Low-level input voltage at F_{IN-A} , F_{IN-B}				0.9	V
$V_{(TH+)}$	Positive input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_I	Input capacitance at F_{IN-A} , F_{IN-B}			5		pF
Z_I	Input impedance at F_{IN-A} , F_{IN-B}			10		$\text{M}\Omega$
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.7	4	mA

NOTE 7: The current into LOGIC V_{DD} when F_{IN-A} and $F_{IN-B} = 30\text{ MHz}$ ($V_{I(PP)} = 3\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.



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electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 3.3\text{ V}$ (unless otherwise noted) (continued)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	2.7			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.4	V
$V_{(TH+)}$	Positive input threshold voltage		1	1.65	2.3	V
I_I	Input current	$V_I = V_{DD}$ or GND			± 1	μA
$Z_{(VCOIN)}$	VCOIN input impedance	$V_{COIN} = 1/2V_{DD}$		10		$\text{M}\Omega$
$I_{DD(INH)}$	VCO supply current (inhibit) (for one chip)	See Note 5		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current (for one chip)	See Note 6		6.2	16	mA

- NOTES: 5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.
 6. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 2.4\text{ k}\Omega$, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	3			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, $V_O = V_{DD}$ or GND			± 1	μA
V_{IH}	High-level input voltage at F_{IN-A} , F_{IN-B}		2.3			V
V_{IL}	Low-level input voltage at F_{IN-A} , F_{IN-B}				1	V
$V_{(TH+)}$	Positive input threshold voltage at PFD INHIBIT		1	1.65	2.3	V
C_I	Input capacitance at F_{IN-A} , F_{IN-B}			5		pF
Z_I	Input impedance at F_{IN-A} , F_{IN-B}			10		$\text{M}\Omega$
$I_{DD(PFD)}$	PFD supply current	See Note 8		0.8	5	mA

- NOTE 8: The current into LOGIC V_{DD} when F_{IN-A} and $F_{IN-B} = 30\text{ MHz}$ ($V_I(PP) = 3.3\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

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electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\text{ V}$ (unless otherwise noted) (continued)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	4.5			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.5	V
$V_{(TH+)}$	Positive input threshold voltage		1.5	2.5	3.5	V
I_I	Input current	$V_I = V_{DD}$ or GND			± 1	μA
$Z_{(VCOIN)}$	VCOIN input impedance	$V_{COIN} = 1/2V_{DD}$		10		$\text{M}\Omega$
$I_{DD(INH)}$	VCO supply current (inhibit) (for one chip)	See Note 5		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current (for one chip)	See Note 6		14	35	mA

NOTES: 5. The current into VCO V_{DD} and LOGIC V_{DD} when VCO INHIBIT = V_{DD} and PFD INHIBIT is high.

6. The current into VCO V_{DD} and LOGIC V_{DD} when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 2.4\text{ k}\Omega$, VCO INHIBIT = ground, and PFD INHIBIT is high.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$	4.5			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
I_{OZ}	High-impedance state output current	PFD INHIBIT = high, $V_O = V_{DD}$ or GND			± 1	μA
V_{IH}	High-level input voltage at F_{IN-A} , F_{IN-B}		3.5			V
V_{IL}	Low-level input voltage at F_{IN-A} , F_{IN-B}				1.5	V
$V_{(TH+)}$	Positive input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_I	Input capacitance at F_{IN-A} , F_{IN-B}			7		pF
Z_I	Input impedance at F_{IN-A} , F_{IN-B}			10		$\text{M}\Omega$
$I_{DD(PFD)}$	PFD supply current	See Note 9		2.6	8	mA

NOTE 9: The current into LOGIC V_{DD} when F_{IN-A} and $F_{IN-B} = 50\text{ MHz}$ ($V_I(PP) = 5\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.



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operating characteristics at $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$f_{(OSC)}$	Oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1/2V_{DD}$	38	48	58	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 10			10	μs
t_r	Output rise time	$C_L = 15\text{ pF}$, See Figure 5		3.3	10	ns
t_f	Output fall time	$C_L = 15\text{ pF}$, See Figure 5		2	8	ns
$f_{(DUTY)}$	Duty cycle	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1/2V_{DD}$	45%	50%	55%	
$f_{(TA)}$	Temperature coefficient of oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1/2V_{DD}$ Top = -20°C to 75°C		0.03		$\%/^\circ\text{C}$
$f_{(VDD)}$	Supply voltage coefficient of oscillation frequency supply	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1.5\text{ V}$, $V_{DD} = 2.85\text{ V}$ to 3.15 V		0.04		$\%/mV$

NOTE 10: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{MAX}	Maximum operating frequency		30			MHz
t_{PLZ}	PFD output disable time from low level	See Figure 6 and Figure 7, and Table 5		20	40	ns
t_{PHZ}	PFD output disable time from high level			18	40	
t_{PZL}	PFD output enable time to low level			4.1	18	ns
t_{PZH}	PFD output enable time to high level			4.8	18	
t_r	Rise time	$C_L = 15\text{ pF}$, See Figure 6		3.1	9	ns
t_f	Fall time			1.5	9	

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operating characteristics at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f(OSC)	Oscillation frequency	RBIAS = 2.4 k Ω , VCOIN = 1/2V _{DD}	42	52	62	MHz
t(STB)	Time to stable oscillation	See Note 10			10	μs
t _r	Output rise time	C _L = 15 pF, See Figure 5		3	8	ns
t _f	Output fall time	C _L = 15 pF, See Figure 5		1.9	7	ns
f(DUTY)	Duty cycle	RBIAS = 2.4 k Ω , VCOIN = 1/2V _{DD}	45%	50%	55%	
f(TA)	Temperature coefficient of oscillation frequency	RBIAS = 2.4 k Ω , Top = -20°C to 75°C, VCOIN = 1/2V _{DD}		0.03		%/°C
f(VDD)	Supply voltage coefficient of oscillation frequency supply	RBIAS = 2.4 k Ω , VCOIN = 1.65 V, V _{DD} = 3.15 V to 3.45 V		0.04		%/mV

NOTE 10: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f _{MAX}	Maximum operating frequency		30			MHz
t _{PLZ}	PFD output disable time from low level	See Figure 6 and Figure 7, and Table 5		20	40	ns
t _{PHZ}	PFD output disable time from high level			18	40	
t _{PZL}	PFD output enable time to low level				16	ns
t _{PZH}	PFD output enable time to high level				16	
t _r	Rise time	C _L = 15 pF, See Figure 6			8	ns
t _f	Fall time				8	

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operating characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$f_{(OSC)}$	Oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1/2V_{DD}$	64	80	96	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 10			10	μs
t_r	Output rise time	$C_L = 15\text{ pF}$, See Figure 5		2.1	5	ns
t_f	Output fall time	$C_L = 15\text{ pF}$, See Figure 5		1.5	4	ns
$f_{(DUTY)}$	Duty cycle	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1/2V_{DD}$	45%	50%	55%	
$f_{(TA)}$	Temperature coefficient of oscillation frequency	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 1/2V_{DD}$ Top = -20°C to 75°C		0.03		$\%/^\circ\text{C}$
$f_{(VDD)}$	Supply voltage coefficient of oscillation frequency supply	$R_{BIAS} = 2.4\text{ k}\Omega$, $V_{COIN} = 2.5\text{ V}$, $V_{DD} = 4.75\text{ V}$ to 5.25 V		0.02		$\%/mV$

PFD section

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{MAX}	Maximum operating frequency		50			MHz
t_{PLZ}	PFD output disable time from low level	See Figure 6 and Figure 7, and Table 5		20	40	ns
t_{PHZ}	PFD output disable time from high level			17	40	
t_{PZL}	PFD output enable time to low level			3.7	10	ns
t_{PZH}	PFD output enable time to high level			3.5	10	
t_r	Rise time	$C_L = 15\text{ pF}$, See Figure 6		1.7	5	ns
t_f	Fall time			1.3	5	

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PARAMETER MEASUREMENT INFORMATION

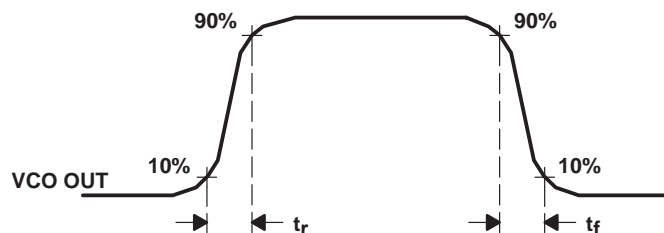


Figure 5. VCO Output Voltage Waveform (Each VCO)

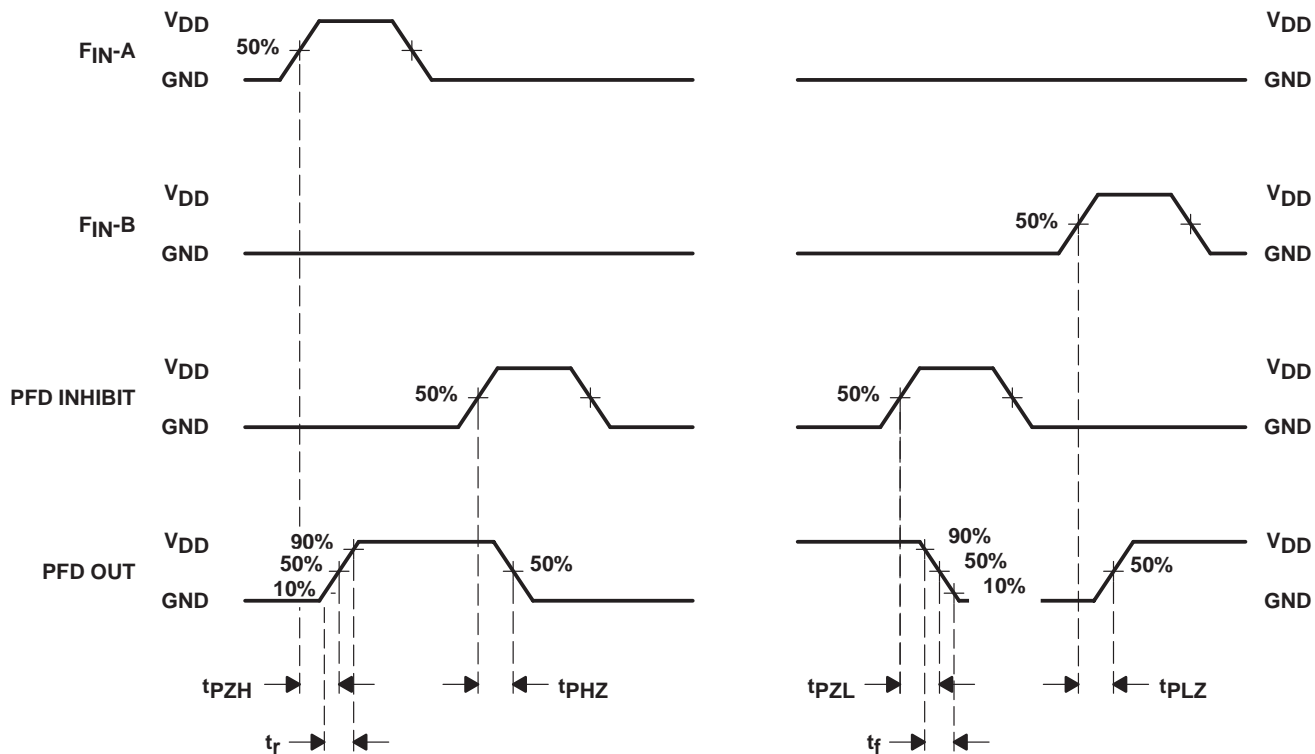


Figure 6. PFD Output Voltage Waveform

PARAMETER MEASUREMENT INFORMATION

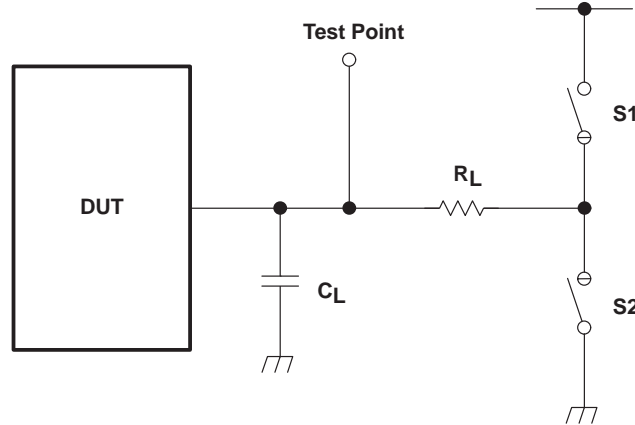


Figure 7. PFD Output Test Conditions

Table 5. PFD Output Test Conditions

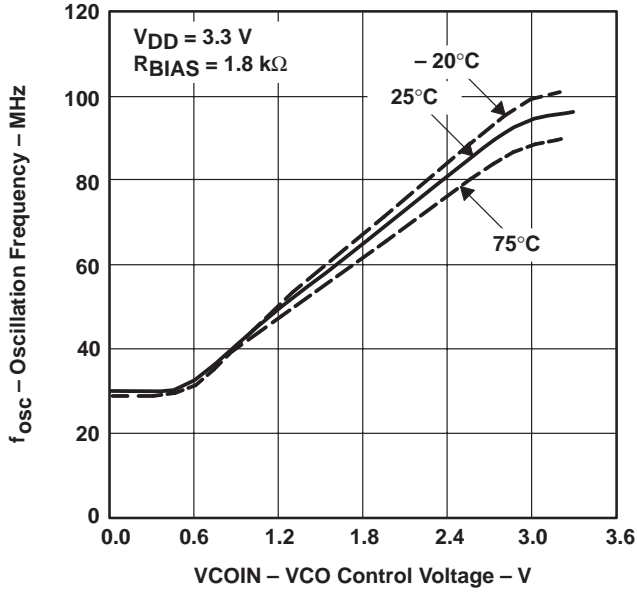
PARAMETER	R_L	C_L	S1	S2
t_{PZH}	1 k Ω	15 pF	OPEN	CLOSE
t_{PHZ}				
t_r				
t_{PZL}			CLOSE	OPEN
t_{PLZ}				
t_f				

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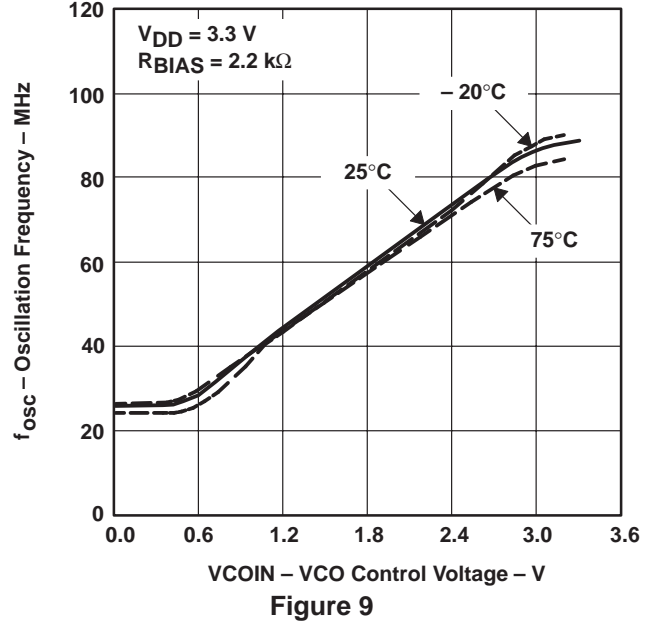
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TYPICAL CHARACTERISTICS

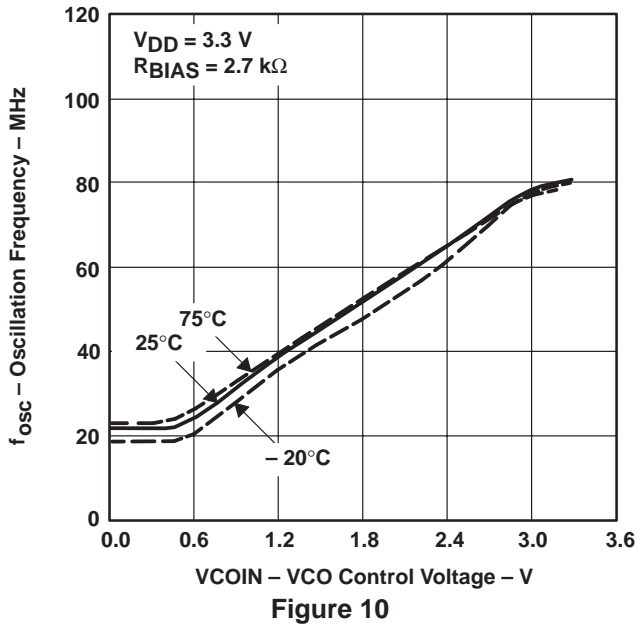
OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE



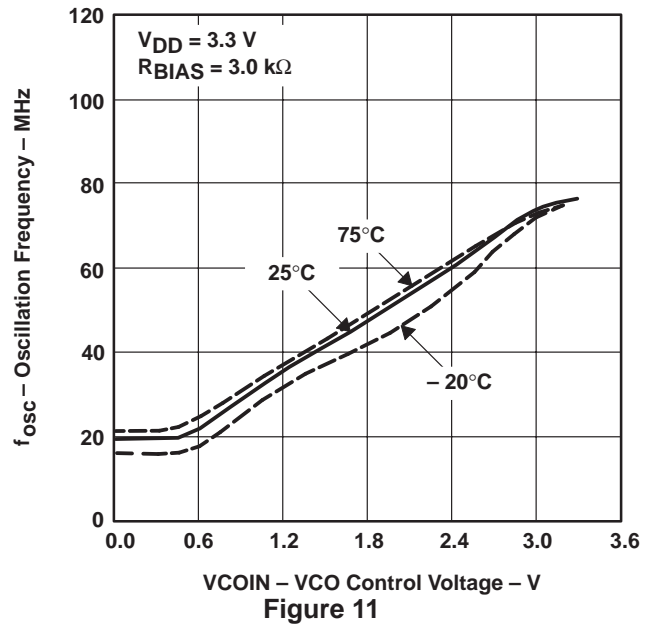
OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE



OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE



OSCILLATION FREQUENCY
vs
CONTROL VOLTAGE



TYPICAL CHARACTERISTICS

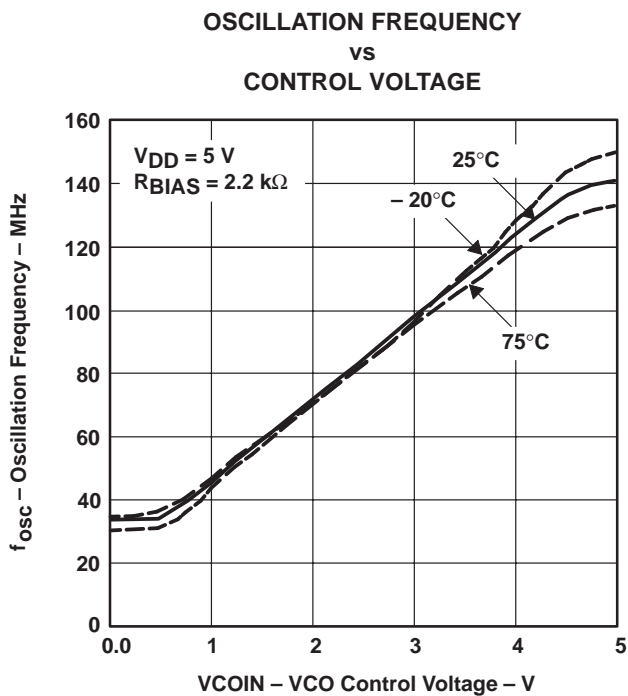


Figure 12

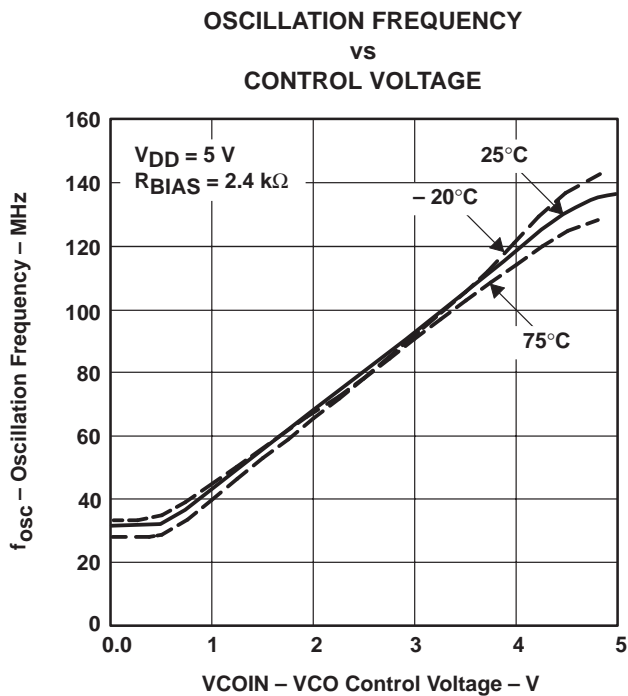


Figure 13

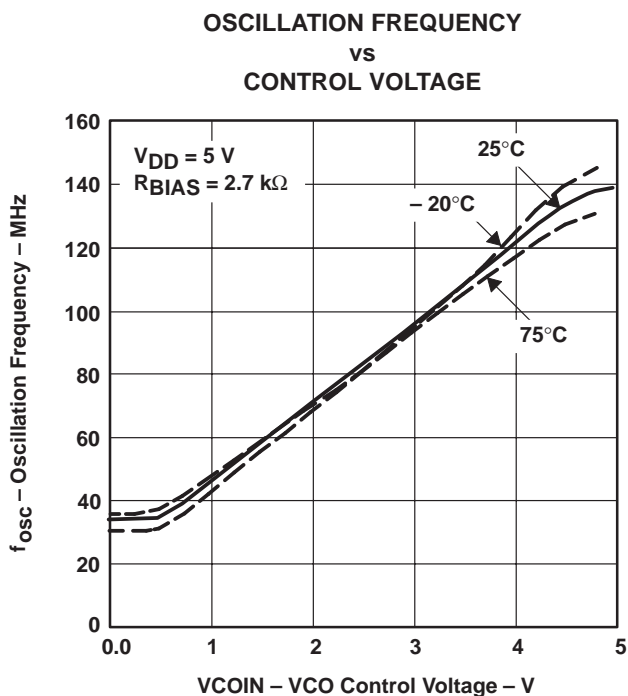


Figure 14

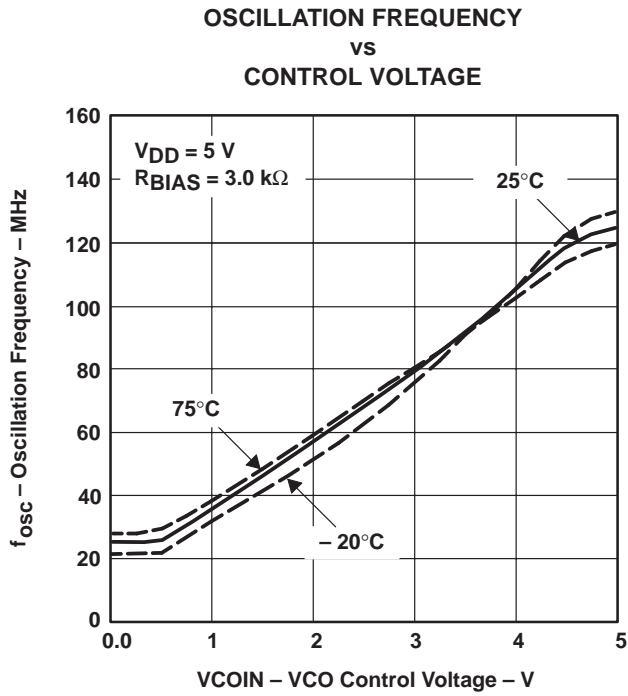


Figure 15

TLC2943 HIGH-PERFORMANCE DUAL PHASE-LOCKED BUILDING BLOCK

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TYPICAL CHARACTERISTICS

LOCK FREQUENCY RANGE
vs
BIAS RESISTANCE

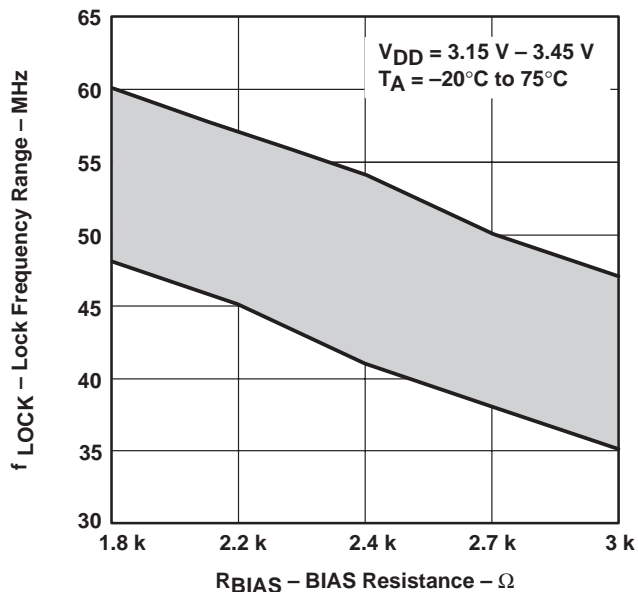


Figure 16

LOCK FREQUENCY RANGE
vs
BIAS RESISTANCE

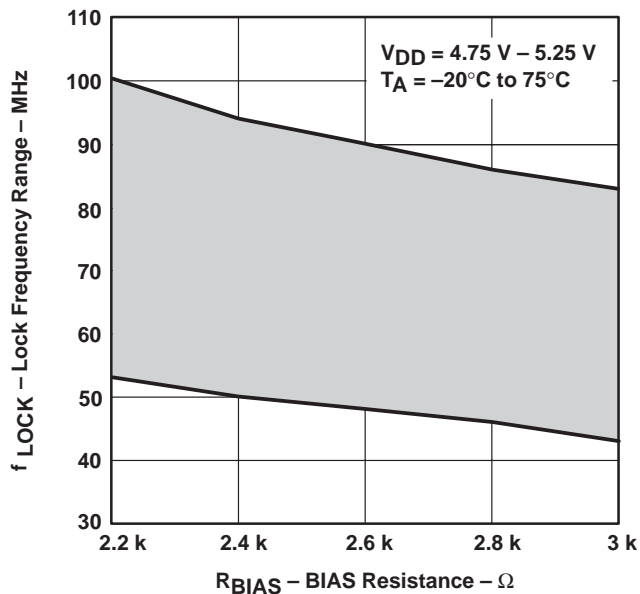


Figure 17

APPLICATION INFORMATION

gain of VCO and PFD

Figure 18 is a block diagram of the PLL. The divider N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 18. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 18(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 18(c).

The parameters for the block diagram with the units are as follows:

- K_V : VCO gain (rad/s/V)
- K_p : PFD gain (V/rad)
- K_f : LPF gain (V/V)
- K_N : countdown divider gain (1/N)

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

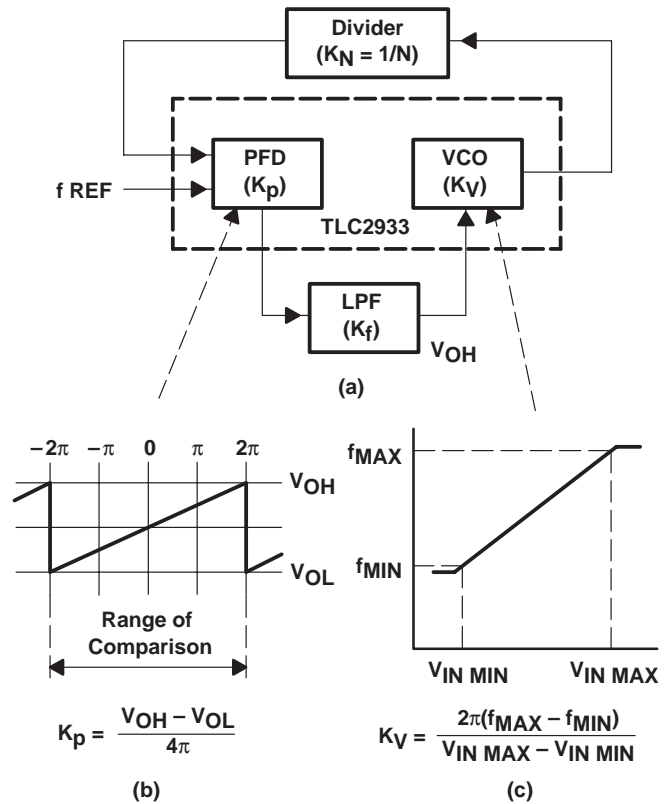


Figure 18. Example of a PLL Block Diagram

R_{BIAS}

The external bias resistor sets the VCO center frequency with $1/2 V_{DD}$ applied to the VCO IN terminal. For the most accurate results, a metal-film resistor is the better choice, but a carbon-composition resistor can also be used with excellent results. A $0.22 \mu\text{F}$ capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 17 is as follows:

$$\Delta\omega_H \approx 0.8 (K_p) (K_V) (K_f(\infty)) \tag{1}$$

Where

$K_f(\infty)$ = the filter transfer function value at $\omega = \infty$

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

References that include detailed design information about LPFs should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 19. When the active filter of Figure 19(c) is used, the reference should be applied to F_{IN}-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

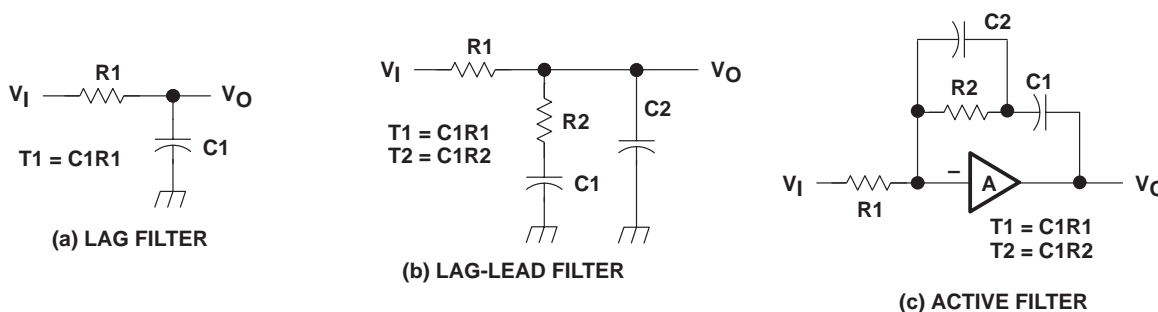


Figure 19. LPF Examples for PLL

passive filter

The transfer function for the low-pass filter shown in Figure 17(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \times T2}{1 + s \times (T1 + T2)} \tag{2}$$

Where

$$T1 = R1 \times C1 \text{ and } T2 = R2 \times C1$$

Using this filter makes the closed-loop PLL system a type 1 second-order system. The response curves of this system to a unit step are shown in Figure 20.

active filter

When using the active filter shown in Figure 19(c), the phase detector inputs must be reversed, since the filter adds an additional inversion. Therefore, the input reference frequency should be applied to the F_{IN}-B terminal and the output of the VCO divider should be applied to the input reference terminal, F_{IN}-A.

The transfer function for the active filter shown in Figure 19(c) is:

$$F(s) = \frac{1 + s \times R2 \times C1}{s \times R1 \times C1} \tag{3}$$

Using this filter makes the closed-loop PLL system a type 2 second-order system. The response curves of this system to a unit step are shown in Figure 21.

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Using the lag-lead filter in Figure 19(b) and divider N value, the transfer function for phase and frequency are shown in equations 4 and 5. Note that the transfer function for phase differs from the transfer function for frequency by only the divider N value. The difference arises from the fact that the feedback for phase is unity, while the feedback for frequency is 1/N.

Hence, the transfer function of Figure 19(a) for phase is

$$\frac{\Phi_2(s)}{\Phi_1(s)} = \frac{K_p \times K_V}{N \times (T_1 + T_2)} \left[\frac{1 + s \times T_2}{s^2 + s \left[1 + \frac{K_p \times K_V \times T_2}{N \times (T_1 + T_2)} \right] + \frac{K_p \times K_V}{N \times (T_1 + T_2)}} \right] \quad (4)$$

and the transfer function for frequency is

$$\frac{F_{OUT}(s)}{F_{REF}(s)} = \frac{K_p \times K_V}{(T_1 + T_2)} \left[\frac{1 + s \times T_2}{s^2 + s \times \left[1 + \frac{K_p \times K_V \times T_2}{N \times (T_1 + T_2)} \right] + \frac{K_p \times K_V}{N \times (T_1 + T_2)}} \right] \quad (5)$$

The standard 2-pole denominator is $D = s^2 + 2 \zeta \omega_n s + \omega_n^2$ and comparing the coefficients of the denominator of equation (4) and (5) with the standard 2-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \times K_V}{N \times (T_1 + T_2)}} \quad (6)$$

Solving for $T_1 + T_2$

$$T_1 + T_2 = \frac{K_p \times K_V}{N \times \omega_n^2}$$

and by using this value for $T_1 + T_2$ in equation (6) the damping factor is

$$\zeta = \frac{\omega_n}{2} \times \left(T_2 + \frac{N}{K_p \times K_V} \right) \quad (7)$$

solving for T_2

$$T_2 = \frac{2 \zeta}{\omega_n} - \frac{N}{K_p \times K_V} \quad (8)$$

then by substituting for T_2 in equation (6)

$$T_1 = \frac{K_V \times K_p}{N \times \omega_n^2} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \times K_V} \quad (9)$$

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From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2 \zeta}{\omega_n} - \frac{N}{K_p \times K_V} \right] \frac{1}{C1} \quad (10)$$

$$R1 = \left[\frac{K_p \times K_V}{\omega_n^2 \times N} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \times K_V} \right] \frac{1}{C1} \quad (11)$$

The capacitor, C1, is usually chosen between 1 μ F and 0.1 μ F to allow for reasonable resistor values and physical capacitor size.

APPLICATION INFORMATION

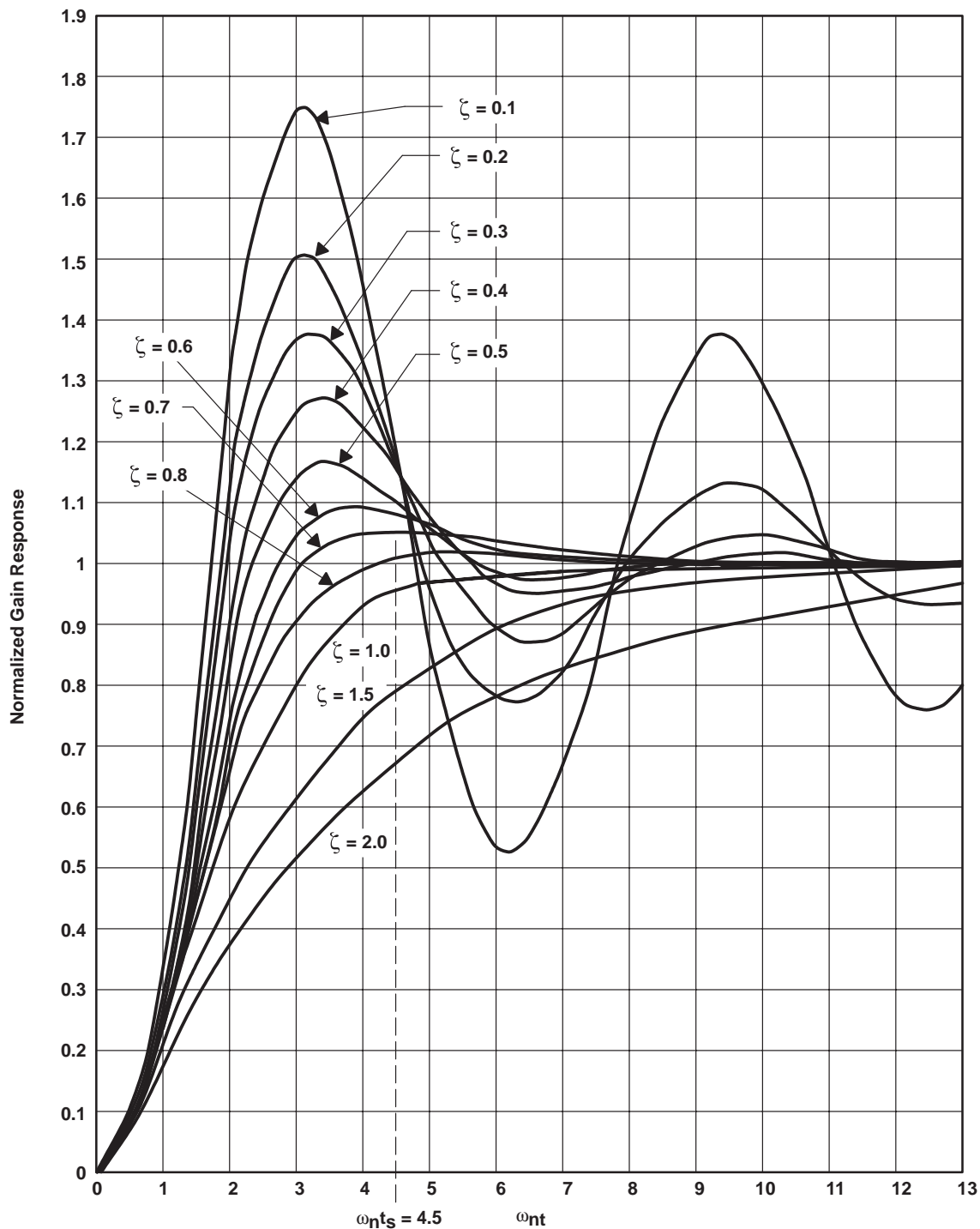


Figure 20. Type 1 Second-Order Step Response

APPLICATION INFORMATION

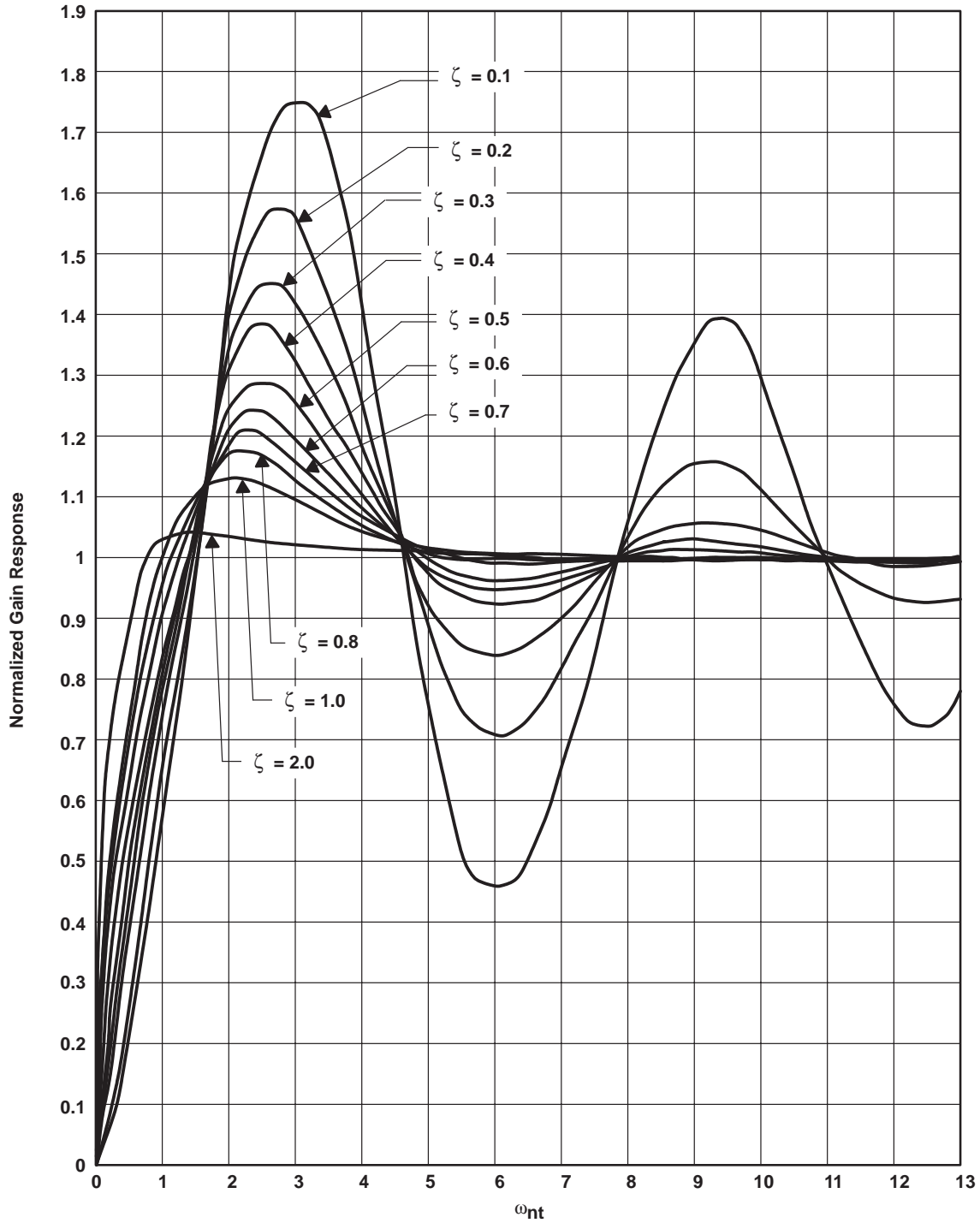


Figure 21. Type 2 Second-Order Step Response

APPLICATION INFORMATION

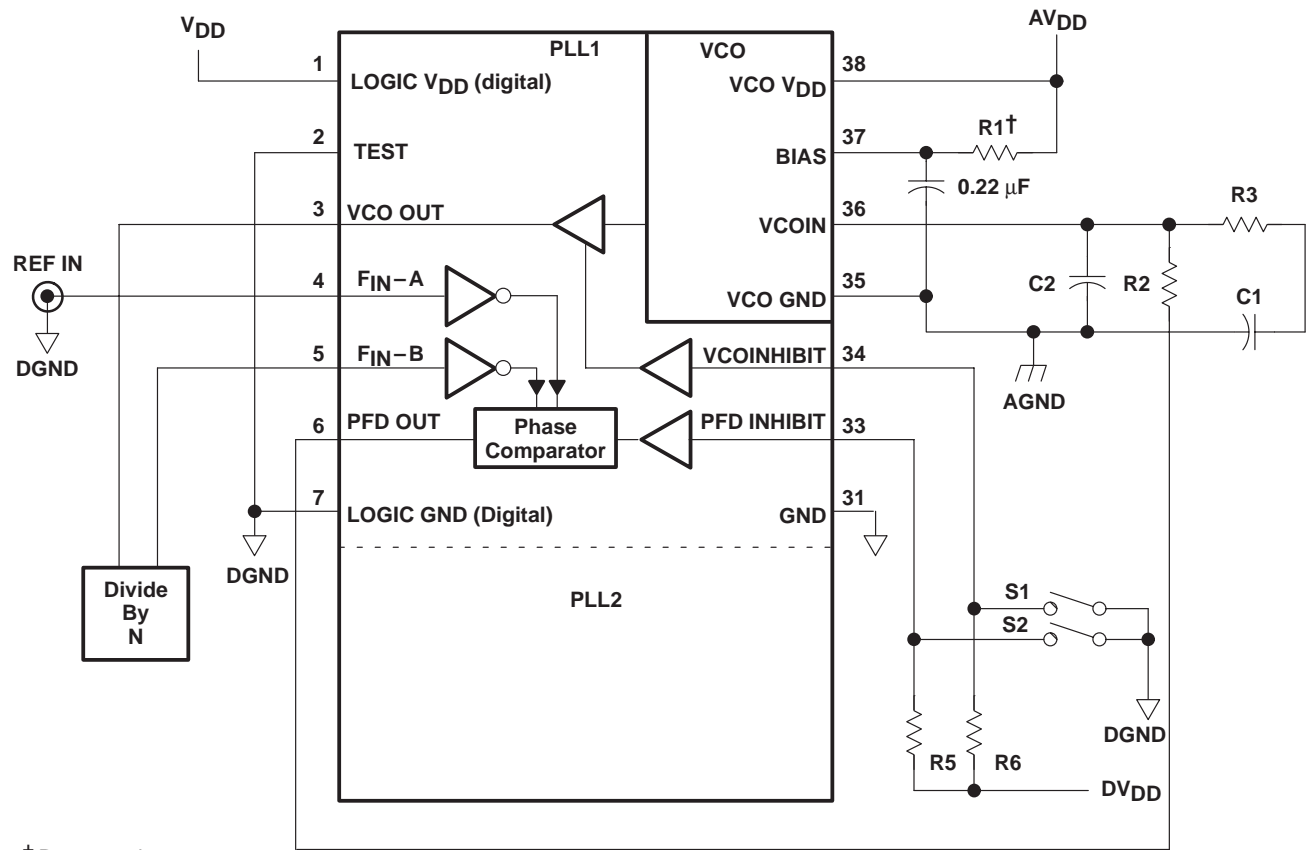
PCB layout considerations

The TLC2943 contains high frequency analog oscillators; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

The following design recommendations benefit the TLC2943 user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1- μF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

The evaluation and operation schematic for the TLC2943 is shown in Figure 22.



† R_{BIAS} resistor

Figure 22. Evaluation and Operation Schematic

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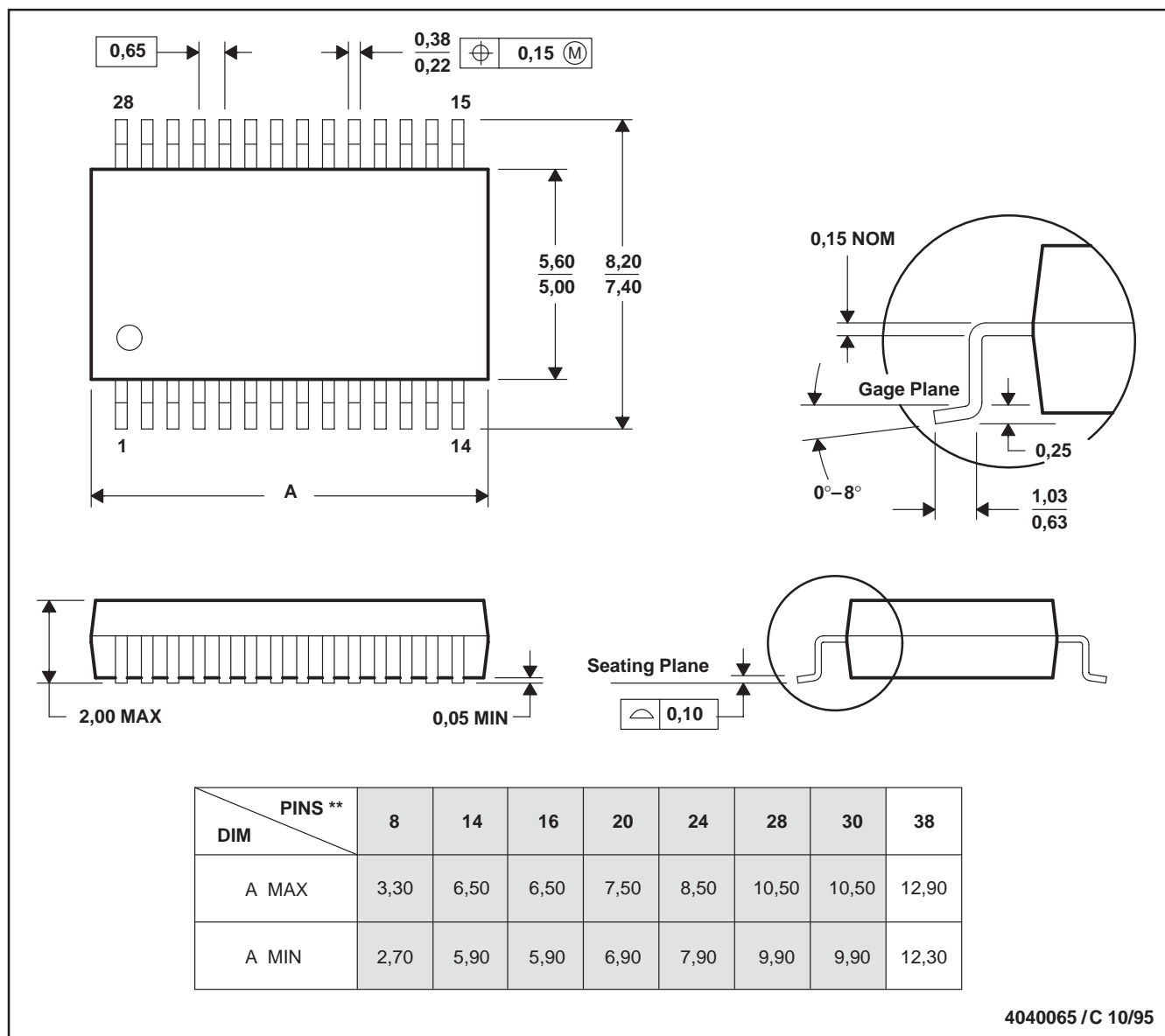
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MECHANICAL DATA

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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