- **LinEPIC™ 1-μm CMOS Process**
- **125-MHz Pipelined Architecture**
- **Available Clock Rates . . . 80, 110, 125, 135 MHz**
- **Dual-Port Color RAM 256 Words x 24 Bits**
- **Bit Plane Read and Blink Masks**
- **EIA RS-343-A Compatible Outputs**
- **Functionally Interchangeable With Brooktree® Bt458**
- **Direct Interface to TMS340XX Graphics Processors**
- **Standard Microprocessor Unit (MPU) Palette Interface**
- **Multiplexed TTL Pixel Ports**
- **Triple Digital-to-Analog Converters (DACs)**
- **Dual-Port Overlay Registers . . . 4 × 24 Bits**
- **5-V Power Supply**

description

The TLC34058 color-palette integrated circuit is specifically developed for high-resolution color graphics in such applications as CAE/CAD/CAM, image processing, and video reconstruction.

The architecture provides for the display of 1280 × 1024 bit-mapped color graphics (up to 8 bits per pixel resolution) with 2 bits of overlay information. The TLC34058 has a 256-word × 24-bit RAM used as a lookup table with three 8-bit video D/A converters.

On-chip features such as high-speed pixel clock logic minimize costly ECL interface. Multiple pixel ports and internal multiplexing provide TTL-compatible interface (up to 32 MHz) to the frame buffer while maintaining sophisticated color graphic data rates (up to 135 MHz). Programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port palette RAM are other key features. The TLC34058 generates red, green, and blue signals compatible with EIA RS-343-A and can drive, without external buffering, 75-Ω coaxial cables terminated at each end.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE	
			Ceramic Grid Array (GA)	Plastic Chip Carrier (FN)
0°C To 70°C	80 MHz	8 Bits	TLC34058-80GA	TLC34058-80FN
	110 MHz	8 Bits	TLC34058-110GA	TLC34058-110FN
	125 MHz	8 Bits	TLC34058-125GA	TLC34058-125FN
	135 MHz	8 Bits	TLC34058-135GA	TLC34058-135FN

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Brooktree® is a registered trademark of Brooktree Corporation.

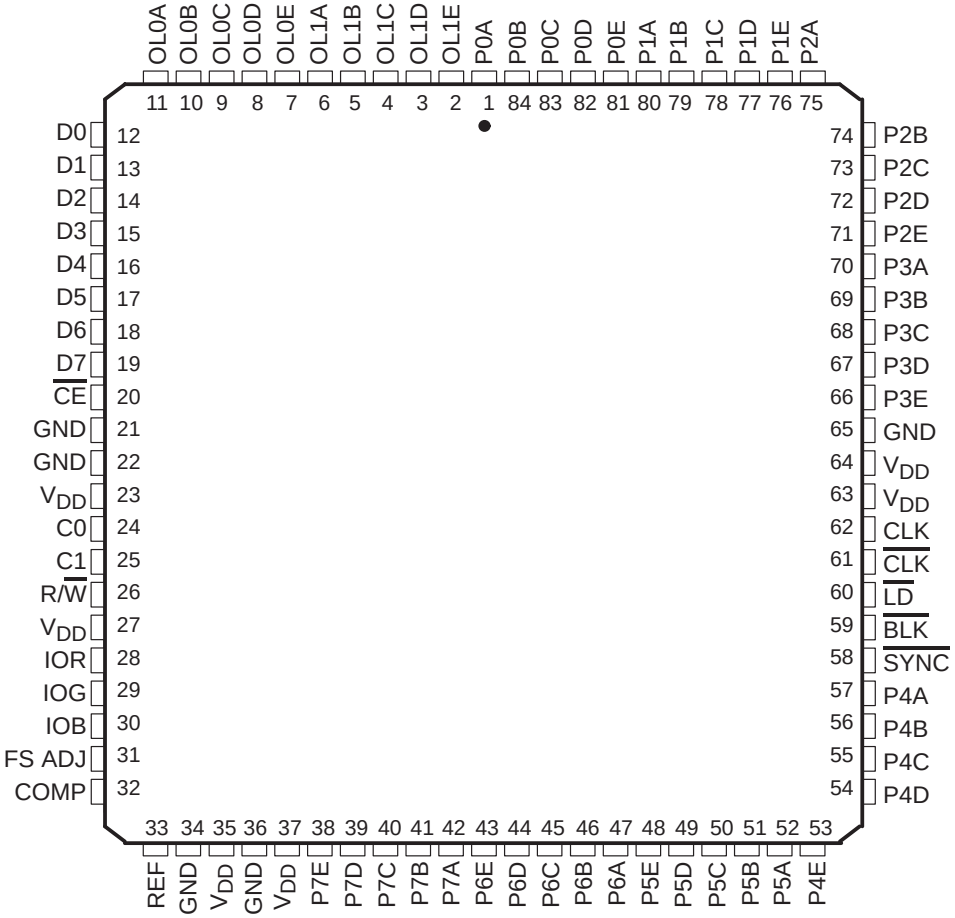
84-PIN GA PACKAGE (TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	GND	V_{DD}	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	V_{DD}	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	REF							P4D	P4B	$\overline{SYNC}$
9	V_{DD}	IOR									$\overline{BLK}$	$\overline{LD}$
8	C1	R/$\overline{W}$									$\overline{CLK}$	CLK
7	V_{DD}	C0									V_{DD}	V_{DD}
6	GND	GND									P3E	GND
5	$\overline{CE}$	D7									P3C	P3D
4	D6	D5		● (ESD SYMBOL OR ALIGNMENT DOT – ON TOP)							P3A	P3B
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B

84-PIN GA PACKAGE (BOTTOM VIEW)

	M	L	K	J	H	G	F	E	D	C	B	A
12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	V_{DD}	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	V_{DD}	GND	IOB
10	$\overline{SYNC}$	P4B	P4D							REF	FS ADJ	IOG
9	$\overline{LD}$	$\overline{BLK}$									IOR	V_{DD}
8	CLK	$\overline{CLK}$									R/$\overline{W}$	C1
7	V_{DD}	V_{DD}									C0	V_{DD}
6	GND	P3E									GND	GND
5	P3D	P3C									D7	$\overline{CE}$
4	P3B	P3A		● (ESD SYMBOL OR ALIGNMENT DOT – ON TOP)							D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A

FN PACKAGE
(TOP VIEW)



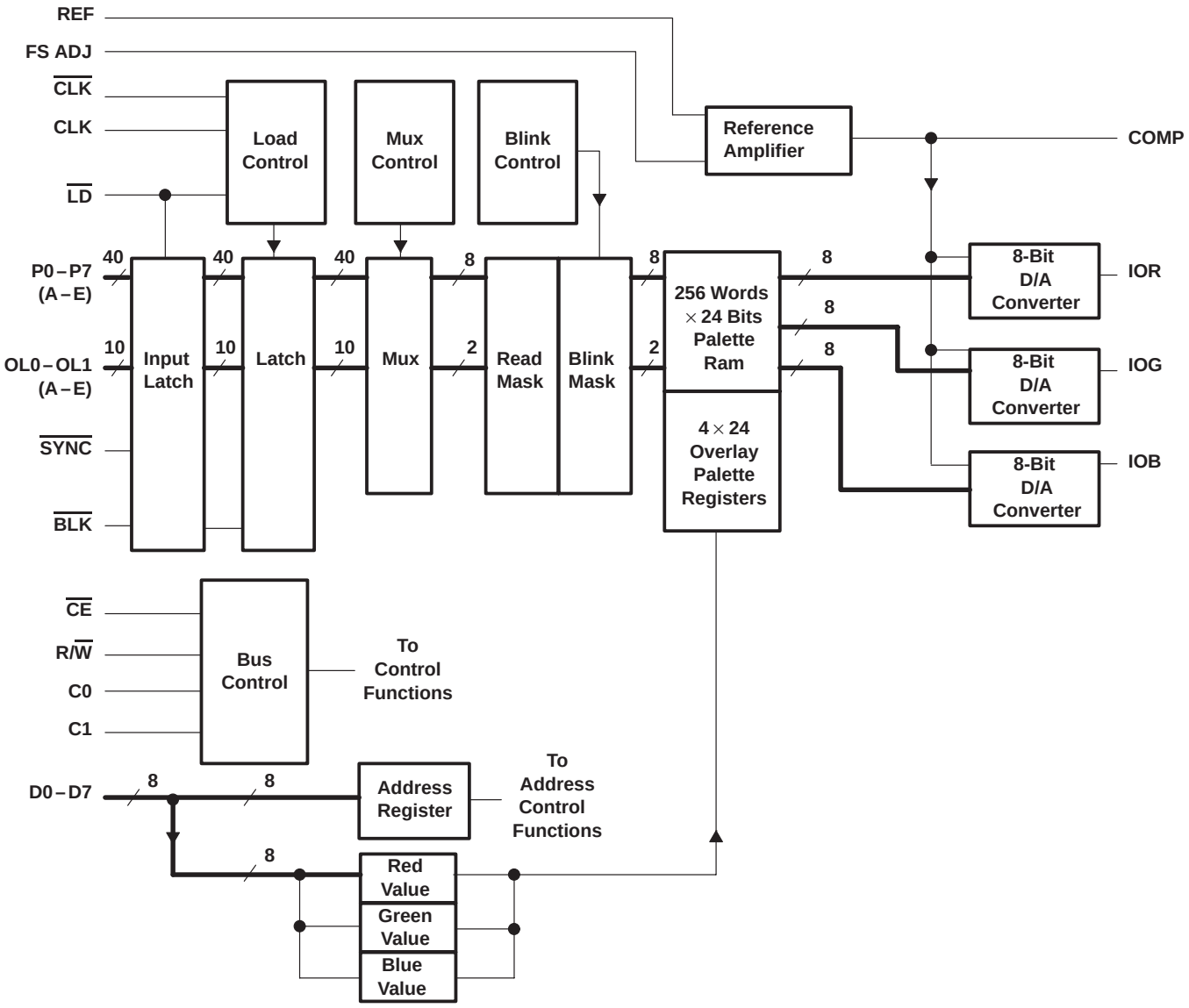
84-pin GA package pin assignments

SIGNAL	PIN NO.
$\overline{BLK}$	L9
$\overline{SYNC}$	M10
$\overline{LD}$	M9
$\overline{CLK}$	L8
CLK	M8
PORT 0	
P0A	G1
P0B	G2
P0C	H1
P0D	H2
P0E	J
PORT 1	
P1A	J2
P1B	K1
P1C	L1
P1D	K2
P1E	L2
PORT 2	
P2A	K3
P2B	M1
P2C	L3
P2D	M2
P2E	M3
PORT 3	
P3A	L4
P3B	M4
P3C	L5
P3D	M5
P3E	L6
PORT 4	
P4A	M11
P4B	L10
P4C	L11
P4D	K10
P4E	M12

SIGNAL	PIN NO.
PORT 5	
P5A	K11
P5B	L12
P5C	K12
P5D	J11
P5E	J12
PORT 6	
P6A	H11
P6B	H12
P6C	G12
P6D	G11
P6E	F12
PORT 7	
P7A	F11
P7B	E12
P7C	E11
P7D	D12
P7E	D11
OVERLAY SELECT 0	
OL0A	A1
OL0B	C2
OL0C	B1
OL0D	C1
OL0E	D2
OVERLAY SELECT 1	
OL1A	D1
OL1B	E2
OL1C	E1
OL1D	F1
OL1E	F2
DAC CURRENT OUTPUTS	
IOG	A10
IOB	A11
IOR	B9

SIGNAL	PIN NO.
POWER, REFERENCE AND MPU INTERFACE	
V_{DD}	C12
V_{DD}	C11
V_{DD}	A9
V_{DD}	L7
V_{DD}	M7
V_{DD}	A7
GND	B12
GND	B11
GND	M6
GND	B6
GND	A6
COMP	A12
FS ADJ	B10
REF	C10
$\overline{CE}$	A5
R/$\overline{W}$	B8
C1	A8
C0	B7
DATA BUS	
D0	C3
D1	B2
D2	B3
D3	A2
D4	A3
D5	B4
D6	A4
D7	B5

functional block diagram



Terminal Functions

PIN NAME	I/O	DESCRIPTION
$\overline{BLK}$	I	Composite blank control. This TTL-compatible blanking input is stored in the input latch on the rising edge of LD. When low, $\overline{BLK}$ drives the DAC outputs to the blanking level, as shown in Table 6. This causes the P0–P7 [A–E] and OL0–OL1 [A–E] inputs to be ignored. When high, $\overline{BLK}$ allows the device to perform in the standard manner.
C0, C1	I	Command control inputs. The inputs specify the type of write or read operation (see Tables 1, 2, 3, and 4). These TTL-compatible inputs are latched on the falling edge of $\overline{CE}$.
$\overline{CE}$	I	Chip enable. This TTL-compatible input control allows data to be stored and enables data to be written or read (see Figure 1). When low, $\overline{CE}$ enables data to be written or read. When high, $\overline{CE}$ allows data to be internally latched on the rising edge during write operations. Care should be taken to avoid transients on this input.
CLK	I	Clock. This input provides the pixel clock rate. CLK and $\overline{CLK}$ inputs are designed to be driven by ECL logic using a 5-V single supply.
$\overline{CLK}$	I	Clock. This input is the complement of CLK and also provides the pixel clock rate.
COMP	I	Compensation. This input is used to compensate the internal reference amplifier (see the video generation section). A 0.1-μF ceramic capacitor is connected between this pin and V_{DD} (see Figure 4). The highest possible supply voltage rejection ratio is attained by connecting the capacitor to V_{DD} rather than to GND.
D0–D7	I	Data input bus. This TTL-compatible bus transfers data into or out of the device. The data bus is an 8-bit bidirectional bus where D0 is the least significant bit.
FS ADJ	I	Full-scale adjust control. A resistor R_{set}, (see Figure 4) which is connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the proportional current and voltage relationships in Figure 3 are maintained independent of the full-scale output current. The relationships between R_{set} and the IOR, IOG, and IOB full-scale output currents are: $R_{set}(\Omega) = 11294 \times V_{ref}(V) / IOG(mA)$ $IOR, IOB (mA) = 8067 \times V_{ref}(V) / R_{set}(\Omega)$
GND		Ground. All GND pins must be connected together.
IOR, IOG IOB	O	Current outputs, red, green, and blue. High-impedance red, green, and blue video analog current outputs can directly drive a 75-Ω coaxial terminated at each end (see Figure 4).
$\overline{LD}$	I	Load control. This TTL-compatible load control input latches the P0–P7 [A–E], OL0–OL1 [A–E], $\overline{BLK}$, and $\overline{SYNC}$ inputs on its rising edge. The $\overline{LD}$ strobe occurs at 1/4 or 1/5 the clock rate and may be phase independent of the CLK and $\overline{CLK}$ inputs. The $\overline{LD}$ duty cycle limits are specified in the timing requirements table.
OL0A–OL1A OL0B–OL1B OL0C–OL1C OL0D–OL1D OL0E–OL1E	I	Overlay selection inputs. These TTL-compatible selection inputs for the Palette overlay registers are stored in the input latch on the rising edge of $\overline{LD}$. These inputs (up to 2 bits per pixel), along with bit CR6 of the command register (refer to the command register section and Table 5), specify whether the color information is selected from the palette RAM or the overlay registers. If the color information is selected from the overlay registers, the OL0–OL1 [A–E] inputs address a particular overlay register. The OL0–OL1 [A–D] or OL0–OL1 [A–E] inputs are simultaneously input to the device (see the description of bit CR7 in the command register section). The OL0–OL1 [A] inputs are processed first, then the OL0–OL1 [B] inputs, and so on. When obtaining the color information from the overlay registers, the P0–P7 [A – E] inputs are ignored. Unused inputs should be connected to GND.
P0A –P7A P0B–P7B P0C–P7C P0D–P7D P0E–P7E	I	Address inputs. These TTL-compatible address inputs for the Palette RAM are stored in the input latch on the rising edge of $\overline{LD}$. These address inputs (up to 8-bits per pixel) select one of 256 24-bit words in the palette RAM, which is subsequently input to the red, green, and blue D/A converters as three 8-bit or 4-bit bytes. Four or five addresses are simultaneously input to the P0–P7 [A–D] or P0–P7 [A–E] ports, respectively (see the description of bit CR7 in the command register section). The word addressed by P0A–P7A is first sent to the DACs, then the word addressed by P0B–P7B, and so on. Unused inputs should be connected to GND.
REF	I	Reference voltage. 1.235-V is supplied at this input. An external voltage reference circuit, shown in Figure 4, is suggested. Generating the reference voltage with a resistor network is not recommended since low-frequency power supply noisewill directly couple into the DAC output signals. This input must be decoupled by connecting a 0.1-μF ceramic capacitorbetween VREF and GND.

Terminal Functions (continued)

PIN NAME	I/O	DESCRIPTION
R/$\overline{W}$	I	Read/write input. This TTL-compatible control input is latched on the falling edge of $\overline{CE}$ (see Figure 1). When low, writes data to the device. Data is internally latched on the rising edge of $\overline{CE}$. When high, reads data from the device.
$\overline{SYNC}$	I	Composite sync control. This TTL-compatible sync control input is stored in the input latch on the rising edge of LD. When low, $\overline{SYNC}$ turns off a 40 IRE current source on the IOG output, as shown in Figure 3. This input does not override any control data input, as shown in Table 6. It should be brought low during the blanking interval only, as shown in Figure 3. When high, $\overline{SYNC}$ allows the device to perform in the standard manner.
V_{DD}		Supply voltage. All V_{DD} pins must be connected together.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage V_{DD} (see Note 1) . . . . . 7 V
Voltage range on any digital input (see Note 1) . . . . . –5 V to V_{DD} + 0.5 V
Analog output short circuit duration to any power supply or common, I_{OS} . . . . . unlimited
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: GA package . . . . . 260°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
High-level Input voltage, V_{IH}	CLK, $\overline{CLK}$	$V_{DD}-1$		$V_{DD}+0.5$	V
	Other inputs	2		$V_{DD}+0.5$	V
Low-level Input voltage, V_{IL}	CLK, $\overline{CLK}$	–0.5		$V_{DD}-1.6$	V
	Other inputs	–0.5		0.8	V
Reference voltage, V_{ref}		1.2	1.235	1.26	V
Output load resistance, R_L			37.5		Ω
FS ADJ resistor, R_{set}			523		Ω
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{ref}	Input reference current					10		µA
k_{SVR}	Supply voltage rejection ratio		f = 1 kHZ, C8 = 0.1 µF (see Figure 4)			0.5		$\frac{\%}{\%\Delta V_{DD}}$
I_{DD}	Supply current	80 MHz	V_{DD} = 5 V,	T_A = 20°C		175		mA
			V_{DD} = 5.25 V,	T_A = 0°C			400	
		110 MHz	V_{DD} = 5 V,	T_A = 20°C		195		
			V_{DD} = 5.25 V,	T_A = 0°C			420	
		125 MHz	V_{DD} = 5 V,	T_A = 20°C		205		
			V_{DD} = 5.25 V,	T_A = 0°C			435	
		135 MHz	V_{DD} = 5 V,	T_A = 20°C		200		
			V_{DD} = 5.25 V,	T_A = 0°C			435	
I_{IH}	High-level input current	CLK, $\overline{CLK}$	V_I = 4 V				1	µA
		Other inputs	V_I = 2.4 V				1	µA
I_{IL}	Low-level input current	CLK, $\overline{CLK}$	V_I = 0.4 V				–1	µA
		Other inputs	V_I = 0.4 V				–1	µA
C_i	Input capacitance, digital		f = 1 MHz,	V_I = 2.4 V		4	10	pF
$C_{i(CLK)}$	Input capacitance, CLK, $\overline{CLK}$		f = 1 MHz,	V_I = 4 V		4	10	pF
V_{OH}	High-level output voltage, D0–D7		I_{OH} = –800 µA		2.4			V
V_{OL}	Low-level output voltage, D0–D7		I_{OL} = 6.4 mA				0.4	V
I_{OZ}	High-impedance-state output current						10	µA
z_o	Output impedance					50		kΩ
C_o	Output capacitance (f = 1 MHz, I_O = 0)					13	20	pF

† All typical values are at T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (see Note 2)

PARAMETER	TIMING† REFERENCE	LIMIT	VERSION				UNITS
			135 MHz	125 MHz	110 MHz	80 MHz	
Clock frequency	–	MAX	135	125	110	80	MHz
$\overline{LD}$ frequency	–	MAX	33.75	31.25	27.5	20	MHz
Setup time, R/$\overline{W}$, C0, C1 high before $\overline{CE}$ ↓	1	MIN	0	0	0	0	ns
Hold time, R/$\overline{W}$, C0, C1 high after $\overline{CE}$ ↓	2	MIN	15	15	15	15	ns
Pulse duration, $\overline{CE}$ low	3	MIN	50	50	50	50	ns
Pulse duration, $\overline{CE}$ high	4	MIN	25	25	25	25	ns
Setup time, write data before $\overline{CE}$ ↑	8	MIN	35	35	35	50	ns
Hold time, write data after $\overline{CE}$ ↓	9	MIN	0	0	0	0	ns
Pixel and control setup time	10	MIN	3	3	3	4	ns
Pixel and control hold time	11	MIN	2	2	2	2	ns
Clock cycle time	12	MIN	7.4	8	9.09	12.5	ns
Pulse duration, CLK high	13	MIN	3	3.2	4	5	ns
Pulse duration, CLK low	14	MIN	3	3.2	4	5	ns
$\overline{LD}$ cycle time	15	MIN	29.6	32	36.36	50	ns
$\overline{LD}$ pulse duration high time	16	MIN	12	13	15	20	ns
$\overline{LD}$ pulse duration low time	17	MIN	12	13	15	20	ns

† See Figures 1 and 2.

NOTE 2. TTL input signals are 0 to 3 V with less than 3 ns rise/fall times between 10% and 90% levels. ECL input signals are V_{DD} – 1.8 V to V_{DD} – 0.8 V with less than 2 ns rise/fall times between 20% and 80% levels. For input and output signals, timing reference points are at the 50% signal level. Analog output loads are less than 10 pF. D0 – D7 output loads are less than 40 pF.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (unless otherwise noted)

analog outputs

PARAMETER			MIN	TYP†	MAX	UNIT
E_L	Integral linearity error (each DAC)				±1	LSB
E_D	Differential linearity error				±1	LSB
	Gray scale error				±5	
I_O	Output current	White level relative to blank	17.69	19.05	20.4	mA
		White level relative to black	16.74	17.62	18.5	mA
		Black level relative to blank	0.95	1.44	1.9	mA
		Blank level on IOR, IOB	0	5	50	µA
		Blank level on IOG	6.29	7.6	8.96	mA
		Sync level on IOG	0	5	50	µA
	LSB size			69.1		µA
	DAC to DAC matching			2%	5%	
	Output compliance voltage		–1		1.2	V

† All typical values are at T_A = 25°C

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, R_{set} = 523 Ω, V_{ref} = 1.235 V (see Note 2)

PARAMETER	TIMING† REFERENCE	LIMIT	VERSION				UNITS
			135 MHz	125 MHz	110 MHz	80 MHz	
$\overline{CE}$ low to data bus enabled	5	MIN	10	10	10	10	ns
$\overline{CE}$ low to data valid	6	MAX	75	75	75	100	ns
$\overline{CE}$ high to data bus disabled	7	MAX	15	15	15	15	ns
Analog output delay time (see Note 3)	18	TYP	20	20	20	20	ns
Analog output rise or fall time (see Note 4)	19	TYP	2	2	2	3	ns
Analog output setting time (see Note 5)	20	MAX	8	8	9	12	ns
Glitch impulse (see Note 6)		TYP	50	50	50	50	pV-s
Analog output skew		TYP	0	0	0	0	ns
		MAX	2	2	2	2	ns
Pipeline delay		MIN	6	6	6	6	clock
		MAX	10	10	10	10	cycles

† See Figures 1 and 2.

NOTES: 2. TTL input signals are 0 to 3 V with less than 3 ns rise/fall times between 10% and 90% levels. ECL input signals are V_{DD} – 1.8 to V_{DD} – 0.8 V with less than 2 ns rise/fall times between 20% and 80% levels. For input and output signals, timing reference points are at the 50% signal level. Analog output loads are less than 10 pF. D0 – D7 output loads are less than 40 pF.

3. Measured from 50% point of rising clock edge to 50% point of full-scale transition.
4. Measured between 10% and 90% of full-scale transition.
5. Measured from 50% point of full-scale transition to output settling within ± 1 LSB. Settling time does not include clock and data feedthrough.
6. Glitch impulse includes clock and data feedthrough. The –3-dB test bandwidth is twice the clock rate.

PARAMETER MEASUREMENT INFORMATION

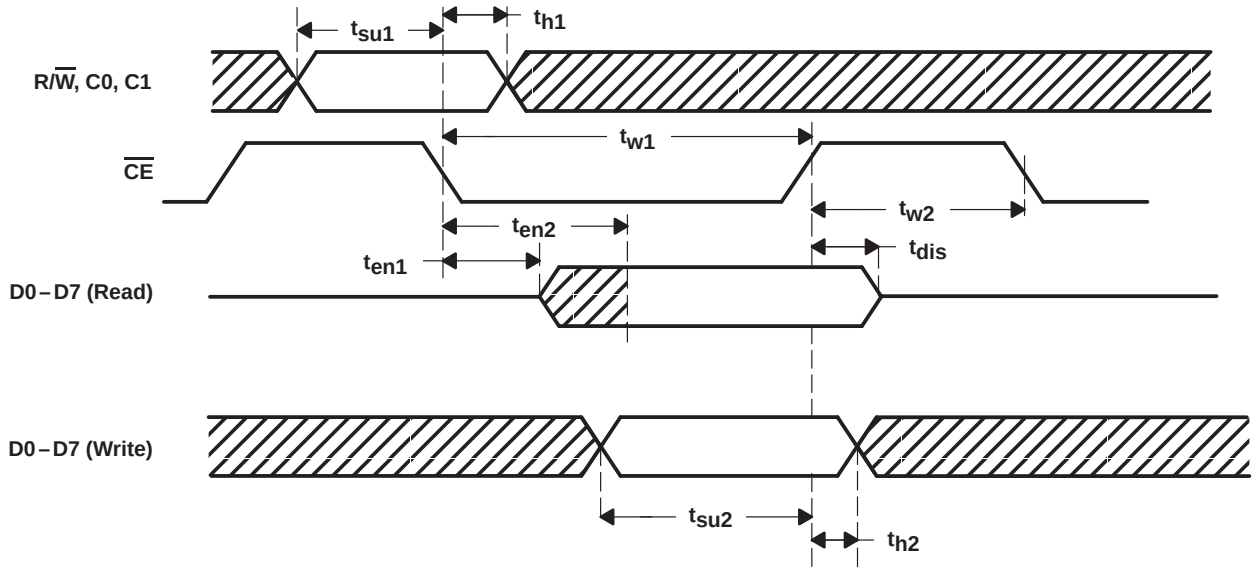


Figure 1. Read/Write Timing Waveform

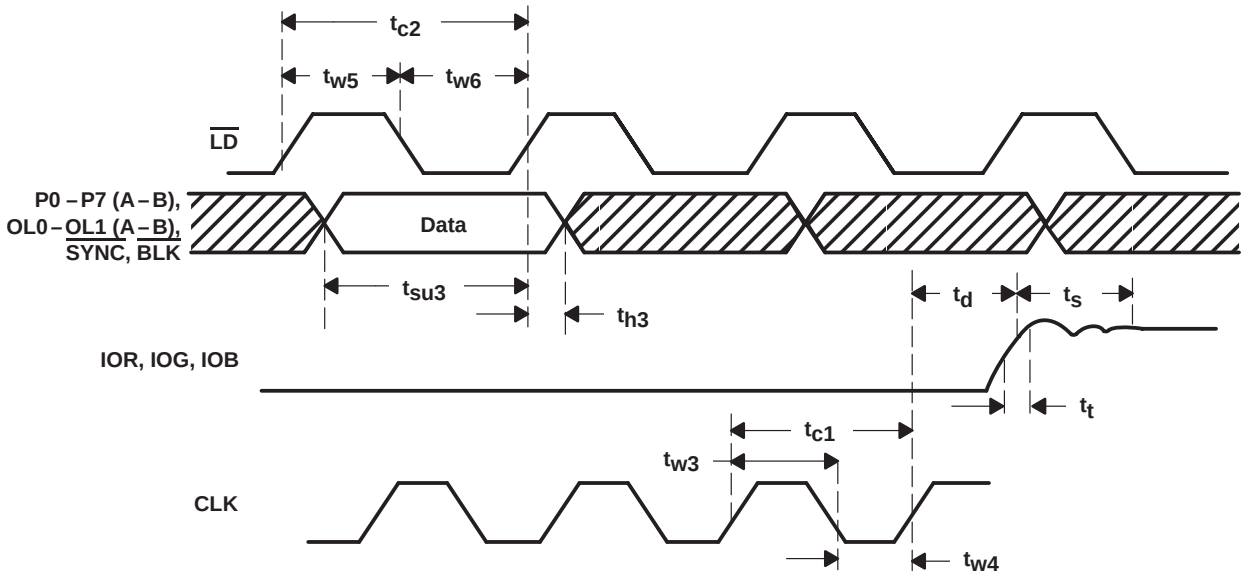
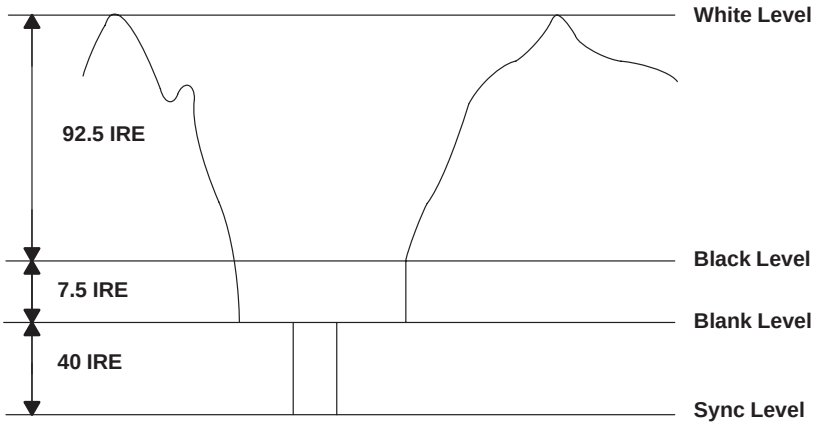


Figure 2. Video Input/Output Timing Waveform

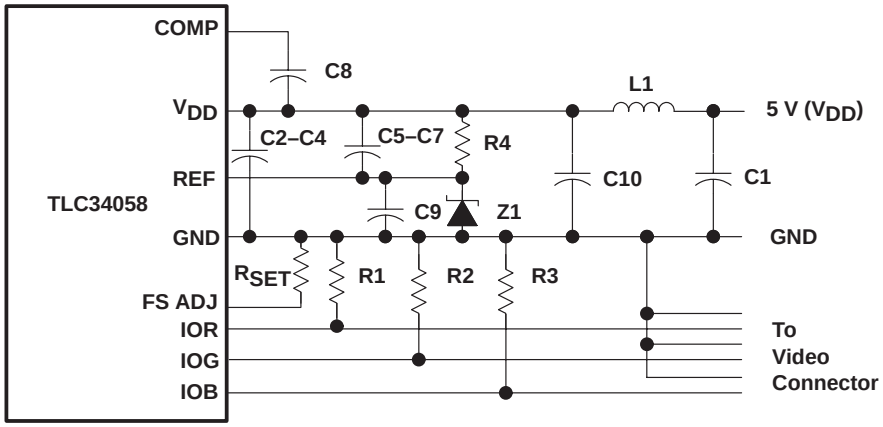
PARAMETER MEASUREMENT INFORMATION

RED, BLUE		GREEN	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.00



NOTE A: The IRE (Institute of Radio Engineers – now IEEE) scale is used for defining the relative voltage levels of the sync, white, black, and blank levels in a monitor circuit. The reference white level is set at 100 IRE units. The blanking level is set at ϕ IRE units. One IRE unit is equivalent to 1/100 of the difference between the reference white level and the blanking level.

Figure 3. Composite Video Output Waveforms



LOCATION	DESCRIPTION	VENDOR PART NUMBER
C1–C4, C8, C9	0.1-μF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01-μF ceramic chip capacitor	AVX 12102T903QA1018
C10	33-μF tantalum capacitor	Mallory CSR13-K336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75-Ω 1% metal film resistor	Dale CMF-55C
R4	1000-Ω 1% metal film resistor	Dale CMF-55C
R_{set}	523-Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2-V diode	National Semiconductor LM385Z-1.2

NOTE A: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics does not degrade the performance of the TLC34058.

Figure 4. Circuit Diagram

PARAMETER MEASUREMENT INFORMATION

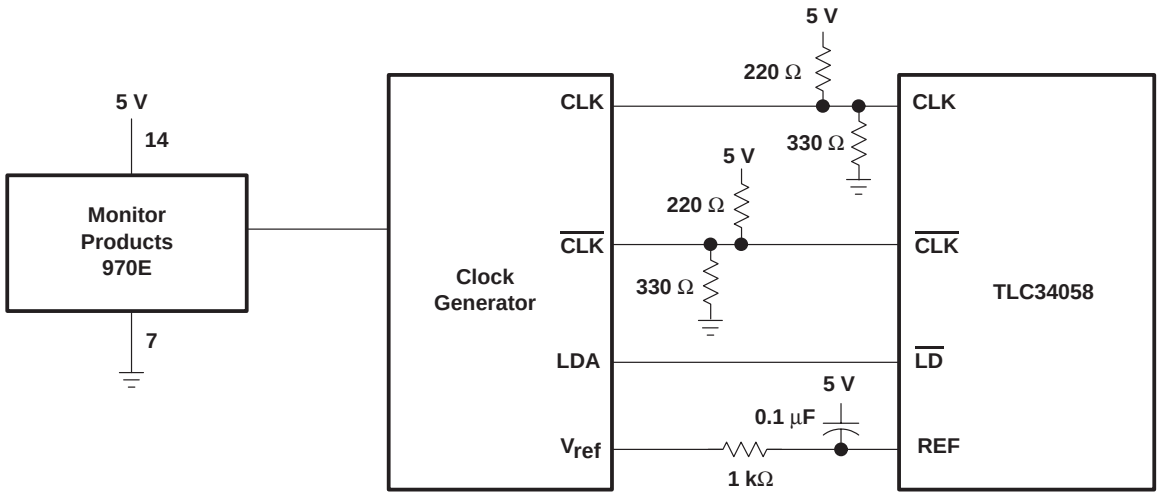


Figure 5. Generating the Clock, Load, and Voltage Reference Signals

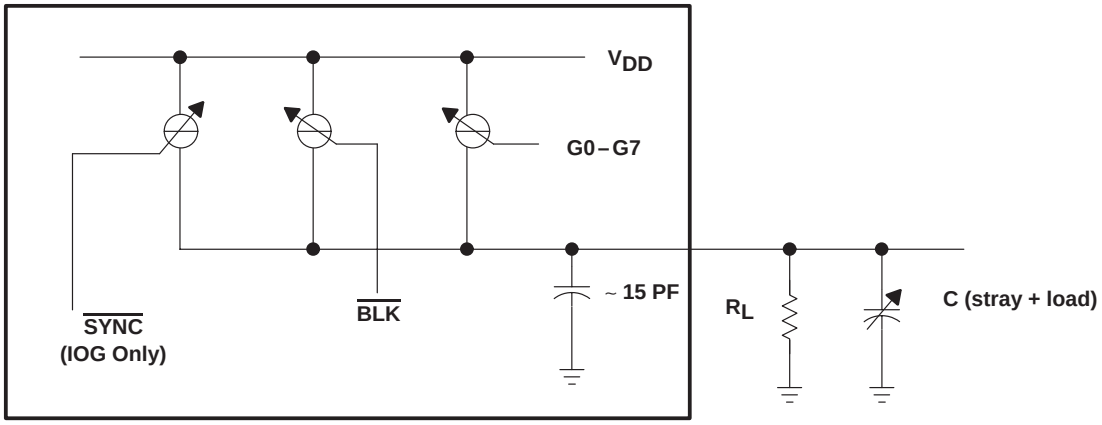


Figure 6. Equivalent Circuit of the Current Output (IOG)

PRINCIPLES OF OPERATION

microprocessor unit (MPU) interface

As shown in the functional block diagram, the MPU has direct access to the internal control registers and color overlay palettes via a standard MPU interface. Since the palette RAM and overlay registers have dual ports, they can be updated without affecting the display refresh process. One port is allocated for updating or reading data and the other for display.

palette RAM write or read

The palette RAM location is addressed by the internal 8-bit address register (ADDR0–7). The MPU can either write to or read from this register. The register eliminates the need for external address multiplexers. ADDR0–ADDR7 are updated via D0–D7. To address the red, green, and blue part of a particular RAM location, the internal address register is provided with two additional bits, ADDRa and ADDRb. These address bits count modulo 3 and are reset to 0 when the MPU accesses the internal address register.

After writing to or reading from the internal address register, the MPU executes three write or read cycles (red, green and blue). The register ADDRab is incremented after each of these cycles so that the red, green, and blue information is addressed from the correct part of the particular RAM location. During the blue write cycle, the red, green, and blue color information is adjoined to form a 24-bit word, which is then written to the particular RAM location. After the blue write/read cycle, the internal address register bits ADDR0–7 are incremented to access the next RAM location. For an entire palette RAM write or read, the bits ADDR0–7 are reset to 00 after accessing the FF (256) palette RAM location.

Two additional control bits, C0 and C1, are used to differentiate the palette RAM read/write function from other operations that utilize the internal address register. C0 and C1 are respectively set high and low for writing to or reading from the palette RAM. Table 1 summarizes this differentiation, along with other internal address register operations. Note that C0 and C1 are each set low for writing to or reading from the internal address register.

PRINCIPLES OF OPERATION

Table 1. Writing to or Reading from Palette RAM

R/$\overline{W}$	C1	C0	ADDRb	ADDRa	FUNCTION
L	L	L	X	X	write ADDR0–7: D0–D7 → ADDR0–7; 0 → ADDRa,b
L	L	H	L	L	write red color: D0–D7 → RREG; increment ADDRa,b
L	L	H	L	H	write green color: D0–D7 → GREG; increment ADDRa,b
L	L	H	H	L	write blue color: D0–D7 → BREG; increment ADDRa,b; increment ADDR0–7; write palette RAM
H	L	L	X	X	read ADDR0–7: ADDR0–7 → D0–D7; 0 → ADDRa,b
H	L	H	L	L	read red color: R0–R7 → D0–D7; increment ADDRa,b
H	L	H	L	H	read green color: G0–G7 → D0–D7; increment ADDRa,b
H	L	H	H	L	read blue color: B0–B7 → D0–D7; increment ADDRa,b; increment ADDR0–7

X = irrelevant

overlay register write/read

With a few exceptions, the overlay register operation is identical to the palette RAM write/read operation (refer to the palette RAM write/read section). Upon writing to or reading from the internal address register, the additional address register ADDRab is automatically reset to 0. ADDRab counts modulo 3 as the red, green, and blue information is written to or read from a particular overlay register. The four overlay registers are addressed with internal address register values 00–03. After writing/reading blue information, the internal address register bits ADDR0–7 are incremented to the next overlay location. After accessing overlay register value 03, the internal address register does not reset to 00 but is advanced to 04.

For writing to or reading from the internal address register, C0 and C1 are set low. When accessing the overlay registers, C0 and C1 are set high. Refer to Table 2 for quick reference.

Table 2. Writing to or Reading from Overlay Registers

R/$\overline{W}$	C1	C0	ADDRb	ADDRa	FUNCTION
L	L	L	X	X	write ADDR0-7: D0–D7 → ADDR0–7; 0 → ADDRa,b
L	H	H	L	L	write red color: D0–D7 → RREG; increment ADDRa,b
L	H	H	L	H	write green color: D0–D7 → GREG; increment ADDRa,b
L	H	H	H	L	write blue color: D0–D7 → BREG; increment ADDRa,b; increment ADDR0–7; write overlay register
H	L	L	X	X	read ADDR0–7: ADDR0–7 → D0–D7; 0 → ADDRa,b
H	H	H	L	L	read red color: R0–R7 → D0–D7; increment ADDRa,b
H	H	H	L	H	read green color: G0–G7 → D0–D7; increment ADDRa,b
H	H	H	H	L	read blue color: B0–B7 → D0–D7; increment ADDRa,b; increment ADDR0–7

X = irrelevant

PRINCIPLES OF OPERATION

control register write/read

The four control registers are addressed with internal address register values 04–07. Upon writing to or reading from the internal address register, the additional address bits ADDRab are automatically reset to 0. To facilitate read-modify-write operations, the internal address register does not increment after writing to or reading from the control registers. All control registers may be accessed at any time. When accessing the control registers, C0 and C1 are respective set low and high. Refer to Table 3 for quick reference.

Table 3. Writing to or Reading from Control Registers

$\overline{R/W}$	C1	C0	ADDRba	ADDRab	FUNCTION
L	L	L	X	X	write ADDR0–7: D0–D7 → ADDR0–7; 0 → ADDRa,b
L	H	L	L	L	write control register: D0–D7 → control register
H	L	L	X	X	read ADDR0–7: ADDR0–7 → D0–D7; 0 → ADDRa,b
H	H	L	L	L	read control register: control register → D0–D7

X = irrelevant

summary of internal address register operations

Table 4 provides a summary of operations that use the internal address register. Figure 1 presents the read/write timing for the device.

If an invalid address is loaded into the internal address register, the device will ignore subsequent data from the MPU during a write operation and will send incorrect data to the MPU during a read operation.

Table 4. Internal Address Register Operations

INTERNAL ADDRESS REGISTER VALUE (ADDR0–7) (HEX)	C1	C0	MPU ACCESS	ADDRab (counts modulo 3)	COLOR
00–FF	L	H	color palette RAM	00 01 11	red value green value blue value
00–03	H	H	over color 0 to 3	00 01 110	red value green value blue value
04	H	L	read mask register		
05	H	L	blink mask register		
06	H	L	command register		
07	H	L	test register		

interruption of display refresh pixel data (via simultaneous pixel data retrieval and MPU write)

If the MPU is writing to a particular palette RAM location or overlay register (during the blue cycle) and the display refresh process is accessing pixel data from the same RAM location or overlay register, one or more pixels on the display screen may be disturbed. If the MPU write data is valid during the complete chip enable period, a maximum of one pixel will be disturbed.

PRINCIPLES OF OPERATION

frame buffer interface and timing

An internal latch and multiplexer enables the frame buffer to send the pixel data to the device at TTL rates. On the rising edges of $\overline{LD}$, information for four or five consecutive pixels is latched into the device. This information includes the palette RAM address (up to 8 bits), the overlay register address (up to 2 bits), and the sync and blank information for each of the four or five consecutive pixels. The timing diagram for this pixel data input transfer is shown in Figure 2, along with the video output waveforms (IOR, IOG, and IOB). Note that with this architecture, the sync and blank timing can only be recognized with four- or five-pixel resolution.

The display refresh process follows the first-in first-out format. Color data is output from the device in the same order in which palette RAM and overlay addresses are input. This process continues until all four or five pixels have been output, at which point the cycle will repeat.

The overlay timing can be controlled by the pixel timing. However, this approach requires that the frame buffer emit additional bit planes to control the overlay selection on a pixel basis. Alternatively, the overlay timing can be controlled by external character or cursor generation timing (see the color selection section).

No phase relationship between the $\overline{LD}$ and CLK signals is required (see Figure 2). Therefore, the $\overline{LD}$ signal can be derived by externally dividing the CLK signal by four or five. Any propagation delay in $\overline{LD}$ caused by the divider circuitry will not render the device nonfunctional. Regardless of the phase relationship between $\overline{LD}$ and CLK, the pixel, overlay, sync, and blank data are latched on the rising edge of $\overline{LD}$.

The device has an internal load signal (not brought out to a pin), which is synchronous to CLK and will follow $\overline{LD}$ by at least one and not more than four clock cycles. This internal load signal transfers the $\overline{LD}$-latched data into a second set of latches, which are then internally multiplexed at the pixel clock or CLK signal frequency.

For 4:1 or 5:1 multiplexing, a rising edge of $\overline{LD}$ should occur every four or five clock cycles. Otherwise, the internal load signal generation circuitry cannot lock onto or synchronize with $\overline{LD}$.

color selection

The read mask, blink mask, and command registers process eight bits of color information (P0–P7) and two bits of overlay information (OL0–OL1) for each pixel every clock cycle. Control registers allow individual bit planes to be enabled/disabled for display and/or blinked at one of four blink rates and duty cycles (see the command register section, bits CR4–CR5).

By monitoring the $\overline{BLK}$ input to determine vertical retrace intervals, the device ensures that a color change due to blinking occurs only during the nonactive display time. Thus, a color change does not occur in the middle of the screen. A vertical retrace is sensed when $\overline{BLK}$ is low for at least 256 $\overline{LD}$ cycles. The color information is then selected from the palette RAM or overlay registers, in accordance with the processed input pixel data. Table 5 presents the effect of the processed input pixel data upon color selection. Note that P0 is the least significant bit (LSB) of the color palette RAM. When CR6 is high and both OL1 and OL0 are low, color information resides in the color palette RAM. When CR6 is low or either of the overlay inputs is high, the overlay registers provide the DAC inputs.

PRINCIPLES OF OPERATION

Table 5. Input Pixel Data versus Color Selection

COMMAND REGISTER BIT	OVERLAY SELECT INPUT		COLOR ADDRESS (HEX)	COLOR INFORMATION
CR6	OL1	OL0	P7 – P0	
H	L	L	00	color palette entry 00
H	L	L	01	color palette entry 01
•	•	•	•	• • • •
•	•	•	•	• • • •
•	•	•	•	• • • •
H	L	L	FF	color palette entry FF
L	L	L	XX	overlay register 0
X	L	H	XX	overlay register 1
X	H	L	XX	overlay register 2
X	H	H	XX	overlay register 3

X = irrelevant

video generation

The TLC34058 presents 8 bits of red, green, and blue information from either the palette RAM or overlay registers to the three 8-bit DACs during every clock cycle. The DAC outputs produce currents that correlate to their respective color input data. These output currents are translated to voltage levels that drive the color CRT monitor. The $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ signals adjust the DAC analog output currents to generate specific output levels that are required in video applications. Table 6 shows the effect of $\overline{\text{SYNC}}$ and $\overline{\text{BLK}}$ upon the DAC output currents. Figure 3 presents the overall composite video output waveforms. Note that only the green output (IOG) contains sync information.

The DAC architecture ensures monotonicity and reduced switching transients by using identical current sources and routing their outputs to the DAC current output or GND. Utilizing identical current sources eliminates the need for precision component ratios within the DAC ladder circuitry. An on-chip operational amplifier stabilizes the DAC full-scale output current over temperature and power supply variations.

Table 6. Effects of Sync and Blank Upon DAC Output Currents (see Note 7)

DESCRIPTION	IOG (mA)	IOR, IOB (mA)	SYNC	BLK	DAC INPUTS
WHITE	26.67	19.05	H	H	FF
DATA	data + 9.05	data + 1.44	H	H	data
DATA w/o $\overline{\text{SYNC}}$	data + 1.44	data + 1.44	L	H	data
BLACK	9.05	1.44	H	H	00
BLACK w/o $\overline{\text{SYNC}}$	1.44	1.44	L	H	00
BLACK	7.62	0	H	L	xx
$\overline{\text{SYNC}}$	0	0	L	L	xx

NOTE 7: The data in this table was measured with full-scale IOG current = 26.67 mA, R_{set} = 523 Ω, V_{ref} = 1.235 V.

command register

The MPU can write to or read from the command register at any time. The command register is not initialized. CR0 corresponds to the D0 data bus line. Refer to Table 7 for quick reference.

PRINCIPLES OF OPERATION

Table 7. Command Register

COMMAND REGISTER BIT	COMMAND REGISTER BIT FUNCTION	COMMAND REGISTER BIT DESCRIPTION
CR7	Multiplex Select Bit low: selects 4:1 multiplexing high: selects 5:1 multiplexing	This bit selects either 4:1 or 5:1 multiplexing for the palette RAM and overlay register address, $\overline{\text{SYNC}}$, and $\overline{\text{BLK}}$ inputs. If 4:1 multiplexing is selected, the device ignores the 'E' palette RAM and overlay register address inputs. These inputs should be connected to GND, and the $\overline{\text{LD}}$ signal frequency should be 1/4 of the clock frequency. If 5:1 is specified, all of the palette RAM and overlay register address inputs are used and the $\overline{\text{LD}}$ signal should be 1/5 of the clock frequency.
CR6	RAM Enable Bit low: use overlay register 0 high: use palette RAM	When the overlay select bits, OL0 and OL1, are both low, this bit causes the DACs color information to be selected from overlay register 0 or the palette RAM.
CR5, CR4	Blink Rate Select Bits 00: 16 on, 48 off (25/75) 01: 16 on, 16 off (50/50) 10: 32 on, 32 off (50/50) 11: 64 on, 64 off (50/50)	These two bits select the blink rate cycle time and duty cycle. The on and off numbers specify the blink rate cycle time as the number of vertical periods. The numbers in parentheses specify the duty cycle in (on/off) percent.
CR3	OL1 Blink Enable Bit low: disable blinking high: enable blinking	If this bit is a high, the OL1 [A–E] inputs will toggle between a logic 0 and their input value at the selected blink rate before latching the incoming pixel data. Simultaneously, command register CR1 must be set high. If the CR2 bit is low, the OL0 [A–E] inputs will be unaffected.
CR2	OL0 Blink Enable Bit low: disable blinking high: enable blinking	If this bit is high, the OL0 [A–E] inputs will toggle between a logic 0 and their input value at the selected blink rate before latching the incoming pixel data. Simultaneously, command register CR0 must be set high. If the CR2 bit is low, the OL0 [A–E] inputs will be unaffected.
CR1	OL1 Display Enable Bit low: disable high: enable	If this bit is low, the OL1 [A–E] inputs are forced to a logic 0 before latching the incoming pixel data. If the CR1 bit is high, the OL1 [A–E] inputs will be affected.
CR0	OL0 Display Enable Bit low: disable high: enable	If this bit is low, the OL0 [A–E] inputs are forced to a logic 0 before latching the incoming pixel data. If the CR0 bit is high, the OL0 [A–E] inputs will be affected.

read mask register

The read mask register is used to enable (high) or disable (low) the eight bit planes (P0–P7) within the palette RAM addresses. The enabling or disabling is accomplished by logic ANDing the read mask register with the palette RAM address before addressing the palette RAM. Note that read mask register bit 0 corresponds to data bus line D0. The MPU can write to or read from this register at any time. This register is not initialized.

blink mask register

The blink mask register is used to enable (high) or disable (low) the blinking of bit planes within the palette RAM addresses. For example, if blink mask register bit n is set high, the true Pn value will address the palette RAM during the on portion of the blink cycle. During the off part of the blink cycle, the Pn value will be replaced with a 0 before the palette RAM is addressed. The blink rate cycle time and duty cycle is specified by command register bits CR4 and CR5. If blink mask register bit n is set low, the true Pn value will always address the palette RAM. Note that blink mask register bit 0 corresponds to data bus line D0. This register is not initialized.

PRINCIPLES OF OPERATION

test register

The test register allows the MPU to read the inputs to the DAC for diagnostic purposes. The MPU can write to or read from this register at any time. This register is not initialized. Only the four least significant bits can be written to, while all 8 bits can be read. Note that test register bit 0 corresponds to data bus line D0.

A function description of this register is presented in Table 8.

Table 8. Functional Description of Test Register

TR3–TR0	D4–D7	FUNCTION
0100	4 MSBs of blue data input	MPU read or write D0–D3
0010	4 MSBs of green data input	
0001	4 MSBs of red data input	
1100	4 LSBs of blue data input	MPU read D0–D7
1010	4 LSBs of green data input	
1001	4 LSBs of red data input	

To read the DAC inputs, the MPU must first load the test register's four least significant bits. One of the test register bits, b0 (red DAC), b1 (green DAC) or b2 (blue DAC), must be set high and the other two bits low. This process determines whether the inputs to the red, green, or blue DAC will be read. The test register bit b3 must be set high for reading the four most significant DAC inputs or low for reading the four least significant inputs. The MPU then reads the test register while the test register's four least significant bits contain the previously written information. Note that either the device clock must be slowed down to the MPU cycle time or the same pixel and overlay data must be continuously presented to the device during the entire MPU read cycle.

APPLICATION INFORMATION

device ground plane

Use of a four-layer PC board is recommended. All of the ground pins, voltage reference circuitry, power supply bypass circuitry, analog output signals, and digital signals, as well as any output amplifiers, should have a common ground plane.

device analog power plane (APP)

The device plus associated analog circuitry should have a separate analog power plane (APP) for V_{DD}. The APP powers the device, voltage reference circuitry, and any output amplifiers. It should be connected to the overall PCB power plane (V_{DD}) at a single point through a ferrite bead, which should be within 3 inches of the device. This connection is shown in Figure 4.

PCB power plane and PCB ground plane

The PCB power plane powers the digital circuitry. The PCB power plane and PCB ground planes should not overlay the APP unless the plane-to-plane noise is common-mode.

supply decoupling

Bypass capacitors should have the shortest possible lead lengths to reduce lead inductance. For best results, a parallel combination of 0.1-μF ceramic and 0.01-μF chip capacitors should be connected from each V_{DD} pin to GND. If chip capacitors are not feasible, radial-lead ceramic capacitors may be substituted. These capacitors should be located as close to the device as possible.

The performance of the internal power supply noise rejection circuitry decreases with noise frequency. If a switching power supply is used for V_{DD}, close attention must be paid to reducing power supply noise. To reduce such noise, the APP could be powered with a three-terminal voltage regulator.

digital interconnect

The digital inputs should be isolated from the analog outputs and other analog circuitry as much as possible. Shielding the digital inputs will reduce noise on the power and ground lines. The lengths of clock and data lines should be minimized to prevent high-frequency clock and data information from inducing noise into the analog part of the video system. Active termination resistors for the digital inputs should be connected to the PCB power plane, not the APP. These digital inputs should not overlay the device ground plane.

analog signal interconnect

Minimizing the lead lengths between groups of V_{DD} and GND minimizes inductive ringing. To minimize noise pickup due to reflections and impedance mismatch, the device should be located as close to the output connectors as possible. The external voltage reference should also be as close to the device as possible, to minimize noise pickup.

To maximize high-frequency supply voltage rejection, the video output signals should overlay the device ground plane and not the APP.

Each analog output should have a 75-Ω load resistor connected to GND for maximum performance. To minimize reflections, the resistor connections between current output and ground should be as close to the device as possible.

APPLICATION INFORMATION

clock interfacing

To facilitate the generation of high-frequency clock signals, the CLK and $\overline{\text{CLK}}$ pins are designed to accept differential signals that can be generated with 5-V (single supply) ECL logic. Due to noise margins of the CMOS process, the CLK and $\overline{\text{CLK}}$ inputs must be differential signals. Connecting a single-ended clock signal to CLK and connecting $\overline{\text{CLK}}$ to GND will not work.

The CLK and $\overline{\text{CLK}}$ pins require termination resistors (220-Ω to V_{DD} and 330-Ω to GND) that should be as close to the device as possible.

$\overline{\text{LD}}$ is typically generated by dividing the clock frequency by four (4:1 multiplexing) or five (5:1 multiplexing) and translating the resulting signal to TTL levels. Since no phase relationship between the $\overline{\text{LD}}$ and CLK signals is required, any propagation delay in $\overline{\text{LD}}$ caused by the divider circuitry will not affect device performance.

The pixel, overlay, sync and blank data are latched on the rising edge of $\overline{\text{LD}}$. $\overline{\text{LD}}$ may also be used as the shift clock for the video DRAMs. In short, $\overline{\text{LD}}$ provides the fundamental timing for the video system.

The Bt438 Clock Generator (from Brooktree) is recommended for generating the CLK, $\overline{\text{CLK}}$, $\overline{\text{LD}}$, and REF signals. It supports both 4:1 and 5:1 multiplexing. Alternatively, the Bt438 can interface the device to a TTL clock. Figure 5 illustrates the interconnection between the Bt438 and the device.

PACKAGING INFORMATION

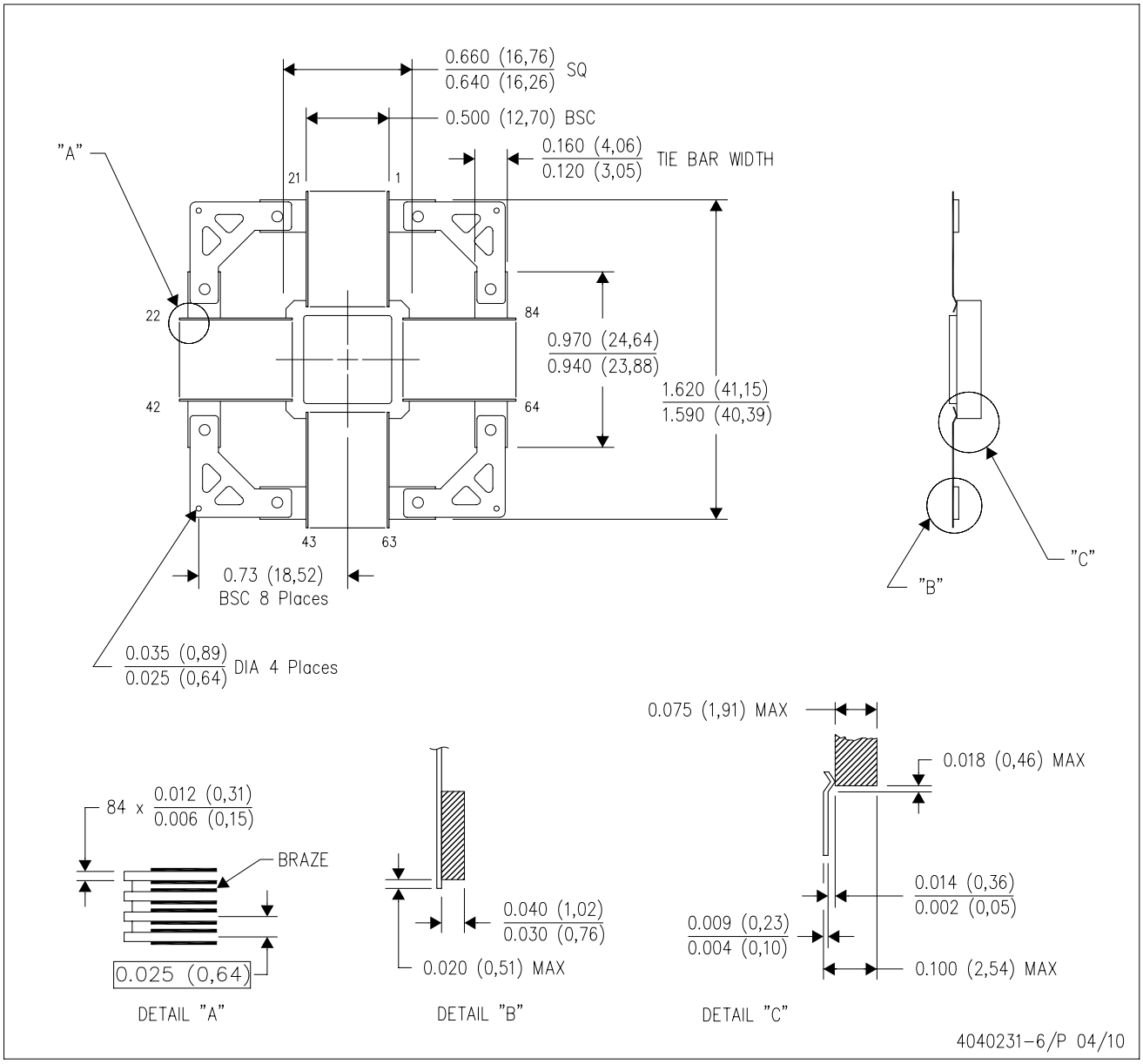
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8992801XA	OBSOLETE	CPGA	GA	84		TBD	Call TI	Call TI
5962-8992801XC	OBSOLETE	CPGA	GA	84		TBD	Call TI	Call TI
TLC34058-110FN	OBSOLETE	PLCC	FN	84		TBD	Call TI	Call TI
TLC34058-110FNR	OBSOLETE	PLCC	FN	84		TBD	Call TI	Call TI
TLC34058-110MGA	OBSOLETE	CPGA	GA	84		TBD	Call TI	Call TI
TLC34058-110MGAB	OBSOLETE	CPGA	GA	84		TBD	Call TI	Call TI
TLC34058-110MHFG	OBSOLETE	CFP	HFG	84		TBD	Call TI	Call TI
TLC34058-135FN	OBSOLETE	PLCC	FN	84		TBD	Call TI	Call TI
TLC34058-80FN	OBSOLETE	PLCC	FN	84		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

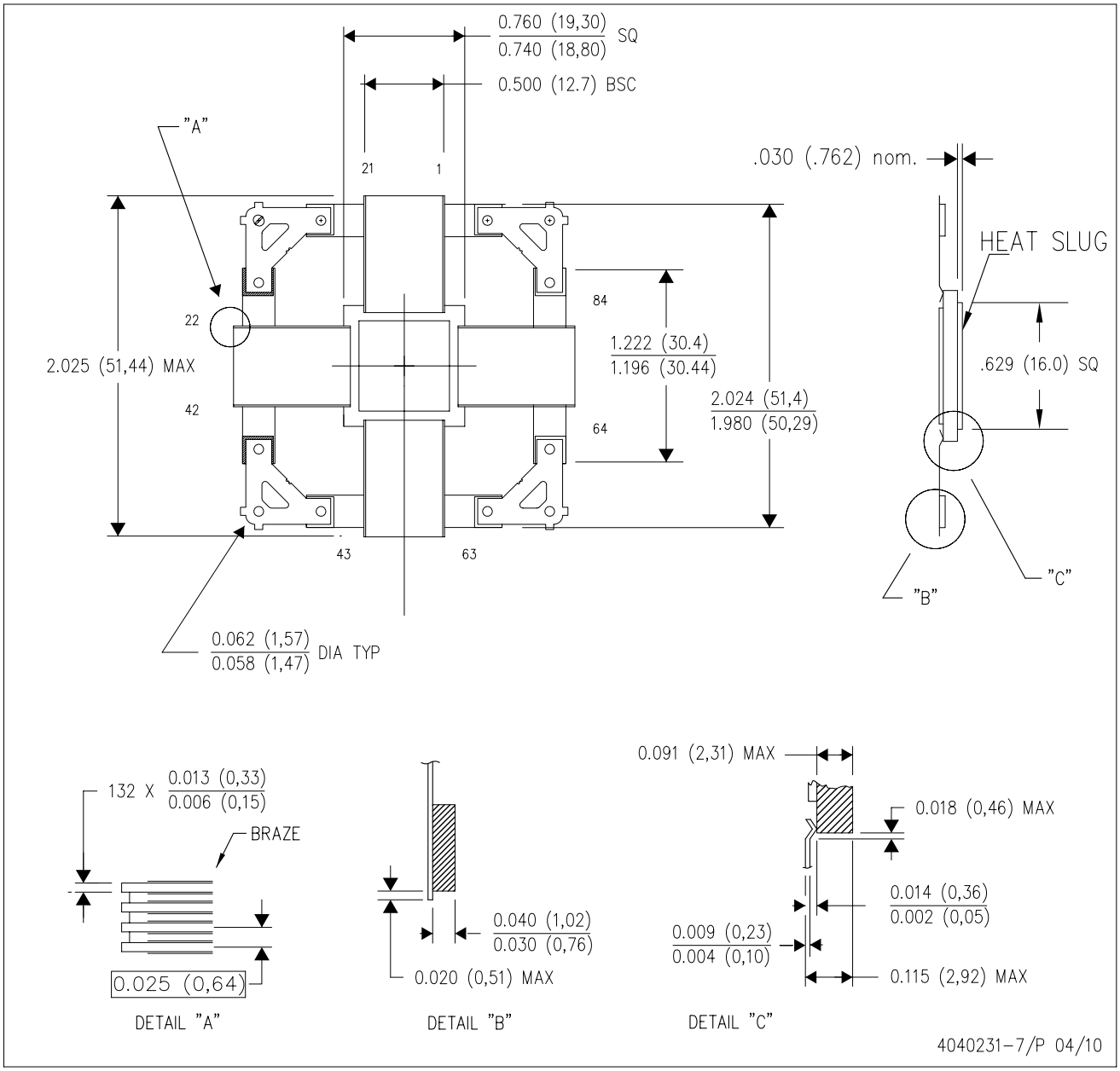
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

HFG (S–CQFP–F84) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

HFG (S–CQFP–F84) CERAMIC QUAD FLATPACK WITH NCTB



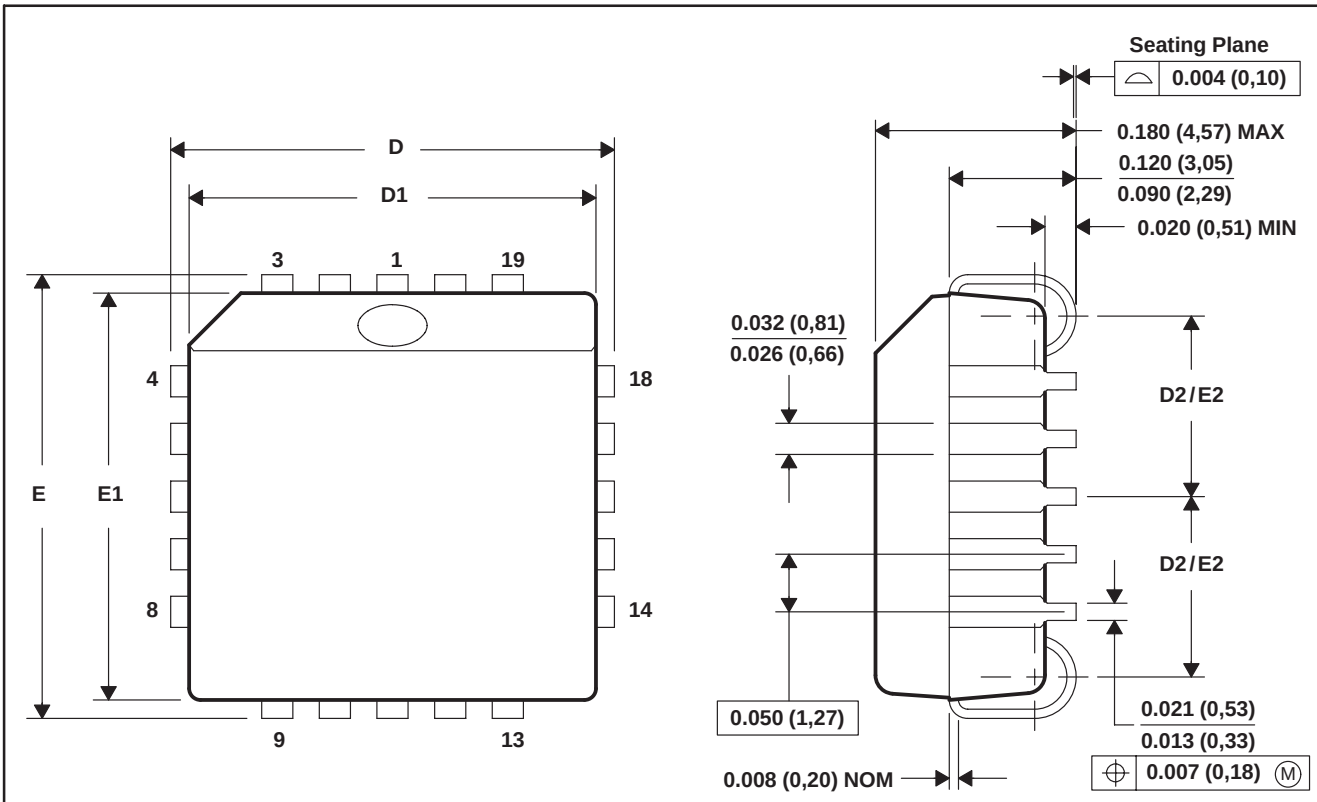
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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