INTEGRATED CIRCUIT

東芝 Toshiba

TECHNICAL DATA

TOSHIBA MOS TYPE DIGITAL INTEGRATED CIRCUIT

TLCS-47

SILICON MONOLITHIC

4-BIT SINGLE CHIP MICROCOMPUTER TLCS-47

GENERAL DESCRIPTION

The TLCS-47 is the high speed and high performance, 4-bit single chip microcomputer series designed for general purpose use.

The TLCS-47 has variously powerful functions in order to meet with the advanced and complicated applications, which will be made in near future. In addition, software compatible NMOS family (TLCS-47N) and CMOS family (TLCS-47C) are also provided.

FEATURES

- 4-bit, single chip microcomputer with built-in
    ROM, RAM, input/output port, divider, timer/counter, and serial port.
- Memory capacity
    - ROM : Max 4,096 × 8 bits
    - RAM : Max   256 × 4 bits
- Instruction execution time
    - NMOS family 2μs(at 4MHz clock)
    - CMOS family 4μs("   )
- Efficient instruction set
    - 90 instructions
    - Software compatible in the series
- Subroutine nesting: Max. 15 levels
- 6 interrupts (External : 2, Internal : 4)
    Independently latched control and multiple interrupt control
- Input/Output (Standard)
    - Input   1 port   4 pins
    - Output(corresponding to PLA)
                   2 ports   8 pins
    - I/O   4 ports 16 pins
    - I/O (Note) 2 ports   7 pins
    Note : These I/O ports are also used for the interrupt input, timer/ counter input, and serial port; therefore, it is programmably selectable for each application.

- PLA data conversion function (instruction) output of data to output port (8-bit)
- Data table look-up and table search function (instruction)
    Table can be set up in the whole ROM area .
- 12-bit timer/counter (2 channels)
- Serial port with 4-bit buffer
- 18-stage divider (with 4-stage prescaler)
- Built-in high output current terminals (NMOS family)
    Typ. 20mA ×8 bits, LED direct drive is available.
- Built-in high breakdown voltage output terminals (CMOS version)
    Max. 42V breakdown voltage
    FL tube direct drive is available.
- Built-in LCD drive circuit (automatic display)(CMOS version)
    - LCD direct drive is available (1/4 duty LCD, Max. 12-digit display)
    - 1/4, 1/3, 1/2 duties or static LCD drive are programmably selectable.
- Stand-by operation (NMOS/CMOS)
    Battery back-up, battery operation and condenser back-up are available.
- On chip oscillator
- TTL/CMOS compatible
- +5V single power supply

253

Configuration of TLCS-47 Series

Family		Name	TLCS-47N				
Item	Unit		TMP4740P	TMP4720P	TMP4700C	TMP4799C	
ROM Capacity	Bytes		4,096	2,048	(External) 4,096	(External) 4,096	
RAM Capacity	Words		256	128	256	256	
Instruction Execution time	μs		2				
No. of instructions			90				
Subroutine nesting	Levels		Max. 15				
Interrupts External			2				
Interrupts Internal			4 (Serial I/O, timer/counter overflow(2), timer of divider)				
Timer/counter	Channels		2				
(Bit length)	Bits		12				
(Mode)			(Event counter, timer and pulse width measurement mode is programmably selectable.)				
Serial port	Bits		4 (With buffer)				
(Mode)			(Receive/transmit mode is programmably selectable.)				
(Clock)			(External/internal, and leading/trailing edge mode are programmably selectable.)				
Divider	Stage		18 (With 4-stage prescaler)				
Input/Output Ports Input			4				
Input/Output Ports Output (corresponding to PLA)			8				
Input/Output Ports I/O	Bits		16				
Input/Output Ports I/O (Combined use)			7				
Input/Output Ports Total			35				
With built-in high output current terminals			8				
With built-in high break-down voltage terminals	Bits		——				
With built-in LCD driver			——				
Memory Standby function			YES				
Hold function			——				
Clock oscillator			With built-in				
Power supply	V		+ 5.0				
Process			Nch Si Gate E/D MOS LSI				
Package			DIP – 42		QIC-80	DIC-42	
Remark					Evaluator Chip	Evaluator Chip(Piggy back type)	

Configuration of Series

Series			TLCS – 47				
Family			TLCS–47N		TLCS–47C		(Evaluator chip)
Item	Unit	Name	TMP4740P	TMP4720P	TMP47C40P	TMP47C20P	TMP47C22F	TMP4700C
ROM Capacity	Bytes		4,096	2,048	4,096	2,048	2,048	(External) 4,096
RAM Capacity	Words		256	128	256	128	192	256
Instruction Execution time	μs		2		4			2
No. of instructions			90					
Subroutine nesting	Levels		Max. 15					
Inter- rupts	External		2					
	Internal		4 (Serial I/O, timer/counter overflow(2), timer of divider)					
Timer/counter	Channels		2					
(Bit length)	Bits		12					
(Mode)			(Event counter, timer and pulse width measurement mode is programmably selectable.)					
Serial port	Bits		4 (With buffer)					
(Mode)			(Receive/transmit mode is programmably selectable.)					
(Clock)			(External/internal, and leading/trailing edge mode are programmably selectable.)					
Divider	Stage		18 (With 4-stage prescaler)					
Input/Output Ports	Input		4				4	4
	Output (corresponding to PLA)	Bits	8				0	8
	I/O		16				16	16
	I/O (Combined use)		7				7	7
	Total		35				27	35
With built-in high output current terminals			YES					YES
With built-in high breakdown voltage terminals					YES			
With built-in LCD driver							YES	
Memory Standby function			YES					YES
Hold function					YES		YES	(YES)
Clock oscillator			With built-in					
Power supply	V		+ 5.0					
Process			Nch Si Gate E/D MOS LSI		Si Gate C²MOS LSI			Nch Si Gate E/D MOS LSI
Package			DIP – 42				FP – 67	QIC – 80