Infineon® LIN LED Driver

TLD7396EK

High Side Driver IC
3 channels

Data Sheet

Rev. 1.0, 2012-067-02

Automotive Power

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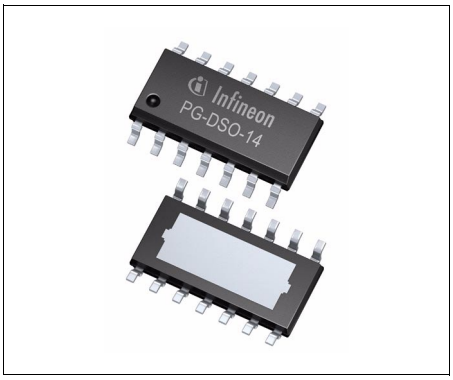
1 Overview



PG-DSO-14-43

Features

- 3 channel device with integrated output stages (current sources), optimized to drive LEDs
- Communication via integrated LIN-transceiver
- LIN-transceiver compatible to LIN 2.1 (20 kbit/s)
- Integrated state machine for LIN protocol handling and LIN-message decoding
- 16 sets of output currents (e.g. color points when using RGB LEDs) can be stored in the integrated non volatile memory (NVM)
- Device Node ID (address) can be stored in the integrated NVM
- Autonomous intensity variation of outputs for theater dimming effects with 12 bit resolution and smooth color transitionings with 10 bit resolution provided by integrated intensity generation unit
- Low current consumption in sleep mode - Wake up via LIN-bus
- Overload protection and under voltage detection
- Wide temperature range: -40 °C < T_j < 150 °C
- 150mil exposed heatslug DSO-package
- Green Product (RoHS compliant)
- AEC Qualified

Description

The Infineon LIN LED Driver IC is a three channel highside driver IC optimized to drive external NPN-transistors. The output current is controlled practically independent of load and supply voltage changes.

The average output current of each channel can be controlled by an 8-bit intensity setting. 16 different sets of intensity settings (i.e. 16 triplets of intensities or average output currents) can be stored in an on-chip non-volatile memory. This is especially useful, when driving a Red-Green-Blue (RGB) LED, where each triplet of intensities represents one color. In addition to these sets of average output currents, the intensities can be dimmed down in 14 steps. The IC also supports theater dimming with a dim-time of up to multiple seconds.

Configuration and diagnosis are done via the integrated LIN interface. LIN 2.1 standard is supported. The integrated state machine supports the LIN protocol handling and command decoding.

Type	Package	Marking
TLD7396EK	PG-DSO-14-43	TLD7396EK

Table 1 Product Summary

Operating voltage	$V_{S(nom)}$	7 V … 18 V
Extended operating voltage (LIN-transceiver active)	$V_{S(ext)}$	6 V… 34V
Minimum supply voltage range for operation, (Outputs active, LIN-transceiver off)	$V_{S(PD)}$	4.8 V
Maximum voltage	$V_{S(max)}$, $V_{OUTx(max)}$	40 V
Maximum output current to drive external NPN-transistors	$I_{PWR(nom,max)}$	40 mA
Current consumption in sleep mode	$I_{S(sleep,typ)}$	16 µA

Protective functions

- ESD protection
- Under voltage lock out
- Over Load protection
- Over temperature prewarning
- Over temperature protection

Diagnostic functions

- LIN communication error detection
- Over load detection via LIN message

Applications

Designed for standard LED lighting applications such as ambient lighting, exterior lighting, interior illumination, dome light, and dash board. Especially well suited for RGB color mixing applications.

2 Block Diagram

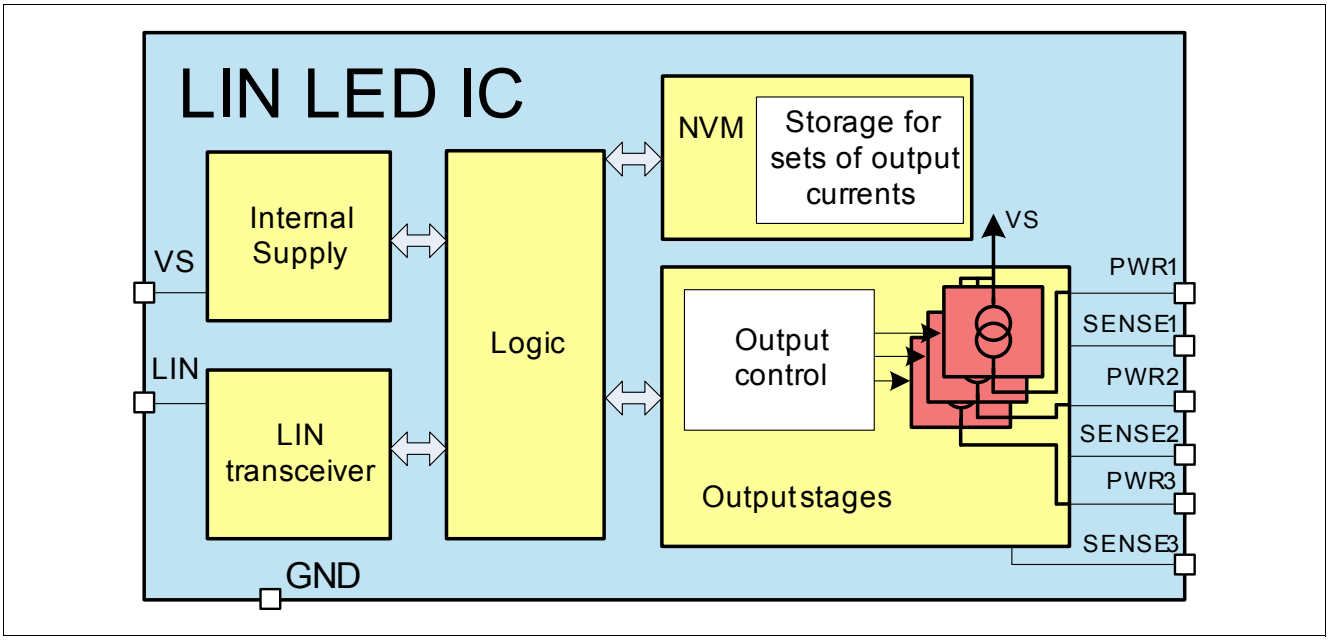


Figure 1 Basic Block Diagram

3 Pin Configuration

3.1 Pin Assignment

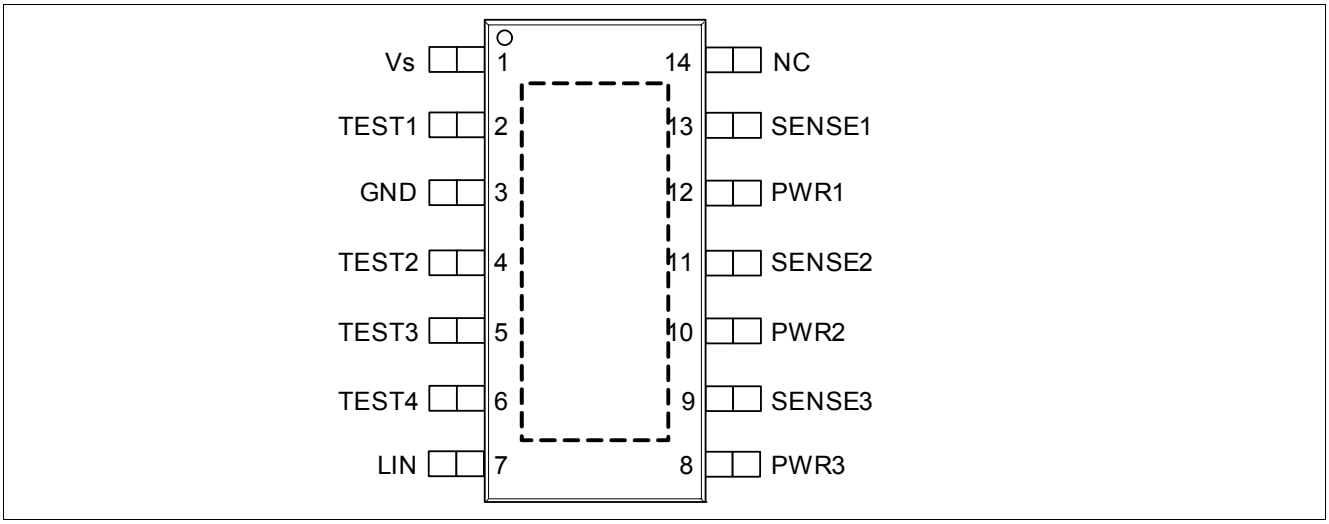


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	
1	V_S	**Supply Voltage;** battery supply, connect an Reverse polarity protection and a decoupling capacitor (100nF - 1µF), see also **Figure 14**
2	TEST1	**Test Pin;** used for Infineon end of line test, connect to GND in application
3	GND	**Ground**
4	TEST2	**Test Pin;** used for Infineon end of line test, leave unconnected in application
5	TEST3	**Test Pin;** used for Infineon end of line test, connect to GND in application
6	TEST4	**Test Pin;** used for Infineon end of line test, connect to GND in application
7	LIN	**LIN Input;** Connected to LIN-master with a filter capacitor (e.g. 220pF) and an external over voltage protection (e.g. MMBZ27VALT1)
8	PWR3	**Base Driver Output 3**
9	SENSE3	**Sense Input 3**
10	PWR2	**Base Driver Output 2**
11	SENSE2	**Sense Input 2**
12	PWR1	**Base Driver Output 2**
13	SENSE1	**Sense Input 1**
14	NC	**Not Connected**
Exposed Pad	GND	**Exposed Pad;** connect to GND in application

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply Voltage	V_S	-0.3	40	V	–
4.1.2	Input Voltage LIN	V_{LIN}	-40	40	V	–
4.1.3	Sense Input Voltage	V_{SENSEx}	-0.3	6	V	–
4.1.4	Base Driver Output Voltage	V_{PWRx}	-0.3	6	V	–
Currents						
4.1.5	Base Driver Output Current	I_{PWRx}	–	60	mA	–
4.1.6	LIN Current	I_{LIN}	–	150	mA	internally limited
Temperatures						
4.1.7	Junction Temperature	T_j	-40	150	°C	–
4.1.8	Ambient Operating Temperature	T_a	-40	85	°C	–
4.1.9	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.10	ESD Resistivity (all pins)	V_{ESD}	-2	2	kV	all pins Human Body Model (100 pF via 1.5 kΩ)[2)]
4.1.11	ESD Resistivity Vs and LIN to GND	V_{ESD}	-6	6	kV	Human Body Model (100 pF via 1.5 kΩ)[2)]
4.1.12	ESD Resistivity all pins	V_{ESD}	-500	500	V	CDM[3)]
4.1.13	ESD Resistivity corner pins	V_{ESD}	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001-2011

3) ESD susceptibility, Charged Device Model “CDM” according to JESD22-C101E

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.14	Supply Voltage Range for Normal Operation	$V_{S(nom)}$	7	18	V	–
4.2.15	Extended Supply Voltage Range for Operation, LIN-transceiver active	$V_{S(ext)}$	6	34	V	Parameter deviations possible, see also **Figure 4**
4.2.16	Extended Supply Voltage Range for Operation, Outputs active; LIN-transceiver off	$V_{S(ext,noLIN)}$	$V_{S(PD)}$	–	V	Parameter deviations possible, see **Spec. Pos. 5.3.6**
4.2.17	Supply Voltage transients slew rate	dV_S/dt	5	5	V/µs	1)
4.2.18	Junction Temperature	T_j	-40	150	°C	–

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	6	–	K/W	1) based on simulation results
4.3.2	Junction to Ambient 1s0p board	R_{thJA}	–	65	–	K/W	1) 2)
4.3.3	Junction to Ambient 2s2p board	R_{thJA}	–	38	–	K/W	1) 3)

1) Not subject to production test, specified by design

2) The R_{thJA} values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 70µm Cu, 300 mm^2 cooling area. T_a = 85°C, total power dissipation 1.5 W distributed statically and homogeneously over all output stages.

3) The R_{thJA} values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm³ board with 2 inner copper layers (outside 2 x 70 µm Cu, inner 2 x 35µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. T_a = 85°C, total power dissipation 1.5 W distributed statically and homogeneously over all output stages.

5 State Machine and Operating Modes

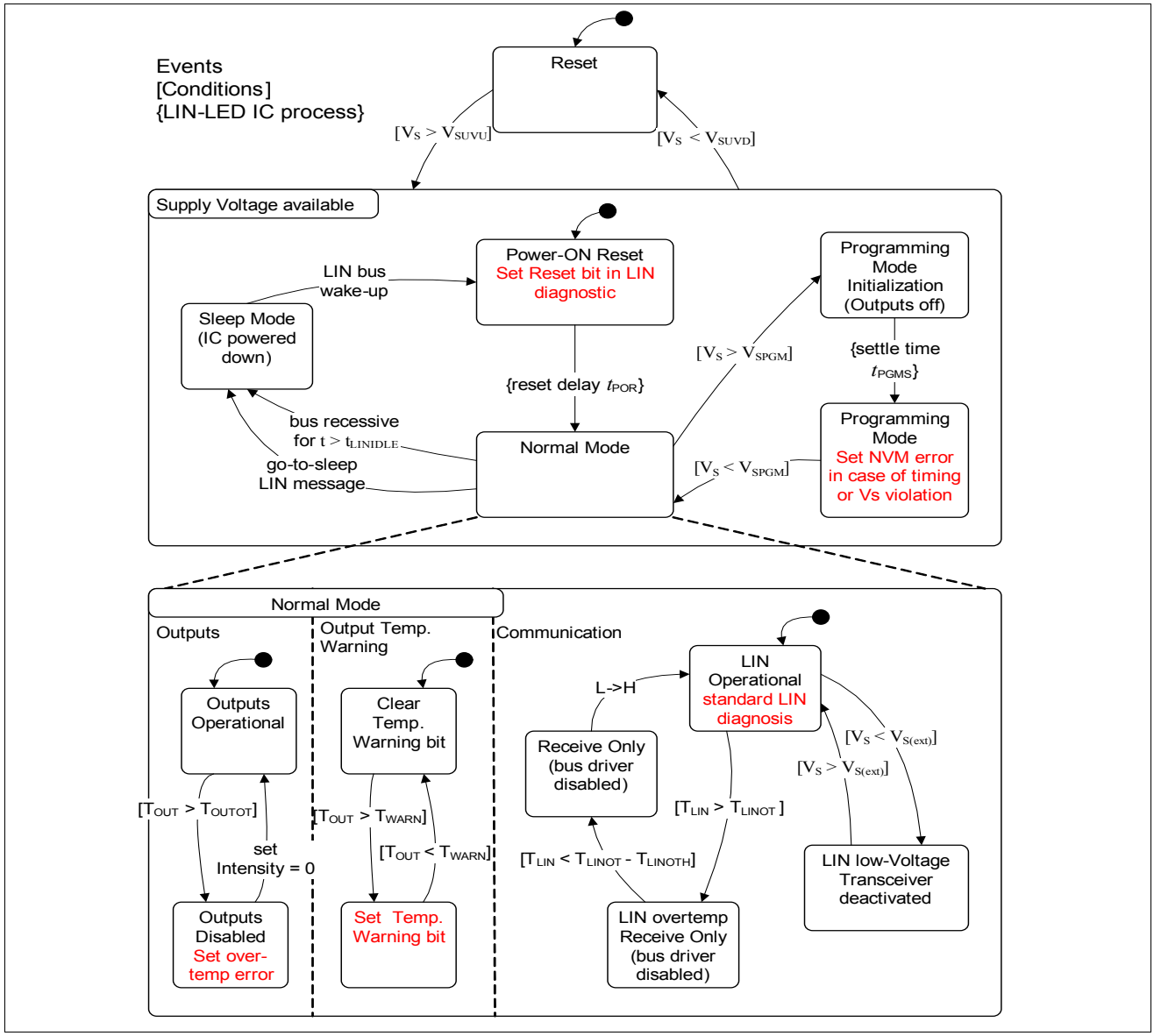


Figure 3 State-Chart, diagnostic features are highlighted in red

Table 2 State-Chart Legend

Symbol	Comment	Symbol	Comment
V_S	Supply Voltage at Vs pin	$t_{PGM(s)}$	Programming mode settle time, **Pos. 8.5.3**
$V_{S(ext)}$	Extended Supply Voltage range, **Pos. 4.2.15**	T_{LIN}	Temperature of LIN-bus driver
$V_{S(PU)}$	Power-Up Voltage, **Pos. 5.3.5**	$T_{LIN(OT)}$	LIN over temperature protection, **Pos. 6.3.25**
$V_{S(PD)}$	Power-Down Voltage, **Pos. 5.3.6**	$T_{LIN(OT,H)}$	LIN over temperature protection hysteresis, **Pos. 6.3.26**
$V_{S(PGM)}$	Programming Voltage, **Pos. 8.5.1** and **Pos. 8.5.2**	T_j	Temperature of Output power stages

Table 2 State-Chart Legend

Symbol	Comment	Symbol	Comment
$t_{LIN(idle)}$	LIN communication time out, **Pos. 6.3.23**	$T_{j(OT)}$	Output deactivation threshold, **Pos. 9.5.11**
t_{POR}	Power-ON Reset delay, **Pos. 5.3.4**	$T_{j(warn)}$	Output prewarning threshold, **Pos. 9.5.10**

5.1 Operating Modes

5.1.1 Normal Mode

Normal Mode is the default operating state and is automatically entered after the device goes through a power-on reset.

During normal mode the device interprets LIN bus messages in order to control the set of intensities (color points) and intensity of the RGB diode. The interpreted LIN instructions include:

- Selection of 1 of 16 average current set points stored in the integrated NVM
- Intensity setting
- Intensity ramp up/down for theater dimming effects
- Selection of the individual (RGB) intensities (e.g. for calibration)
- Request to respond to LIN-master with status and error diagnostic information
- Go to sleep mode

*Note: A LIN-communication at frequencies around f_{FLASH} during normal mode ($V_S < V_{S(PGM,L)}$) or in programming mode ($V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$, (**Pos. 8.5.1** and **Pos. 8.5.2**)) without being the subscriber, brings the device into a stop-mode. A LIN-communication of the device is not possible any more until the LIN communication time out $f_{LIN(idle)}$ (**Pos. 6.3.23**) is exceeded and the device enters the sleep mode, or a power-on reset is done.*

5.1.2 Programming Mode (Flash-Mode)

This mode is used to program the NVM. More details on the NVM programming can be found in **Chapter 8.2**. To enter this mode the user has to apply a supply voltage V_S within the programming voltage range $V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$ (**Pos. 8.5.1** and **Pos. 8.5.2**) for longer than the programming settle time $t_{PGM(s)}$ (**Pos. 8.5.3**). This also enables the LIN-transceiver flash-mode for higher speed data transmission. The maximum transmission rate on the LIN-bus can be increased to f_{FLASH} (**Pos. 6.3.24**). In this operation mode all three output stages are turned off.

*Note: Please consider the important note in **Chapter 5.1.1**.*

5.1.3 Sleep Mode

In order to reduce the current consumption the LIN LED Driver IC offers a sleep mode. In sleep mode the quiescent current on V_S and the leakage current on the pin LIN are cut back to a minimum.

To switch the LIN LED Driver IC from normal operation mode to sleep mode, the LIN-message “Go to Sleep” has to be received by the LIN LED Driver IC.

While the LIN LED Driver IC is in sleep mode the following functions are available:

- The output stage is disabled and the internal LIN-bus terminations are switched off (high impedance on the pin LIN). The internal current source on the LIN-pin ensures that the levels on the pin LIN remains recessive and protects the LIN-network against accidental bus Wake-Up events.
- The receiver stage is turned off.

The LIN-bus wake-up comparator is active and turns the LIN LED Driver IC to normal operation mode in case of a bus wake-up event.

5.2 Internal Supply Unit

5.2.1 Power-On Reset

In case V_S is dropping below the Power-On reset level V_S < $V_{S(PD)}$, the LIN LED Driver IC is in Reset condition. In Reset condition the output stages of the LIN LED Driver IC are disabled and no communication is possible.

If the power supply V_S reaches a higher level as the minimum operating voltage level V_S > $V_{S(PU)}$, the LIN LED Driver IC will become active again. The Error bit “Reset” is set to 1 and cleared after the next valid diagnosis request frame (LED_L1_P00 or LED_L1_P01).

During a Power-On Reset all registers are set to their default value. The settings programmed in the NVM will not be changed during a Power-On Reset.

5.2.2 Low Voltage Behavior

The LIN LED Driver IC has under voltage detection and shut-off integrated in order to prevent erroneous operation at low supply voltages.

With Vs below $V_{S(nom)min}$ (**Pos. 4.2.14**) but above $V_{S(ext)min}$ (**Pos. 4.2.15**) the device functions, but specification parameter deviations are possible, the integrated LIN-transceiver is active. With Vs below $V_{S(ext)min}$ (**Pos. 4.2.15**) but above $V_{S(PD)}$ (**Pos. 5.3.6**) the output stages remain on, the internal logic will be active and the content of the internal registers is not cleared. The integrated LIN-transceiver is deactivated (communication is blocked). As soon as the supply voltage is above $V_{S(ext)min}$ (**Pos. 4.2.15**) again the integrated LIN-transceiver is activated again without generating any diagnostic error.

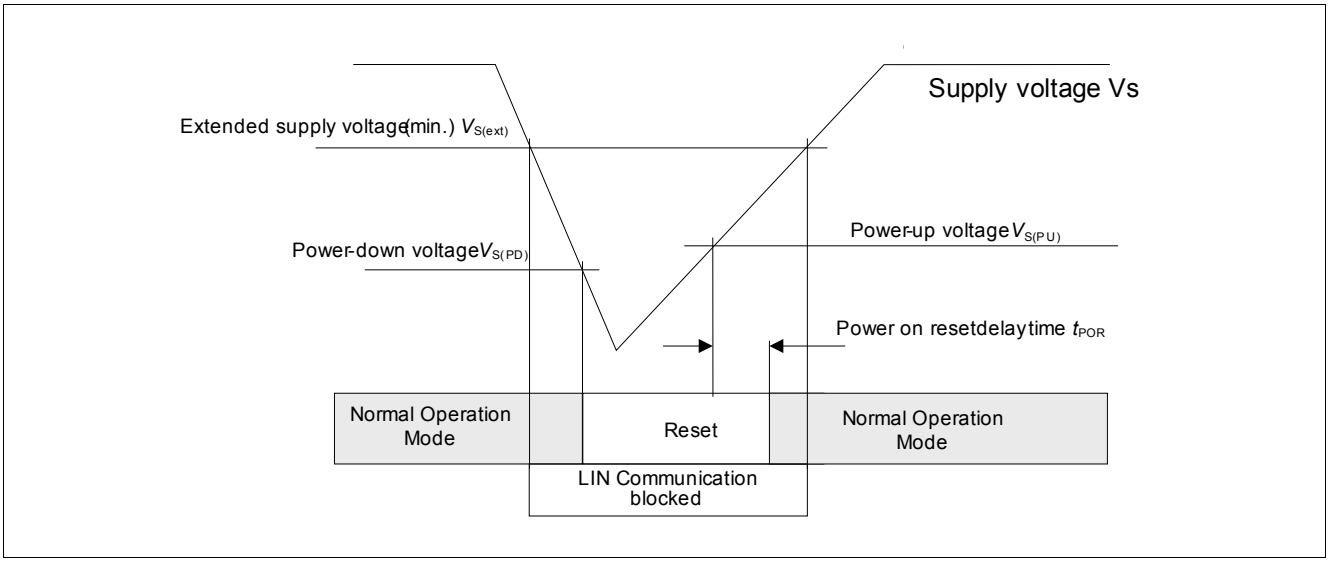


Figure 4 Power-on reset / Low voltage behavior

5.3 Electrical Characteristics Internal Supply

Electrical Characteristics: Supply

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Supply current consumption in sleep mode	$I_{S(sleep)}$	–	–	18	µA	V_S = 16 V; V_{LIN} = V_s
5.3.2	Typical supply current consumption in sleep mode	$I_{S(sleep,typ)}$	–	–	16	µA	1) T_j < 85 °C V_S = 13.5 V V_{LIN} = V_S
5.3.3	Current consumption at V_S in normal operation mode	I_S	–	–	8	mA	I_{PWRx} = 0 mA outputs off
5.3.4	Power on reset delay time	t_{POR}	–	–	5	ms	1)see **Figure 4**
5.3.5	Power-up voltage	$V_{S(PU)}$	4	–	5	V	see **Figure 4**
5.3.6	Power-down voltage	$V_{S(PD)}$	–	–	4.8	V	see **Figure 4**
5.3.7	Under-voltage hysteresis	$V_{S(PU)}$ - $V_{S(PD)}$	100	–	–	mV	1) –

1) Not subject to production test, specified by design

6 LIN-Interface

The LIN LED Driver IC provides a LIN-transceiver and LIN protocol handler. The specification supports LIN 2.1 standard. The IC also contains an application specific message decoder. It decodes messages from the LIN-master and provides commands for configuration, control, and diagnosis of the LIN LED Driver IC via the LIN-interface.

6.1 LIN-Basics

The LIN-bus (Local Interconnect Network) is a one-wire bus system. The data is transmitted via a single data line between one LIN-master and multiple LIN-slave devices (up to 16). All LIN-slaves are connected in parallel to the LIN-bus, which reduces the wiring effort to a minimum. The LIN-bus uses the supply voltage as reference voltage.

The LIN-master initiates every communication. Therefore, the master sends out a header with a defined message content. According to this header the addressed slave-devices perform the requested action or provide their information on the bus (via putting the LIN-bus to recessive state (high potential, close to the supply voltage) or dominant state (low potential)). The default state of the LIN-bus is high potential.

The LIN-messages are called LIN-frames. LIN-frames, which requests only an action (e.g. switch on a channel) at the slave devices, are called master published frame-IDs. LIN-frames, which request an answer of the slave-device, start with the slave frame-ID and are called slave published frame-IDs.

6.2 Physical Layer

The integrated LIN-transceiver is the physical layer interface between the protocol handler and the physical bus. It is especially suited to drive the bus line in LIN-systems in automotive and industrial applications. The device acts as a LIN-slave on the network. The logical values stored in the registers of the protocol handler are driven to the physical LIN-bus when data is requested from the LIN-master. Physical LIN-bus information from the master is transferred into the registers of the protocol handler for command and control of the LIN LED Driver IC. The transceiver offers excellent EMC performance within a broad frequency range independent of battery voltage. This is achieved by implementing a slope control mechanism based on a constant slew rate.

6.2.1 LIN-Specifications 2.1

The TLD7396EK IC fulfills the Physical Layer Specification LIN 2.1.

6.2.2 Wake-Up via LIN-bus

The LIN-bus Wake-Up event, often called remote Wake-Up, changes the operation mode from sleep mode to normal operation mode. A falling edge on the LIN-bus, followed by a dominant bus signal t > $t_{WK(LIN)}$ (**Pos. 6.3.20**) results in a bus Wake-Up event.

The mode change to normal operation mode becomes active with the following rising edge on the LIN-bus (see also **Figure 5**). This rising edge starts the Power-On Reset. After the time $t_{START(LIN)}$ (**Pos. 6.3.21**) the Power-On Reset is completed and the device is able to receive LIN messages.

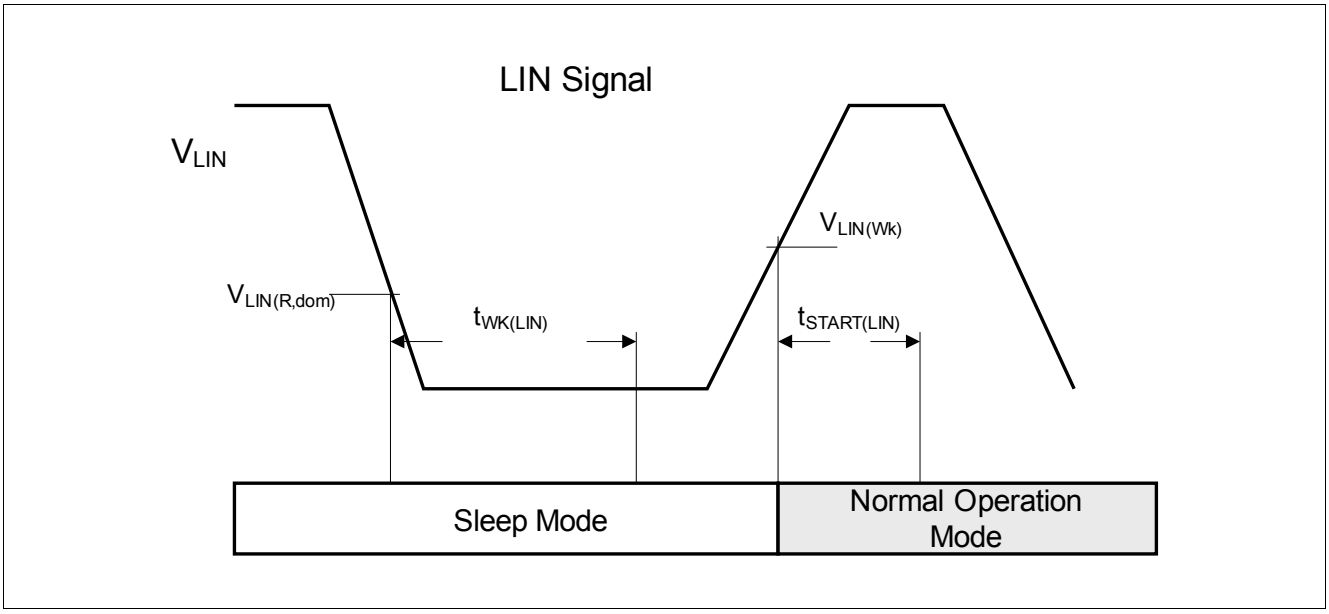


Figure 5 LIN Wake-Up behavior

6.2.3 LIN Operation During Low V_S Voltage

If the supply voltage at the Vs pin drops below the extended operating voltage range $V_{S(ext)min}$ (**Pos. 4.2.15**), the integrated LIN-transceiver terminates communication. This feature is implemented to avoid any permanent dominant or erroneous signals on the LIN-bus. When the supply voltage rises above the detection threshold $V_{LIN(wk)}$ (**Pos. 6.3.7**), communication is re-enabled. The LIN-bus termination remains active during under voltage operation. When the supply voltage is removed, the LIN-bus output is switched to high impedance in order to not disrupt bus communication.

6.2.4 LIN-bus Driver Over Temperature Protection

The LIN-bus driver within the transceiver has an integrated over temperature sensor to protect the driver from thermal overstress. If the integrated LIN driver temperature reaches a critical temperature $T_{LIN(OT)}$ (**Pos. 6.3.25**) the LIN-bus driver will be deactivated and the transceiver will be switched to receive only mode. If the chip has cooled down more than the temperature hysteresis $\Delta T_{LIN(OT)}$ (**Pos. 6.3.26**) below $T_{LIN(OT)}$ the LIN-bus driver will be activated again. To avoid a bit failure after cooling down, the bus driver remains off till the next dominant to recessive transmission initiated by the LIN LED Driver IC state machine.

The failure is not indicated in the LIN diagnostic response.

6.2.5 LIN message Idle Time

If the LIN-bus is recessive for more than $t_{LIN(idle)}$ (**Pos. 6.3.23**) between two LIN messages, the device will change from normal operation mode to sleep mode.

6.2.6 Oscillator Tolerance

The LIN LED Driver IC uses the sync field to synchronize its internal clock for LIN communication. According to the LIN calculation table, an oscillator clock tolerance < 2% with respect to the master sync signal is maintained within one LIN frame.

6.3 Electrical Characteristics LIN-transceiver

Electrical Characteristics: LIN-transceiver

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
LIN-bus Receiver							
6.3.1	Receiver threshold voltage, recessive to dominant edge	$V_{LINth(R,dom)}$	0.4 × V_S	0.45 × V_S		V	–
6.3.2	Receiver dominant state	$V_{LIN(R,dom)}$	–	–	0.4 × V_S	V	LIN Spec 2.1 (Par. 17)
6.3.3	Receiver threshold voltage, dominant to recessive edge	$V_{LINth(R,rec)}$		0.55 × V_S	0.6 × V_S	V	–
6.3.4	Receiver recessive state	$V_{LIN(R,rec)}$	0.6 × V_S	–	1.15 x V_S	V	[1] LIN Spec 2.1 (Par. 18)
6.3.5	Receiver center voltage	$V_{LIN(R,CNT)}$	0.475 × V_S	–	0.525 × V_S	V	[2] LIN Spec 2.1 (Par. 19)
6.3.6	Receiver hysteresis	$\Delta V_{LIN(R)}$	0.07 × V_S	0.12	0.175 × V_S	V	[3] LIN Spec 2.1 (Par. 20)
6.3.7	Wake-up threshold voltage	$V_{LIN(wk)}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–
LIN-bus Transmitter							
6.3.8	Bus short circuit current	$I_{LIN(LIM)}$	40	100	150	mA	V_{LIN} = 13.5 V LIN Spec 2.1 (Par. 12)
6.3.9	Leakage current during loss of GND	$I_{LIN(no\ GND)}$	-1000	–	5	µA	V_S = 0 V V_{LIN} = -12 V LIN Spec 2.1 (Par. 15)
6.3.10	Leakage current during loss of Vs	$I_{LIN(no\ Vs)}$	–	–	5	µA	V_S = 0 V V_{LIN} = 18 V LIN Spec 2.1 (Par. 16)
6.3.11	Leakage current during LIN transmitter off and bus dominant	$I_{LIN(PAS\ dom)}$	-1	–	–	mA	V_S = 18 V V_{LIN} = 0 V LIN Spec 2.1 (Par. 13)
6.3.12	Leakage current during LIN transmitter off and bus recessive	$I_{LIN(PAS\ rec)}$	–	–	20	µA	V_S = 8 V V_{LIN} = 18 V LIN Spec 2.1 (Par. 14)
6.3.13	Bus pull-up resistance	R_{slave}	20	30	47	kΩ	Normal Mode LIN Spec 2.1 (Par. 26)

Electrical Characteristics: LIN-transceiver (cont'd)

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.14	Propagation delay LIN-bus to RxD Dominant to RxD Low Recessive to RxD High	 $t_{rx(pdf)}$ $t_{rx(pdr)}$	 – –	 1 1	 6 6	 µs µs	[4] LIN Spec 2.1 (Par. 31) R_{RxD} = 2.4 kΩ C_{RxD} = 20 pF
6.3.15	Receiver delay symmetry	$t_{rx(sym)}$	-2	–	2	µs	[4] LIN Spec 2.1 (Par. 32) $t_{rx(sym)} = t_{rx(pdf)} - t_{rx(pdr)}$ R_{RxD} = 2.4 kΩ C_{RxD} = 20 pF
6.3.16	Duty cycle D1	D_1	0.396	–	–		[5] duty cycle 1 $TH_{Rec}(max) = 0.744 \times V_S$ $TH_{Dom}(max) = 0.581 \times V_S$ V_S = 7.0…18 V t_{bit} = 50 µs $D_1 = t_{LIN\_rec(min)}/(2\ t_{bit})$ LIN Spec 2.1 (Par. 27)
6.3.17	Duty cycle D2	D_2	–	–	0.581		[5] duty cycle 2 $TH_{Rec}(min) = 0.422 \times V_S$ $TH_{Dom}(min) = 0.284 \times V_S$ V_S = 7.6…18 V t_{bit} = 50µs $D_2 = t_{LIN\_rec(max)}/(2\ t_{bit})$ LIN Spec 2.1 (Par. 28)
6.3.18	Duty cycle D3	D_3	0.417	–	–		[5] duty cycle 3 $TH_{Rec}(max) = 0.778 \times V_S$ $TH_{Dom}(max) = 0.616 \times V_S$ V_S = 7.0…18 V t_{bit} = 96µs $D_3 = t_{LIN\_rec(min)}/(2\ t_{bit})$ LIN Spec 2.1 (Par. 29)

Electrical Characteristics: LIN-transceiver (cont'd)

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.19	Duty cycle D4	D_4	–	–	0.590		5) duty cycle 4 TH_{Rec}(min) = 0.389 × V_S TH_{Dom}(min) =0.251 × V_S V_S = 7.6… 18 V t_{bit} = 96µs D_4 = $t_{LIN\_rec(max)}$/(2 t_{bit}) LIN Spec 2.1 (Par. 30)
6.3.20	Dominant time for LIN-bus Wake-Up	$t_{WK(LIN)}$	30	–	150	µs	–
6.3.21	LIN start-up time	$t_{START(LIN)}$	–	–	5	ms	4) time from V_{LIN} > $V_{LIN(wk)}$ until LIN message can be received, see **Figure 5**
6.3.22	Internal BUS dominant time out	$t_{timeout}$	6	9	12	ms	–
6.3.23	LIN communication time out	$t_{LIN(idle)}$	4	8	10	s	–
6.3.24	LIN flash mode speed	f_{FLASH}	112.7	115	117.3	kbit/s	4) –
6.3.25	LIN over temperature protection	$T_{LIN(OT)}$	150	–	–	°C	4) –
6.3.26	LIN over temperature protection hysteresis	$\Delta T_{LIN(OT)}$	–	15	–	°C	4) –
6.3.27	LIN clock tolerance	$k_{LIN(CLK)}$	0.98	–	1.02	-	4) $f_{LIN(CLK)} = k_{LIN(CLK)} * f_{MSTR\text{-}Sync}$

1) Maximum limit not subject to production test, specified by design
2) $V_{LIN(R,CNT)}$ = ($V_{LINth(R,dom)}$ + $V_{LINth(R,rec)}$)/2; see LIN spec. for variable definition
3) $\Delta V_{LIN(R)}$ = $V_{LIN(R,rec)}$ - $V_{LIN(R,dom)}$
4) Not subject to production test, specified by design
5) Bus load concerning LIN Spec 2.1:
   Load 1 = 1 nF / 1 kΩ = C_{LIN} / R_{LIN}
   Load 2 = 6.8 nF / 660 Ω = C_{LIN} / R_{LIN}
   Load 3 = 10 nF / 500 Ω = C_{LIN} / R_{LIN}

6.4 Protocol Handler (Data Link Layer)

Every data transfer is initiated from the master by sending a header. This header contains a sync-break field, a sync byte and a protected identifier byte (PID). The PID contains the frame identifier (frame-ID) and the parity. The frame-ID defines the response, which is sent by the master or the slave immediately after the header. The response contains 1 to 8 data bytes and one checksum byte (end of frame). The producer of any information is called “Publisher” and the consumer of this information is called “Subscriber”.

Except the sync-break field, LIN frames are byte oriented and the LIN specification allows a delay between bytes (interbyte delay). Every byte has a start bit, 8 data bits and one stop bit. The bits are encoded with value 0 (dominant) or 1 (recessive). The LSB is the first bit and the MSB the last bit in a bit stream of a data byte.

Figure 6 shows a complete LIN frame for an identifier using 4 data bytes in the response field. The sync-break re-initializes the receiver and marks in any case the start of a frame.

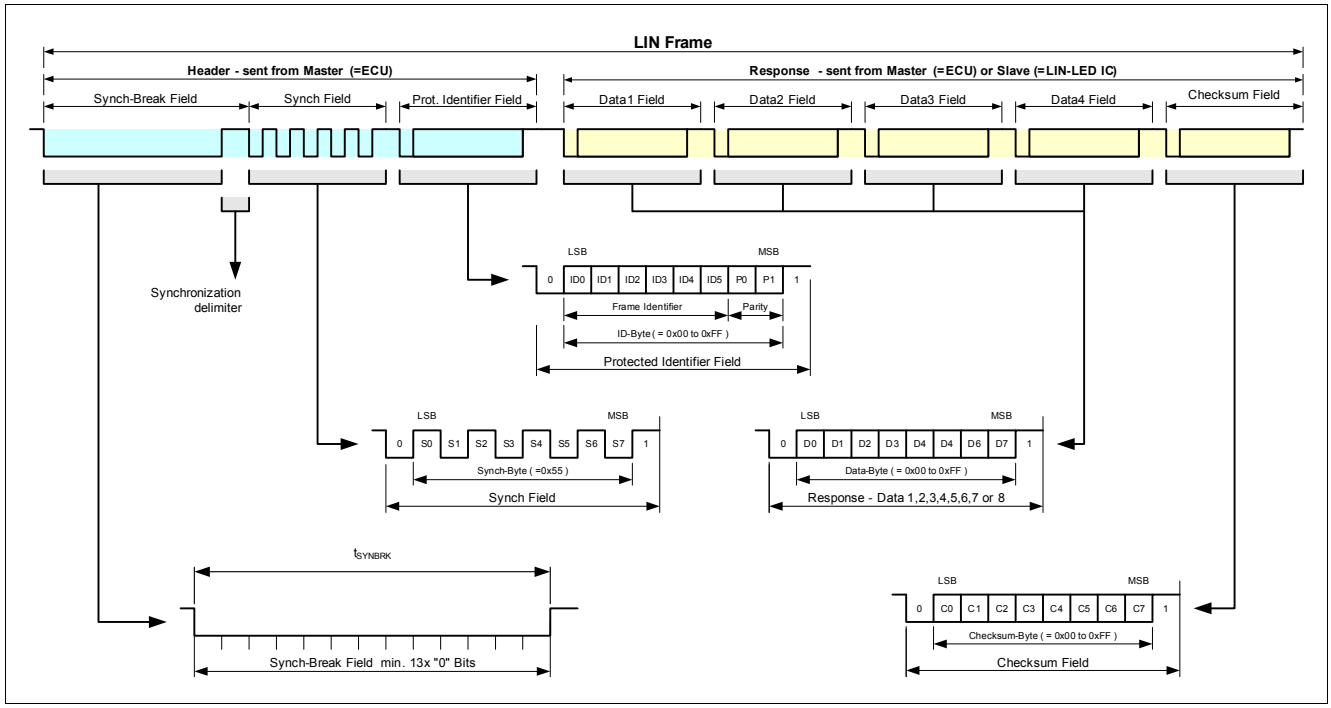


Figure 6 LIN Frame

The value of the checksum byte is calculated following the LIN 2.1 standard (enhanced checksum). The checksum contains the inverted eight bit sum with carry over all data bytes and the protected identifier. The frame-ID 0x3C (go to sleep command) uses the classic checksum, which contains the inverted eight bit sum with carry over all data bytes (but not the protected identifier). This is in line with LIN 2.1 that requests classic checksum for the diagnostic frames for downward compatibility and with J2602, which specifies enhanced checksum.

6.4.1 LIN Communication Error Detection

The LIN LED Driver IC has an integrated monitoring functions to detect errors in the LIN communication between the master and the slaves. These errors include:

- Data Error
- Checksum Error
- Byte Field Framing Error
- ID Parity Error

If the LIN-bus is recessive for more than $t_{timeout}$ during the transmission of a LIN message the receiver is re-initialized. That means, the synchronization delimiter or any interbyte space must not exceed $t_{timeout}$ otherwise the frame is lost.

The status on the LIN-bus can be read out using the register LEDLINStatus of the LIN frame LED_L1_P00. If there are errors in the LIN communication the LIN driver stage remains active.

6.5 LIN Message Decoder (Application Layer)

The LIN LED Driver IC understands seven communication frames (messages). Five frames are for master-to-slave data transfer (i.e. TLD7304EK is the subscriber) and two frames are for slave-to-master data transfer (i.e. LIN LED Driver IC is the publisher). **Table 3** gives an overview over the used message frames.

Note: The frame identifiers for master-to-slave and slave-to-master data transfers are not supposed to overlap!

Table 3 Frame Overview

Frame Symbol	frame-ID	LIN LED Driver IC is	Checksum	Description
MSTR_L1_P00	frame_ID_mstr e.g. 0x00	Subscriber	enhanced	Master sends color, intensity and intensity ramp setting to slave. This is the standard command used in the application
MSTR_L1_P01	frame_ID_mstr + 1 e.g. 0x01	Subscriber	enhanced	Master sends direct intensity information per output (Out1, 2, 3) to slave. This command can be used for LED calibration or direct output control independent of the sets of output currents stored in the NVM
MSTR_L1_P02	frame_ID_mstr + 2 e.g. 0x02	Subscriber	enhanced	Master erases or writes data into NVM of slave. This command should not be used once the LIN LED Driver IC is connected to an application LIN network.
MSTR_L1_P03	frame_ID_mstr + 3 e.g. 0x03	Subscriber	enhanced	Master sends dim-time setting to slave. This is an optional command that can be used in the application in case alternative dim-times are required
MSTR_L1_P04	0x3C	Subscriber	classic	Master Request frame
LED_L1_P00	frame_ID_slave e.g. 0x0D	Publisher	enhanced	LIN LED Driver IC sends diagnostic information back to master. This command is used for network diagnostic, e.g. a roll-call at system start-up
LED_L1_P01	frame_ID_slave + 1 e.g. 0x0E	Publisher	enhanced	LIN LED Driver IC sends content of NVM back to master. This command can be used to verify successful NVM
LED_L1_P02	0x3D	Publisher	classic	Slave Response frame

6.5.1 Frame Identifiers

The LIN LED Driver IC is intended to be used multiple times as a slave in the same LIN network. To differentiate different slaves (different LIN LED-devices), it is necessary to assign specific frame-IDs to the slave published frames.

6.5.2 Slave Published Frame-IDs

The frame-IDs for the two slave published frames are defined by the 6-bit register frame_ID_slave in the non-volatile memory. The frame_ID_slave has to be programmed into the device prior to being connected to the physical LIN network. The first frame-ID for the message LED_L1_P00 is the content of this register. The frame-

ID for the message LED_L1_P01 is set to frame_ID_slave + 1. The NVM register is set to the default value of 0x34. In order to detect not properly programmed devices, the user may leave the Frame ID 0x34 unassigned in his network configuration.

Frame_ID_slave values between 0x00 and 0x38 can be used unrestricted (except the master published frame-IDs). The LIN 2.1 spec reserves the frame-IDs 0x3E - 0x3F for diagnostic purposes. Therefore, frame_ID_slave values higher than 0x3A, which should be programmed to the NVM, are not stored in the NVM. The protocol handler uses in such cases the default value of 0x34 to avoid a conflict with the reserved frame-IDs. This is also shown in **Table 4**.

Note: In the NVM programming mode the LIN LED device answers with 1 stop-bit on slave frame-IDs.

Table 4 Slave Published Frame ID Examples

Frame ID for LED_L1_P00 (= NVM register frame_ID_slave)	**Frame ID for LED_L1_P01** (generated by LIN LED Driver IC)
0x00	0x01
0x04	0x05
0x08	0x09
0x0C	0x0D
0x10	0x11
0x14	0x15
0x18	0x19
0x1C	0x1D
0x20	0x21
0x24	0x25
0x28	0x29
0x2C	0x2D
0x30	0x31
0x34 (default)	0x35 (default)

6.5.3 Master Published Frame-IDs

To increase the flexibility of the LIN LED Driver IC, the frame IDs for the four master published frames MSTR_L1_P00 - P03 are also configurable using the same scheme. The frame-ID for MSTR_L1_P00 is the content of the NVM register frame_ID_mstr, which has to be programmed into the device prior to being connected to the physical LIN network. The default frame-IDs are 0x00 - 0x03, the other frame-ID options are shown in **Table 5**. Values of frame-ID_mstr, which lead to assignment of reserved frame-IDs (e.g. values higher than 0x38), are ignored and the default value is used.

The go to sleep command MSTR_L1_P04 has a fixed frame-ID of 0x3C, (data byte 0 has to contain value 0x00).

In order to avoid bus conflicts, the user has to program frame_ID_slave and frame_ID_mstr to values, which do not overlap.

Note: In the NVM programming mode master published frame-IDs have to use 2 or more stop-bits.

Table 5 Master Published Frame-IDs

Frame ID for MSTR_L1_P00 (= NVM register frame_ID_mstr)	Frame ID for MSTR_L1_P01	Frame ID for MSTR_L1_P02	Frame ID for MSTR_L1_P03	Frame ID for MSTR_L1_P04
0x00 (default)	0x01 (default)	0x02 (default)	0x03 (default)	0x3C (fixed ID)
0x01	0x02	0x03	0x04	
0x02	0x03	0x04	0x05	
...	...	...	...	
0x37	0x38	0x39	0x3A	
0x38	0x39	0x3A	0x3B	

6.5.4 Location Identifier

In addition to the frame-IDs discussed in the previous sections, LIN LED Driver IC offers an additional ID to increase the flexibility of usage. This ID is called location ID. It allows to build up groups of devices, which can be dressed by a single command. Therefore, multiple LIN LED devices can be programmed at the same time. This allows a reduced communication effort on the LIN-bus and does not cause any unwanted switch on delays of devices caused by sequential LIN-messages.

The location ID has to be programmed into the device prior to being connected to the physical LIN network. The location ID is 8 bit long and is subdivided into a 4 bit zone information and a 4 bit location information. This is shown in detail in **Table 6**. For instance, the slave with the location ID 0x73 can be addressed by a master-frame with the location IDs 0x73, 0x70, 0x40 and 0x00. The default location ID is set to 0xFF. In order to detect not properly programmed devices, the user shall leave the location ID 0xFF unassigned in his network configuration. A 0xFF location ID in the NVM generates a “not configured” error in the diagnostic frame (see **Chapter 6.6.6**)

Table 6 Location Identifier

Broadcast “All”	Super-Zone	Zone	Location IDs
0x00	-	0x10	0x11, 0x12, ... 0x1F
	-	0x20	0x21, 0x22, ... 0x2F
	-	0x30	0x31, 0x32, ... 0x3F
	0x40	0x50	0x51, 0x52, ... 0x5F
		0x60	0x61, 0x62, ... 0x6F
		0x70	0x71, 0x72, ... 0x7F
		0x80	0x81, 0x82, ... 0x8F
	-	0x90	0x91, 0x92, ... 0x9F
	-	0xA0	0xA1, 0xA2, ... 0xAF
	-	0xB0	0xB1, 0xB2, ... 0xBF
	-	0xC0	0xC1, 0xC2, ... 0xCF
	-	0xD0	0xD1, 0xD2, ... 0xDF
	-	0xE0	0xE1, 0xE2, ... 0xEF
	-	0xF0	0xF1, 0xF2, ... 0xFF[1)]

1) The Location ID 0xFF shall not be used in the application. A Location ID of 0xFF generates an ApInfo3 error (slave not configured)

6.6 Message Frame Decoding

6.6.1 MSTR_L1_P00 Message Frame (Set color and intensity)

This is the standard command used in the application to set and change colors (from the predefined color points in the NVM) and intensities of the LIN LED Driver IC slaves in the network. This frame uses enhanced checksum.

Table 7 Frame MSTR_L1_P00

Frame Symbol	MSTR_L1_P00																							
Data field within frame	data byte 1								data byte 2								data byte 3							
Data bit within field	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Information field symbol (signal)	Location_ID								Color_Trans_Time0	Update_Color	Color				Color_Transistion_Enable	Intensity_Dimming_Enable[1]	Update_Intensity		Color_Trans_Time2	Color_Trans_Time1	Global_Intensity[2]			
Bit within information field (signal)	7	6	5	4	3	2	1	0	0	0	3	2	1	0	0	0	1	0	2	1	3	2	1	0

1) Must not be changed during activated outputs or intensities > 0.

2) A changing of the intensity during an active dimming process leads to different dimming times than programmed.

Table 8 Information Fields of Frame MSTR_L1_P00

Symbol (signal)	Bits	Value	Description
Global_Intensity	3:0	0:0xF	Global output intensity setting between 0 (OFF) and 0xF (100%), see Chapter 7.1.1 for details. Default value is 0.
Color_Trans_Time1	4	0:1	Color transitioning time bit 1
Color_Trans_Time2	5	0:1	Color transitioning time bit 2 (MSB)
Update_Intensity	7:6	0	Update intensity to new value transmitted in this frame.
		1	Store intensity value transmitted in this frame, but the intensity at the outputs it not changed.
		2	Update intensity to stored value, ignore intensity data transmitted in this frame.
		3	Ignore intensity data transmitted in this frame, the intensity at the outputs it not changed.
Intensity_Dimming_Enable	0	0	After frame transmission LIN LED Driver IC switches to new intensity without dimming.
		1	After frame transmission LIN LED Driver IC ramps to new intensity within dim-up/dim-down time.

Table 8 Information Fields of Frame MSTR_L1_P00

Symbol (signal)	Bits	Value	Description
Color_Transition_ Enable	1	0	After frame transmission LIN LED Driver IC switches to new color without smooth transitioning.
		1	After frame transmission LIN LED Driver IC changes to new color within selected color transition time.
Color	5:2	0:0xF	Set of output intensities as defined in the NVM. If a value of 0xY is written into the frame, the color point with the NVM address 0x(Y+1) is used.
Update_Color	6	0	Ignore defined color data in Color-Bits, do not change color.
		1	Update color (set of intensities) to new set of output intensities according to data transmitted in this frame.
Color_Trans_Time0	7	0:1	Color transitioning time bit 0 (LSB)
Location _ID	7:0	0:0xFF	Location_ID defines which individual slave or zone of slaves is addressed with this command, according to **Table 6**.

6.6.2 MSTR_L1_P01 Message Frame (LED calibration, direct intensity access)

This command allows to set the absolute intensities of the three output channels without using the sets of output currents stored in the NVM. This frame uses enhanced checksum. It can be used for two different applications:

- After assembly on a LIN LED slave PCB, the LIN LED driver IC needs to be calibrated according to the brightness and wavelength characteristics of the individual LED. During this calibration process an individual set of output intensities is required. This individual set of output intensities can be applied by using the MSTR_L1_P01 message frame.
- For setting individual colors or intensities (independent of the 16 calibrated sets of output intensities in the NVM) the MSTR_L1_P01 message frame can be used as well.

After successful transmission of this frame, the output intensities are changed according to the transmitted data. The change (parameters for color transitioning) is done according to the settings of the MSTR_L1_P00 message frame. This means that any previously programmed color setting by MSTR_L1_P00 frame transmission is overwritten. This new set of output intensities remains valid until either a new MSTR_L1_P01 frame is transmitted, or a new MSTR_L1_P00 frame with Update_Color = 1 is transmitted.

Note: For an output activation by the MSTR_L1_P01 message frame without using the calibrated NVM intensity sets the global intensity setting in the MSTR_L1_P00 message frame needs to be set after the MSTR_L1_P01 message frame. The update color bit must be 0.

Table 9 Frame MSTR_L1_P01

Frame Symbol	MSTR_L1_P01															
Data field within frame	data byte 1								data byte 2							
Data bit within field	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Information field symbol (signal)	Location_ID								Intensity_Out1_Command							
Bit within information field (signal)	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

MSTR_L1_P01															
data byte 3								data byte 4							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Intensity_Out2_Command								Intensity_Out3_Command							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Table 10 Information Fields of Frame MSTR_L1_P01

Symbol	Bits	Value	Description
Intensity_Out3_Command	7:0	0:0xFF	Set output intensity of Out3 to this value.
Intensity_Out2_Command	7:0	0:0xFF	Set output intensity of Out2 to this value.
Intensity_Out1_Command	7:0	0:0xFF	Set output intensity of Out1 to this value.
Location_ID	7:0	0:0xFF	Location_ID defines, which individual slave or zone of slaves is addressed with this command according to **Table 6**.

6.6.3 MSTR_L1_P02 Message Frame (Write Non-Volatile Memory)

This message is used to program the on-chip non-volatile memory (NVM), see **Chapter 8** for details on the NVM itself. This frame works at an increased battery voltage $V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$ (**Pos. 8.5.1** and **Pos. 8.5.2**) and is intended for usage during assembly and programming of the LED slave hardware prior to integration into a LIN network. This frame should not be used by the LIN master in the actual network application. This frame uses enhanced checksum.

The non volatile memory map and a programming example can be found in **Chapter 8.1**.

Note: In case this frame is received, while the LIN LED Driver IC is not in programming mode, this frame is ignored (no diagnostic error is generated).

Table 11 Frame MSTR_L1_P02

Frame Symbol	MSTR_L1_P02															
Data field within frame	data byte 1								data byte 2							
Data bit within field	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Information field symbol (signal)	Erase_NVM	Always set to 0	NVM_Address						Program_Data1							
Bit within information field (signal)	0	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0

MSTR_L1_P02															
data byte 3								data byte 4							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Program_Data2								Program_Data3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Table 12 Information Fields of Frame MSTR_L1_P02

Symbol	Bits	Value	Description
Program_Data3	7:0	0:0xFF	This data is written into the addressed register, bits 16-23
Program_Data2	7:0	0:0xFF	This data is written into the addressed register, bits 8-15
Program_Data1	7:0	0:0xFF	This data is written into the addressed register, bits 0-7
NVM_Address	5:0	0:0x10	Address of NVM register that is to be programmed or erased. Bit 5 not used, reserved for future extensions
Always set to 0	6	0	Always set this bit to 0.
Erase_NVM	7	0	The data transmitted in this frame is written into the addressed register
		1	The addressed register is erased first, then the data transmitted in this frame is written into it.

6.6.4 MSTR_L1_P03 Message Frame (Set custom dim-times)

This command allows to program custom dim-times for the dimming engine described in **Chapter 7** and the temperature prewarning threshold can be selected. As soon as this frame was successfully transmitted, the addressed slave(s) uses the new dim-times, starting with the next intensity change event. If the application uses the default settings of nominal 0.7 sec. for dimming up and 1.7 sec. for dimming down, this message is not needed. After a reset, the dim-times are reset to these nominal values. This frame uses enhanced checksum.

The detailed timings for the dimming is specified in **Chapter 7.2.1**.

Table 13 Frame MSTR_L1_P03

Frame Symbol	MSTR_L1_P03															
Data field within frame	data byte 1								data byte 2							
Data bit within field	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Information field symbol (signal)	Location_ID								Temp. Prewarning		Always set to 0		Dim_Up_Time[1]			
Bit within information field (signal)	7	6	5	4	3	2	1	0	1	0	1	0	3	2	1	0

1) A changing of the dimming times during an active dimming process leads to different dimming times than programmed.

MSTR_L1_P03							
data byte 3							
7	6	5	4	3	2	1	0
Always set to 0				Dim_Down_Time[1]			
3	2	1	0	3	2	1	0

Table 14 Information Fields of Frame MSTR_L1_P03

Symbol	Bits	Value	Description
Dim_Down_Time	3:0	0:0xF	New time setting for dimming down the LED intensity.
Always set to 0	7:4	0	Always set those bits to 0.
Dim_Up_Time	3:0	0:0xF	New time setting for dimming up the LED intensity.
Always set to 0	5:4	0	Always set those bits to 0.

Table 14 Information Fields of Frame MSTR_L1_P03

Symbol	Bits	Value	Description
Temp. Prewarning	7:6	0	Sets the temperature prewarning to T_j = 140 °C (default)
		1	Sets the temperature prewarning to T_j = 120 °C
		2	Sets the temperature prewarning to T_j = 160 °C
		3	Temperature prewarning deactivated
Location_ID	7:0	0:0xFF	Location_ID defines, which individual slave or zone of slaves is addressed with this command according to **Table 6**

6.6.5 MSTR_L1_P04 and LED_L1_P02 Message Frame (Go to sleep command)

The message frame MSTR_L1_P04 has a fixed frame ID 0x3C and is used as go to sleep command, read by identifier command or assign frame range command. The message frame LED_L1_P02 has a fixed frame ID 0x3D and is used as read by identifier command or assign frame range response. The frame length is fixed to 8 byte, the data content is defined by the LIN 2.1 standard. This frame uses classic checksum, which contains the inverted eight bit sum with carry over all data bytes (but not the protected identifier). The data byte 1 for the go to sleep command has to be 0, all other bytes have to be 0xFF. As far as the read by identifier command and the assign frame range command use the same frame IDs 0x3C (and 0x3D for the response), the command differentiation is done by the PCI (Protocol Control Information) and SID (Service Identifier).

The LIN LED Driver IC supports node configuration and identification as described in the LIN 2.1 standard. Only the mandatory services “Read by Identifier” and “Assign frame identifier range” are implemented in the LIN LED Driver IC.

6.6.5.1 Go to sleep command

Table 15 Frame MSTR_L1_P04

Frame Symbol	MSTR_L1_P04							
Data field within frame	data1	data2	data3	data4	data5	data6	data7	data8
Go to sleep	0	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

6.6.5.2 Read by Identifier

This command allows the readout of the supplier identity and product identity, which are needed to correctly respond to a read by identifier request:

Supplier ID = 0x001C

Function ID = 0x6013

Variant ID = 0x00

If a wrong request command is sent, no device reaction and no response is sent.

Table 16 Read by identifier request

Frame Symbol	MSTR_L1_P04 (0x3C)							
Data field within frame	NAD	PCI	SID	D1	D2	D3	D4	D5
Read by identifier request	frame_ID_slave	0x06	0xB2	0x00	0xFF	0x7F	0xFF	0xFF

Table 17 Read by identifier response

Frame Symbol	LED_L1_P02 (0x3D)							
Data field within frame	NAD	PCI	RSID	D1	D2	D3	D4	D5
Read by identifier response	frame_ID _slave	0x06	0xF2	Supplier ID LSB	Supplier ID MSB	Function ID LSB	Function ID MSB	Variant ID

Example: LIN LED Driver IC with frame_ID_slave of 0x08 shall send its identity

LIN master send: 0x3c 0x08 0x06 0xB2 0x00 0xFF 0x7F 0xFF 0xFF

LIN master send: 0x3d slave response: 0x08 0x06 0xF2 0x1C 0x00 0x13 0x60 0x00

6.6.5.3 Assign Frame Identifier range

This command enables a volatile shift of the frame IDs, which is stored in NVM. Please note that only the Master Frame ID MSTR_L1_P00 and the Slave Frame ID LED_L1_P00 can be reassigned. All other Frame IDs change according to **Table 3**. Frame ID MSTR_L1_P00 is located on start index 0, Frame ID LED_L1_P00 is located on start index 4. Data byte D2 provides the New Frame ID in protected identifier format. The start index defines the starting ID, which is reassigned.

If a wrong request command is sent, no device reaction and no answer is sent.

Note: The reconfiguration done during "assign frame identifier range" is only stored in the RAM registers of the LIN LED Driver IC. The information is lost after a power up reset or a go to sleep command, and the IDs according to the NVM-setting are valid again.

Table 18 Assign Frame identifier range request

Frame Symbol	MSTR_L1_P04 (0x3C)							
Data field within frame	NAD	PCI	SID	D1	D2	D3	D4	D5
Assign Frame identifier range request	frame_ID _slave	0x06	0xB7	start index	New frame_ID	0xFF	0xFF	0xFF

Table 19 Assign Frame identifier range response

Frame Symbol	LED_L1_P02 (0x3D)							
Data field within frame	NAD	PCI	RSID	not used				
Assign Frame identifier range response	frame_ID _slave	0x01	0xF7	0xFF	0xFF	0xFF	0xFF	0xFF

Example 1: LIN LED Driver IC with frame_ID_slave of 0x08 shall get the Master Frame ID (MSTR_L1_P00) of 0x28 (protected ID 0xA8 (protected ID includes the frame ID and the parity bits))

LIN master send: 0x3c 0x08 0x06 0xB7 0x00 0xA8 0xFF 0xFF 0xFF

LIN master send: 0x3d slave response: 0x08 0x01 0xF7 0xFF 0xFF 0xFF 0xFF 0xFF

Example 2: LIN LED Driver IC with fame_ID_slave of 0x08 shall get the Slave Frame ID (LED_L1_P00) of 0x2C (protected ID 0xEC)

LIN master send: 0x3c 0x08 0x06 0xB7 0x04 0xEC 0xFF 0xFF 0xFF

LIN master send: 0x3d slave response: 0x08 0x01 0xF7 0xFF 0xFF 0xFF 0xFF 0xFF

6.6.6 LED_L1_P00 Message Frame (Diagnostic Response)

With this frame, the master can request diagnostic information from each individual LIN LED Driver IC slave in the network. The individual slave is addressed by the frame-IDs as defined in **Table 4**. This frame uses enhanced checksum. The diagnostic information is structured into three information fields:

- A 5-bit Application Information (ApInfo0 - ApInfo3) field. The LIN LED Driver IC provides information about hardware failures detected by the embedded protection and diagnostic functions.
- A 3-bit LINStatus field. This is a LIN standard diagnostic reply containing information about the LIN link. In case of an error, the error is reset by reading out the error bit. In case of multiple errors, the error with the highest priority is set first and is cleared after readout. At the next readout of the LINStatusfield the next error is shown.
- The 8-bit location identifier, which has been programmed into the LIN LED Driver IC NVM.

Table 20 Frame LED_L1_P00

Frame Symbol	LED_L1_P00															
Data field within frame	data byte 1								data byte 2							
Data bit within field	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Information field symbol (signal)	LIN_Status			ApInfo3	ApInfo2		ApInfo1	ApInfo0	LED_Location_ID							
Bit within information field (signal)	2	1	0	0	1	0	0	0	7	6	5	4	3	2	1	0

Table 21 Information Fields of Frame LED_L1_P00

Symbol	Bits	Value	Description
LED_Location_ID	7:0	0:0xFF	The LIN LED Driver IC sends its Location_ID back to the master
ApInfo0	0	0	No fault detected by LIN LED Driver IC
		1	Temperature warning
ApInfo1	1	0	Not used, always low
ApInfo2	3:2	0	No fault detected by LIN LED Driver IC
		1	Not used
		2	The LIN LED Driver IC is in over temperature condition, outputs switched off
		3	NVM programming error
ApInfo3	4	0	No fault detected by LIN LED Driver IC
		1	LIN LED Driver IC was not configured, LED_Location_ID is at default value
LIN_Status	7:5	0	No Fault Detected - The last frame transmission was successful
		1	Reset - the LIN LED Driver IC was reset since the last transmission (i.e. this is the first LIN communication after a reset)
		2	Reserved - not used by LIN LED Driver IC
		3	Reserved - not used by LIN LED Driver IC
		4	Data Error
		5	Checksum Error - The last frame transmission had a checksum error and was ignored
		6	Byte Field Framing Error
		7	ID Parity Error

6.6.7 LED_L1_P01 Message Frame (Read NVM content)

With this frame, the master can request the content of the embedded NVM. This frame uses enhanced checksum. It can be used for:

- Confirmation of successful NVM programming
- The master node acquires LED calibration data represented in the NVM, e.g. for advanced color mixing

The frame contains only the data of one NVM register. To be able to access the entire NVM content, an internal counter is implemented in the LIN LED Driver IC that runs through all NVM register addresses. This counter is incremented by one after each successful transmission of the LED_L1_P01 frame. After a reset, the counter starts at 0x00. The transmission of a MSTR_L1_P02 frame (Write NVM) sets the counter to the address that was programmed last. This enables programming verification by sending LED_L1_P01 directly after MSTR_L1_P02.

Note: Addition information on the NVM verification at ***Chapter 8.4****.*

Table 22 Frame LED_L1_P01

Frame Symbol	**LED_L1_P01**															
Data field within frame	data byte 1								data byte 2							
Data bit within field	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Information field symbol (signal)	LIN_Status			ApInfo3	ApInfo2		ApInfo1	ApInfo0	Unused		NVM_Address					
Bit within information field (signal)	2	1	0	0	1	0	0	0	1	0	5	4	3	2	1	0

LED_L1_P01																								
data byte 3								data byte 4								data byte 5								
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Content_Data1								Content_Data2								Content_Data3							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Table 23 Information Fields of Frame LED_L1_P01

Symbol	**Bits**	**Value**	**Description**
Content_Data3	7:0	0:0xFF	Data content of bit 16-23 of the NVM register with the address NVM_Address
Content_Data2	7:0	0:0xFF	Data content of bit 8-15 of the NVM register with the address NVM_Address
Content_Data1	7:0	0:0xFF	Data content of bit 0-7 of the NVM register with the address NVM_Address
NVM_Address	6	0:0x10	Address of NVM register that is reported back to the master in this frame (counter), Bit 5 unused
Unused	7:6	-	Unused bits
ApInfo	4:0	-	See **Table 21**
LIN_Status	7:5	-	See **Table 21**

7 Intensity Generation Unit

Note: In the following chapters the naming OUT1, OUT2, OUT3 is used as for the 3 output channels, where OUT1 represents PWR1+SENSE1, OUT2 represents PWR2/SENSE2 and OUT3 represents PWR3/SENSE3.

The LIN LED Driver IC has an integrated Intensity Generation Unit that manages the intensities (i.e. average output currents) of the three LED driver outputs OUT1, OUT2 and OUT3.

One of the main applications is to drive the three channels of an RGB (red, green, blue) LED. Therefore, special methods to manage color mixing are implemented.

The intensity generation unit fulfills the following major functions:

- Multiply set of output intensities (average current stored in NVM) and global intensity to calculate the desired total average output current per output channel (0 - 100% of constant current power stage)
- Generate a time-dependent pulse-stream to represent an average ON-time equal to the desired output intensity
- Manage theater dimming (time-dependent transition between intensities)

Figure 7 shows a schematic block diagram of the intensity generation unit. The user selects the desired set of output intensities (e.g. a specific RGB color mix) and intensity by LIN communication. The LIN LED Driver IC transforms this data into a physical output current.

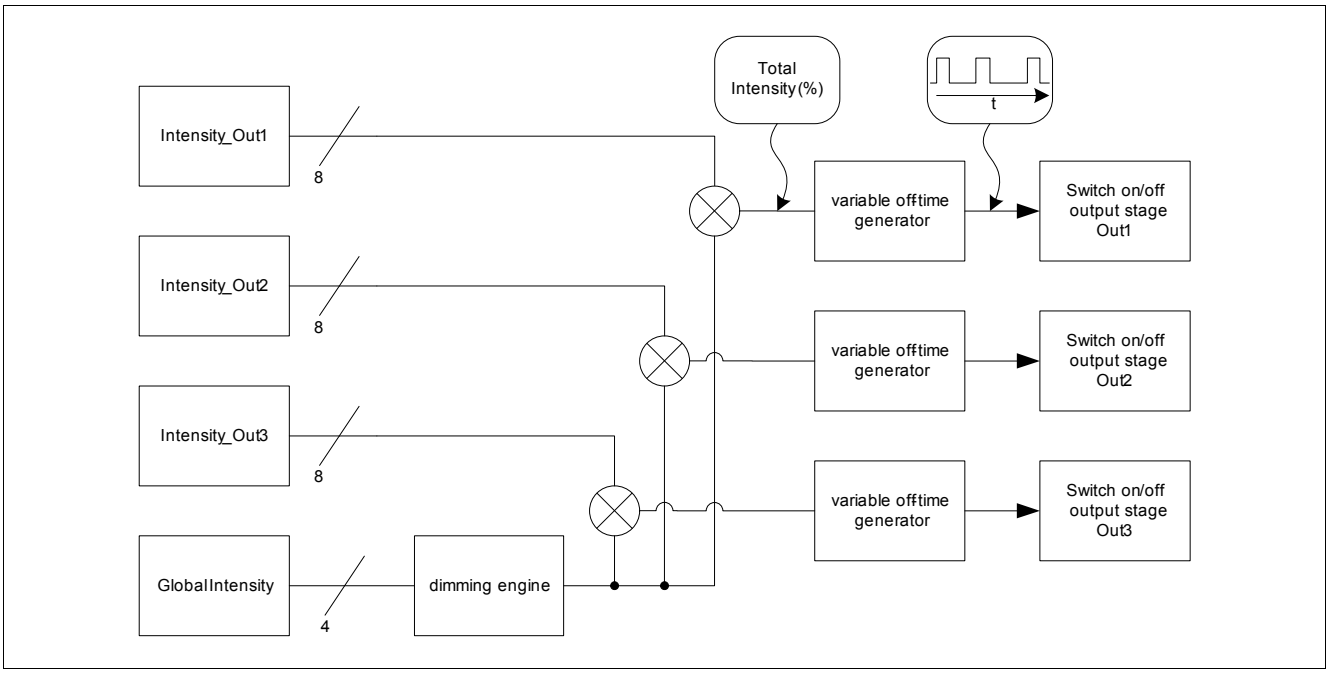


Figure 7 Intensity Generation Unit

7.1 Intensity Calculation

The intensity generation unit processes data from internal registers. These register values are associated with relative intensities, which are defined by the intensity setting either stored in the NVM or directly programmed via the direct intensity setting.

7.1.1 Global Intensity

The intensity setting of a predefined NVM color point (set of three intensity values) allows a change of the intensity to 14 different values as shown in **Table 24**, which means in case of using an RGB-LED that colors can be dimmed

from 0% to 100%. The desired intensity is defined by the LIN command MSTR_L1_P00. The default value after reset is 0. These 14 intensities are evenly distributed between 0% and 100%.

Table 24 Intensity Settings

Intensity Register	Global Intensity
0x0	0 (Outputs OFF)
0x1	1.56%
0x2	2.34%
0x3	3.12%
0x4	4.69%
0x5	6.25%
0x6	9.38%

Intensity Register	Global Intensity
0x7	12.5%
0x8	18.7%
0x9	25%
0xA	37.5%
0xB	50%
0xC	75%
0xD, 0xE, 0xF	100%

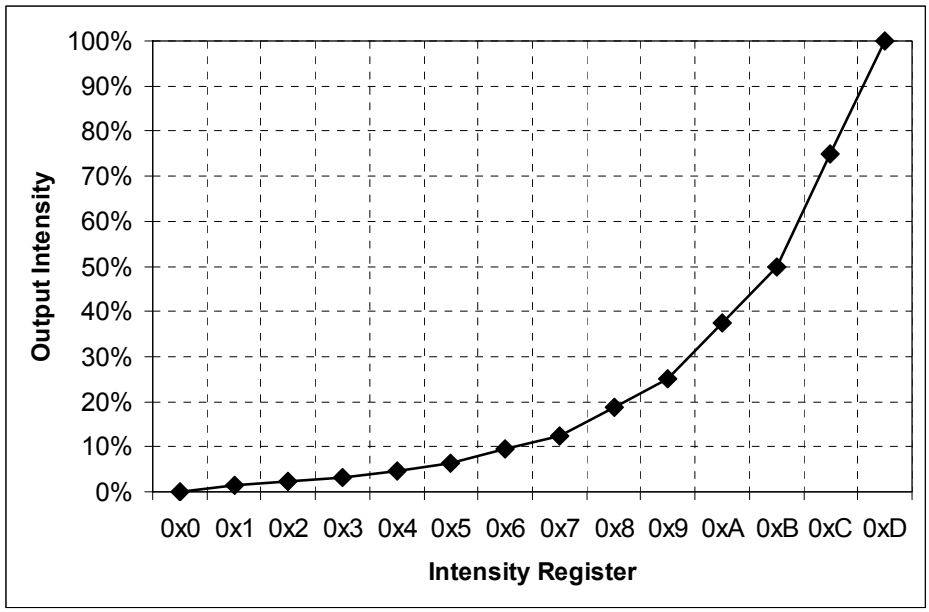


Figure 8 Available Intensities

Note: The default intensity after startup is 0, so to activate the outputs of the device the intensity has to be changed from it's default value!

7.1.2 Sets of Output Intensities

The LIN LED Driver IC contains 16 8-bit NVM registers for each of the three outputs (i.e. 48 registers, each 8 bit wide). Each triplet of registers contains one set of output intensities (from 0 to 100%). In case an RGB-LED is driven, each set represents one color point.

Once the NVM has been programmed, the user can select the desired set of output intensities by the 4-bit color signal in the LIN command MSTR_L1_P00. The default color after startup is 0. The according set of output intensities is read from the NVM register and written into the Intensity_Outx (Intensity_Out1, Intensity_Out2, Intensity_Out3) registers. Those registers are the input for the intensity generation unit. The Intensity_Outx registers can be overwritten by the user with the LIN message MSTR_L1_P01 to generate arbitrary sets of output

intensities, independent of the NVM register content. The relative intensity is the numeric value of the Intensity_Outx register scaled to 1:

$$\text{Relative OUTx Intensity} = \frac{\text{Intensity\_OUTx}}{0xFF} \quad (1)$$

For example, an Intensity_Out1 value of 0x9A is equal to:

$$\text{Relative OUT1 Intensity} = \frac{0x9A}{0xFF} = \frac{154}{255} = 60.4\% \quad (2)$$

7.1.3 Total Intensity

The desired total intensity is the product of the intensity values and the global intensity setting:

$$\text{Total OUTx Intensity} = \text{Global Intensity} \cdot \text{Relative OUTx Intensity} \quad (3)$$

This shall be illustrated by the following example:

Table 25 Total Intensity Calculation Example

Channel	set of output intensities		Intensity		Total Intensity	Output current of power-stage (set by current_adjust register)	Effective average Output current
	Intensity_ Outx register	Relative Outx Intensity	Global Intensity register	Relative Intensity			
Out1 (red)	0xE6	90%	0x0B	50%	45%	24mA	10.8mA
Out2 (green)	0x33	20%			10%		2.4mA
Out3 (blue)	0x0	0%			0		OFF

7.2 Dimming

The LIN LED Driver IC has a dimming engine implemented, which allows a smooth transition between any of the 14 available global intensity settings, including 0 (all outputs OFF). The duration for the dimming is always according to the programmed value (16 different dim times can be selected according to **Table 26**), independent of the starting and ending intensity. The default values are set to nominal 0.7 s for dimming up and 1.7 s for dimming down. The dimming is realized with a 12 bit resolution (12 bit for the entire range 0 to 100% intensity). For details on the dimming time accuracy please refer to **Pos. 7.4.1**. The exponential spacing between the available intensities provides an exponential decay of LED current over time when the start- and end-intensity span a wider dynamic range.

Note: The selection, if the dimming by the bit `ramp-intensity` *in the master published frame MSTR_L1_P00 according to* ***Table 7*** *should be activated or not, has to be done during disabled output stages (i.e. intensity setting is 0). A change of the intensity settings (bit* `intensity` *in the master published frame MSTR_L1_P00) or a change of the dimming times (bit* `dim_down_time` *and* `dim_up_time` *in the master published frame MSTR_L1_P03) during a running dimming process leads to different dimming times than programmed.*

7.2.1 Custom Dim Times

The default dim-up and dim-down times (0.7 and 1.7 s) can be changed by the master published frame MSTR_L1_P03 in the application. **Table 26** specifies the nominal dim-times associated with the Dim_Up_Time and Dim_Down_Time settings. As soon as this frame is successfully transmitted, the addressed slave(s) will use the new dim-times, starting with the next intensity change event. After Power-ON Reset, the dim-times are reset to the default values.

Note: A change of the dimming times (bit `dim_down_time` *and* `dim_up_time` *in the master published frame MSTR_L1_P03) during a running dimming process leads different dimming times than programmed.*

Table 26 Timing Characteristics: Dim-time decoding

Dim_Up_Time Register	Nominal dim up time t_{dim} [s]
0	0.28
1	0.43
2	0.57
3 (default)	0.71 (default)
4	0.85
5	1.00
6	1.28
7	1.43
8	1.71
9	1.85
A	2.00
B	2.28
C	2.56
D	3.00
E	3.56
F	4.56

Dim_Down_Time Register	Nominal dim down time t_{dim} [s]
0	0.28
1	0.43
2	0.57
3	0.71
4	0.85
5	1.00
6	1.28
7	1.43
8 (default)	1.71 (default)
9	1.85
A	2.00
B	2.28
C	2.56
D	3.00
E	3.56
F	4.56

The dim-times are derived from the internal oscillator, the nominal values given in this table refer to its nominal frequency. The accuracy of the dim times is specified in **Chapter 7.3**.

7.2.2 Color Transitioning

The device offers a function for smooth color transitions between the color points stored in the NVM or programmed via the direct intensity access by the master published frame MSTR_L1_P01 with a resolution of 10 bit. The nominal time for the color transitions is defined in **Table 27** and can be programmed by the master published frame MSTR_L1_P00.

Table 27 Timing Characteristics: Color transition time decoding

Color_Trans_Time Register	Nominal transition time $t_{trans(nom)}$ [s]
0	0.05
1	0.08
2	0.13
3 (default)	0.21 (default)
4	0.34
5	0.55
6	0.89
7	1.45

The final color transitioning time $t_{trans(fin)}$ depends on the requested color change and is calculated according to **Equation (4)**, where OUT1_A represents the decimal value of the channel 1's 8 bit starting intensity. OUT1_B

represents the decimal value of the finally desired intensity. The same is valid for the two other outputs OUT2 and OUT3.

$$t_{trans(fin)} = t_{trans(nom)} \cdot \frac{\max\{|OUT1\_B - OUT1\_A|, |OUT2\_B - OUT2\_A|, |OUT3\_B - OUT3\_A|\}}{2^8 - 1} \quad (4)$$

Example:

OUT1_A = 0x1E = 30, OUT1_B = 0xFF = 255

OUT2_A = 0x64 = 100, OUT2_B = 0x2C = 44

OUT3_A = 0x08 = 8, OUT3_B = 0x5C = 92

`Color_Trans_Time` = 110_b, which means a nominal transition time of 0.55 s.

The resulting transition time is:

$$t_{trans(fin)} = 0.55s \cdot \frac{\max\{|255 - 30|, |44 - 100|, |92 - 8|\}}{2^8 - 1} = 0.49s \quad (5)$$

7.3 Variable Off-time Generator

The internal intensity calculation and the dimming engine results in a desired total intensity between 0-100%. In the variable off-time generator block the value is transformed into a stream of on/off pulses, which controls the according power-stage. The pulse-stream is generated accordingly to fulfill:

- The average on-time is equal to the programmed intensity (i.e. the average output current is equal to the desired intensity multiplied with the current source output value (which is defined by the current_adjust register)).
- A high switching frequency to avoid any LED flickering effects.

7.4 Electrical Characteristics Intensity Generation Unit

Electrical Characteristics: Intensity Generation Unit

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.4.1	Dimming time accuracy	t_{dim} / $t_{dim(nom)}$	0.97 0.95	1 1	1.03 1.05		1) T_j = 25 °C 1) T_j = 20...105 °C
7.4.2	Color transitioning time accuracy	t_{trans} / $t_{trans(nom)}$	0.97 0.95	1 1	1.03 1.05		1) T_j = 25 °C 1) T_j = 20...105 °C

1) Not subject to production test, specified by design

8 Non-Volatile Memory

The LIN LED Driver IC offers an integrated non-volatile memory (NVM) to store 16 sets of output currents for color calibration, a slave NAD and master NAD to define LIN frame-IDs and a location identifier.

8.1 Non Volatile Memory Map

Table 28 shows the mapping of the NVM registers. The NVM register address is the one used in the MSTR_L1_P02 and LED_L1_P01 LIN message frames (see **Chapter 6.6.3** and **Chapter 6.6.7** for details).

Registers 0x1 to 0x10 contain the 16 sets of output intensities. They can be used for color mixing of 16 pre-defined RGB colors, which could be calibrated e.g. during the RGB module manufacturing. Register 0x0 contains the LIN frame IDs for the publisher and subscriber messages as described in **Chapter 6.5.2** and **Chapter 6.5.3** and the location identifier explained in **Chapter 6.5.4**.

The registers' default values are shown in **Chapter 8.3** and **Table 29**.

Note: frame_ID_slave and frame_ID_mstr field contain the unprotected identifier. The LIN *LED Driver IC calculates the protected ID internally.*

Table 28 NVM register mapping

Register Address	bit within register																							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x10	OUT3_15								OUT2_15								OUT1_15							
0xF	OUT3_14								OUT2_14								OUT1_14							
0xE	OUT3_13								OUT2_13								OUT1_13							
0xD	OUT3_12								OUT2_12								OUT1_12							
0xC	OUT3_11								OUT2_11								OUT1_11							
0xB	OUT3_10								OUT2_10								OUT1_10							
0xA	OUT3_9								OUT2_9								OUT1_9							
0x9	OUT3_8								OUT2_8								OUT1_8							
0x8	OUT3_7								OUT2_7								OUT1_7							
0x7	OUT3_6								OUT2_6								OUT1_6							
0x6	OUT3_5								OUT2_5								OUT1_5							
0x5	OUT3_4								OUT2_4								OUT1_4							
0x4	OUT3_3								OUT2_3								OUT1_3							
0x3	OUT3_2								OUT2_2								OUT1_2							
0x2	OUT3_1								OUT2_1								OUT1_1							
0x1	OUT3_0								OUT2_0								OUT1_0							
0x0	Always set to 1	Always set to 0	Current_adjust[1]		Location_ID								frame_ID_mstr						frame_ID_slave					
Register Address	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

1) Please refer to **Table 31**

One example for the NVM register 0x0 for an initial device with default programming:

The default values are:

Frame_ID_master = 0x00

Frame_ID_slave = 0x34

Location_ID = 0xFF

Current_adjust = 0x1 = 240 mV

Table 29 shows the according default register content:

Table 29 NVM register 0x0 default values

Register Address	bit within register																							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x0	1	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	0	1	0	0

Another example with values to be programmed into the NVM register 0x0:

Frame_ID_master = 0x2A

Frame_ID_slave = 0x14

Location_ID = 0x84

Current_adjust = 0x1 = 240 mV

Programming frame: 02 80 94 4A 98

The according register content is shown in **Table 30**:

Table 30 NVM register 0x0 example

Register Address	bit within register																							
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x0	1	0	0	1	1	0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	1	0	0

8.2 NVM Programming

To program the NVM, the LIN LED Driver IC needs to be set to NVM programming mode. The NVM programming mode is activated by applying a supply voltage V_S within the programming voltage range $V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$ (**Pos. 8.5.1** and **Pos. 8.5.2**) for longer than the programming settle time $t_{PGM(s)}$ (**Pos. 8.5.3**). This also enables the LIN-transceiver flash-mode for higher speed data transmission. The maximum speed on the LIN-bus is increased to f_{flash} (**Pos. 6.3.24**). Once the programming mode is entered (V_S within $V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$), the NVM-registers can be programmed by the MSTR_L1_P02 frame. In the NVM programming mode master published frame-IDs have to use 2 or more stop-bits. The LIN LED Driver IC answers for slave frame-IDs with 1 stop-bit.

After a successful transmission of a programming frame, the LIN LED Driver IC programs the data transmitted into the NVM address transmitted. The programming requires a time of $t_{PGM(d)}$. The next programming is allowed only after the expired delay time $t_{PGM(d)}$ (**Pos. 8.5.4**).

Note: A high supply voltage spike shorter than $t_{PGM(s)}$ does not cause an activation of the programming mode. Only a supply voltage V_S within the range $V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$ applied for a time longer than $t_{PGM(s)}$ and a correct NVM programming command allows an NVM programming.

8.2.1 NVM Programming Procedure

The following NVM procedure should be used:

1. Apply a supply voltage V_S within $V_{S(PGM,L)} < V_S < V_{S(PGM,U)}$ (**Pos. 8.5.1** and **Pos. 8.5.2**)
2. Keep supply voltage stable at the programming voltage $V_{S(PGM)}$ longer than $t_{PGM(s)}$ (**Pos. 8.5.3**)
3. Program NVM-register by the MSTR_L1_P02 frame
4. Wait the programming delay time $t_{PGM(d)}$ (**Pos. 8.5.4**)
5. Program next NVM-register
6. ...
7. Reduce supply voltage below power-up voltage $V_{S(PU)}$ to reset the LIN LED Driver IC

8.3 NVM Erase

The NVM is realized as an EEPROM, which needs to be erased before re-programming. The LIN LED Driver IC supports only erasing of complete registers. It is shipped with erased registers 0x01 to 0x10. The default value of those registers is 0xFFFFFF. Therefore, it is not needed to erase the NVM before the first NVM programming. The register 0x00 contains the default values for frame_ID_slave (default value 0x34), frame_ID_master (default value 0x00), and location_ID (default value 0xFF) and current_adjust (default value 0x1). This register needs to be erased before the first programming. If the IC needs to be re-programmed, a MSTR_L1_P02 frame with the Erase_NVM bit set to 1 (see **Chapter 6.6.3**) has to be sent. After this command a wait time of $t_{ERASE(d)}$ (**Pos. 8.5.5**) has to elapse before programming the next frame.

To ensure high quality data retention, the user has to limit the total number of erase and re-programming cycles to a maximum of N_{PRG} (**Pos. 8.5.6**) (i.e. N_{PRG} erase and N_{PRG} programming events, or sending the MSTR_L1_P02 frame with Erase_NVM = 1 less than N_{PRG}).

8.4 NVM Verification

It is recommended to verify the the successful NVM programming. After $t_{PGM(d)}$ is elapsed, a read back of the NVM can be performed by the LIN frame LED_L1_P01 as described in **Chapter 6.6.7**. This frame also is available in programming mode. The flash-mode of the LIN interface (faster data transfer, maximum speed on the LIN-bus increased to f_{flash} (**Pos. 6.3.24**)) can be used to reduce the time of this verification. The read address counter is always set to the last register, which was write-accessed. This means a read command (LED_L1_P01) sent directly after a write command (MSTR_L1_P02) always provides verification of the last write process. To be able to access the entire NVM content, an internal counter is implemented in the LIN LED Driver IC, which runs through all NVM register addresses. This counter is incremented by one after each successful transmission of the LED_L1_P01 frame. After a reset, the counter starts at 0x00. All NVM registers (0x00 to 0x10) can be read out by

sequential sending of the NVM read command (LED_L1_P01). Furthermore, additional 4 NVM registers (0x11 to 0x14) are implemented in the NVM. Those registers are also shown during the readout of the NVM. They are for internal purposes and read only. After reading the register 0x14 the next readout register in a sequential NVM readout loop is 0x00. **Figure 9** and **Figure 10** show the recommended programming sequence.

8.4.1 NVM Error

The LIN LED Driver IC detects two errors during NVM programming:

- The supply voltage is not within the programming range during the programming cycle.
- A new NVM write command was received before the active write cycle was finished.
- A program address outside the allowed address range 0x00...0x10 is used for the NVM write command.

In both cases, the NVM programming error is set in the ApInfo field of the diagnostic response (LED_L1_P00 frame). It is cleared by a power-on reset or by a successful transmission of the diagnostic byte (i.e. successful transmission of LED_L1_P00 or LED_L1_P01 frame). If an NVMError = 1 message is received during NVM verification, the according register must be erased and re-programmed, even if the data content reported back in the LED_L1_P01 frame was correct.

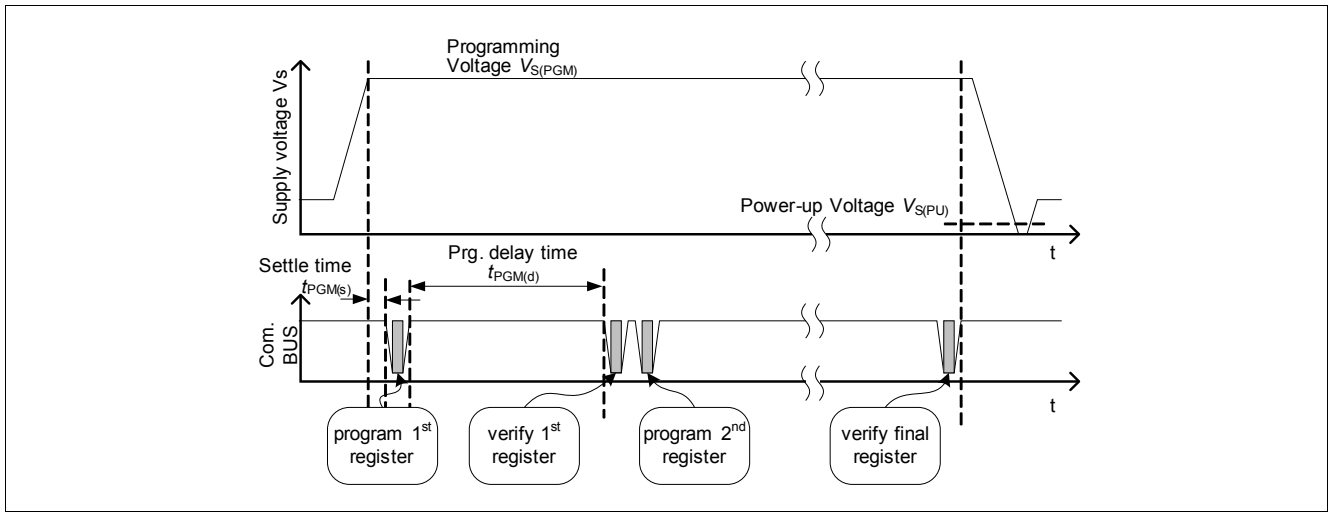


Figure 9 NVM programming sequence without erase

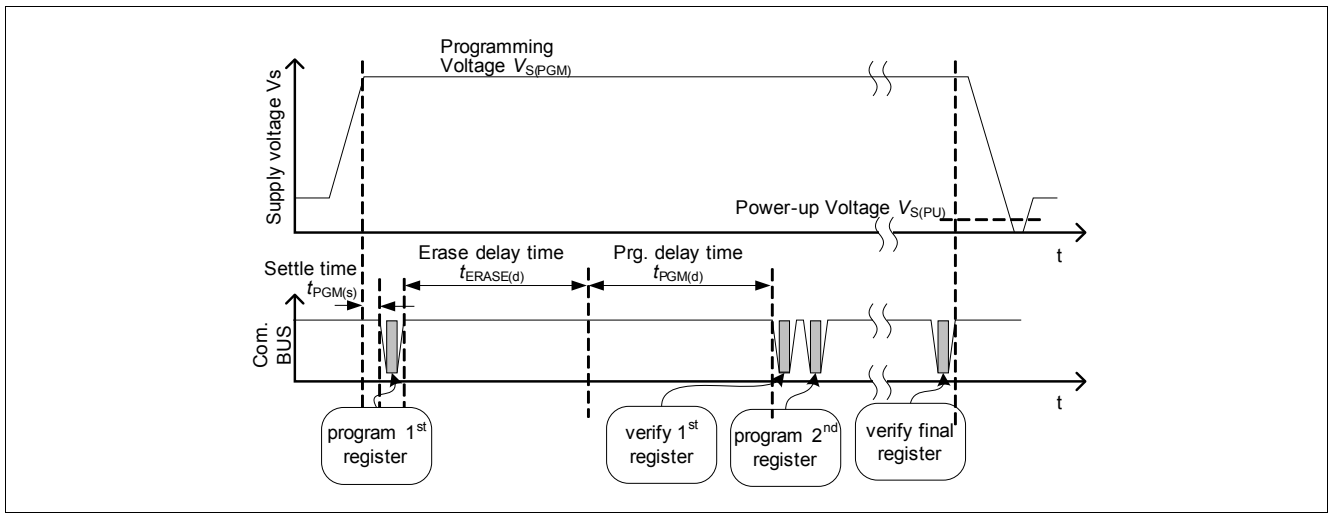


Figure 10 NVM programming sequence with erase

8.5 Electrical Characteristics NVM

Electrical Characteristics: NVM

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.5.1	Lower limit programming voltage	$V_{S(PGM,L)}$	34	–	38.2	V	T_j = 25 °C
8.5.2	Upper limit programming voltage	$V_{S(PGM,U)}$	38.8	–	–	V	1) T_j = 25 °C
8.5.3	Programming mode settle time	$t_{PGM(s)}$	–	–	5	ms	–
8.5.4	Programming delay time	$t_{PGM(d)}$	–	–	2.4	ms	T_j = 25 °C
8.5.5	Erase delay time	$t_{ERASE(d)}$	–	–	2.4	ms	T_j = 25 °C
8.5.6	Number of EEPROM erase & programming cycles per register	N_{PGM}	–	–	10	Cycles	–

1) Not subject to production test, specified by design

9 Power Stage

The output stages are realized as high side current sources (Drain of output transistor is internally connected to Vs) with a maximum current of I_{PWR} (**Pos. 9.3.1**). During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.

9.1 PWRx Output

The base driver output (PWRx) is designed to drive external NPN-transistors in linear mode. Base resistors can be used to limit the base current in low V_s voltage conditions.

9.2 SENSE Input

The integrated control loop is designed to regulate the voltage on the sense input (SENSEx) to V_{SENSE}. V_{SENSE} can be adjusted during module calibration via the MSTR_L1_P02 frame via NVM-programming. Four different values can be programmed, see **Table 31**. The sense voltage for all three channels can only be adjusted simultaneously to four different voltages using NVM register 0x00 bit 20 and 21. The setting is valid for all three output stages. The maximum system accuracy can be achieved by using the highest sense voltage:

Table 31 Sense voltages

Current_adjust register	Sense voltage $V_{SENSE(nom)}$ [mV]
0	120
1	240
2	360
3	480

The switching time of the base driver output voltage is defined in the following figure.

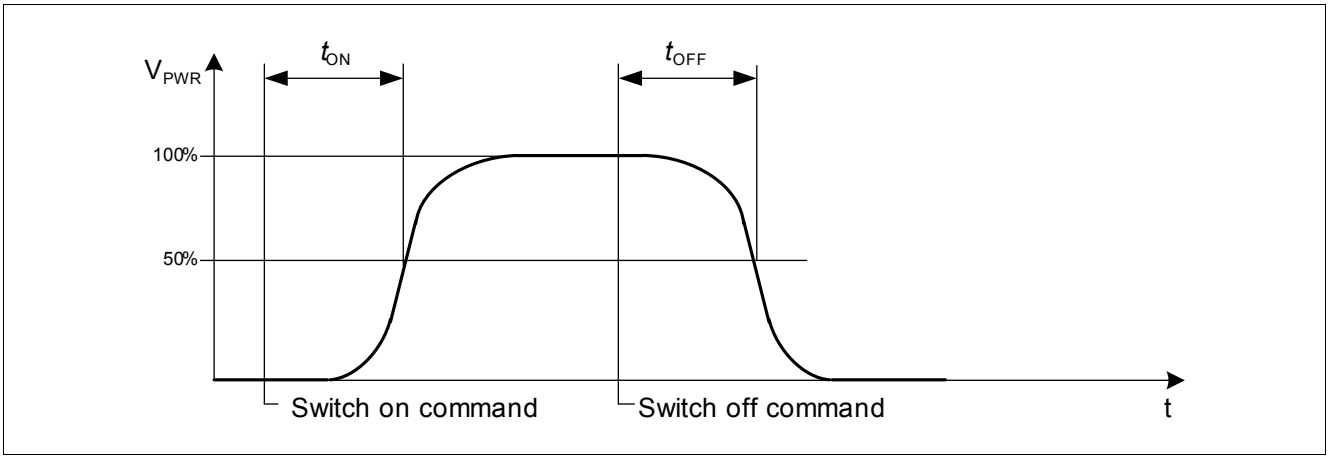


Figure 11 Switching times

The following setup is used for testing the sense voltage V_{SENSE}.

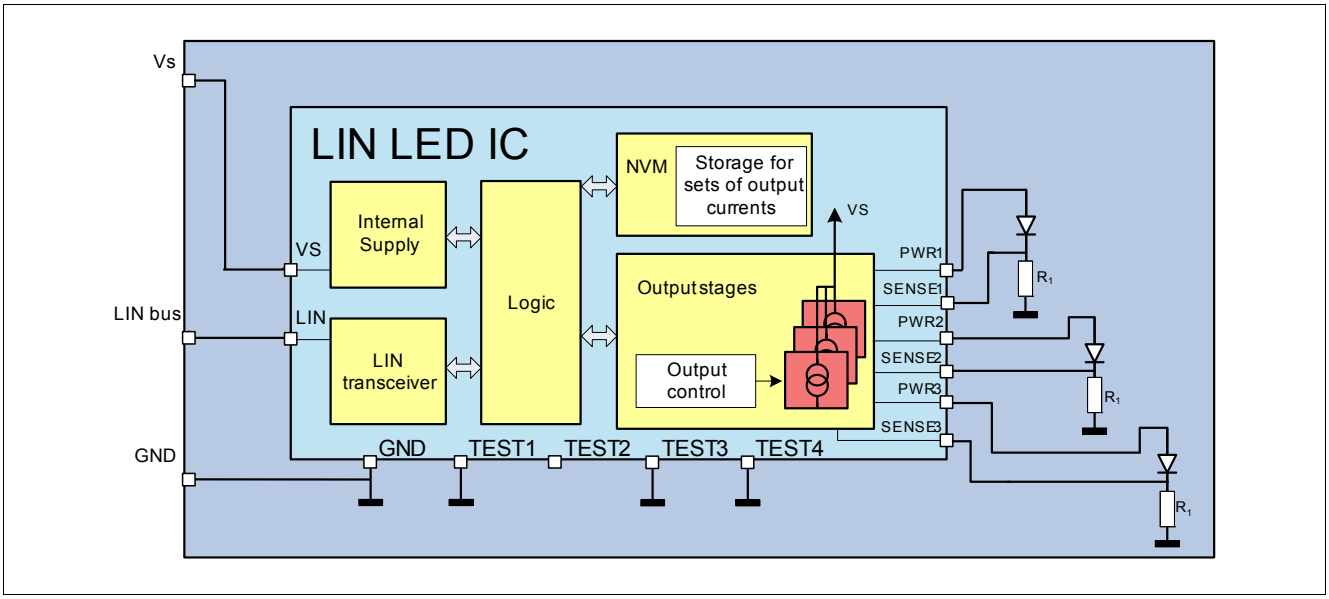


Figure 12 Sense voltage test setup

9.3 Electrical Characteristics Power Stage

Electrical Characteristics: Power Stage

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.3.1	Maximum power output current	I_{PWRx}	40	–	–	mA	–
9.3.2	Power output pull-down resistor	R_{PWRx}	80	115	150	Ω	V_{PWRx} = 1 V I_{PWRx}= 10 mA
9.3.3	Power output voltage drop for current control	V_S - V_{PWRx}	1.8 0.8	– –	4.3 3.2	V	I_{PWRx}= 12 mA I_{PWRx}= 40 mA
9.3.4	Sense input voltage accuracy	V_{SENSEx}	-10%	–	+10%		R_1 = 10 Ω setup according **Figure 12**
9.3.5	Sense input current	I_{SENSEx}	0.5	–	0.5	µA	V_{SENSE} = 480 mV
9.3.6	Base driver output switch on-time to 50% of V_S	t_{on}	–	–	2	µs	[1] R_1 = 10 Ω `Current_adjust` register = 3 V_{PWRx} = 0.5 * V_S setup according **Figure 12**
9.3.7	Base driver output switch off-time to 50% of V_S	t_{off}	–	–	2	µs	[1] R_1 = 10 Ω `Current_adjust` register = 3 V_{PWRx} = 0.5 * V_S setup according **Figure 12**

Electrical Characteristics: Power Stage (cont'd)

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.3.8	Base driver output pulse time	$t_{PWR(min)}$	4.5	–	–	µs	1)–
9.3.9	Base driver output switching frequency	f_{max}	–	–	110	kHz	1) –

1) Not subject to production test, specified by design

9.4 Protection and Diagnosis

9.4.1 Over Load Behavior

An over load detection circuit is integrated in the LIN LED Driver IC. It is realized by a temperature monitoring of the output stages (PWRx). A two step diagnosis/protection concept is integrated in the LIN LED Driver IC. shows an example of the over temperature:

1. As soon as the output stage temperature exceeds $T_{j(warn)}$ the ApInfo0 bit of the LIN frame LED_L1_P00 is set to 1. The warning is not latched, the device remains fully functional. This feature is integrated to allow the LIN master module to react on high temperature conditions in the LED module.
2. As soon as the junction temperature exceeds the over temperature threshold $T_{j(OT)}$ all three output stages are turned off. An over temperature condition is reported in the ApInfo2 bits. The error is latched, this means the output stages do not automatically turn on again after cooling down. This feature is implemented to a avoid "flickering" of the LEDs at static output overload condition. To unlatch and reactivate the outputs, the intensity must be programmed to zero and then sub sequentially programmed to a value higher than zero.

Figure 13 shows the function of the temperature warning and over temperature protection.

Table 32 Temperature prewarning settings

Register value	Typ. prewarning temperature $T_{j(warn)}$
0	140°C (default value)
1	120°C
2	160°C
3	function deactivated

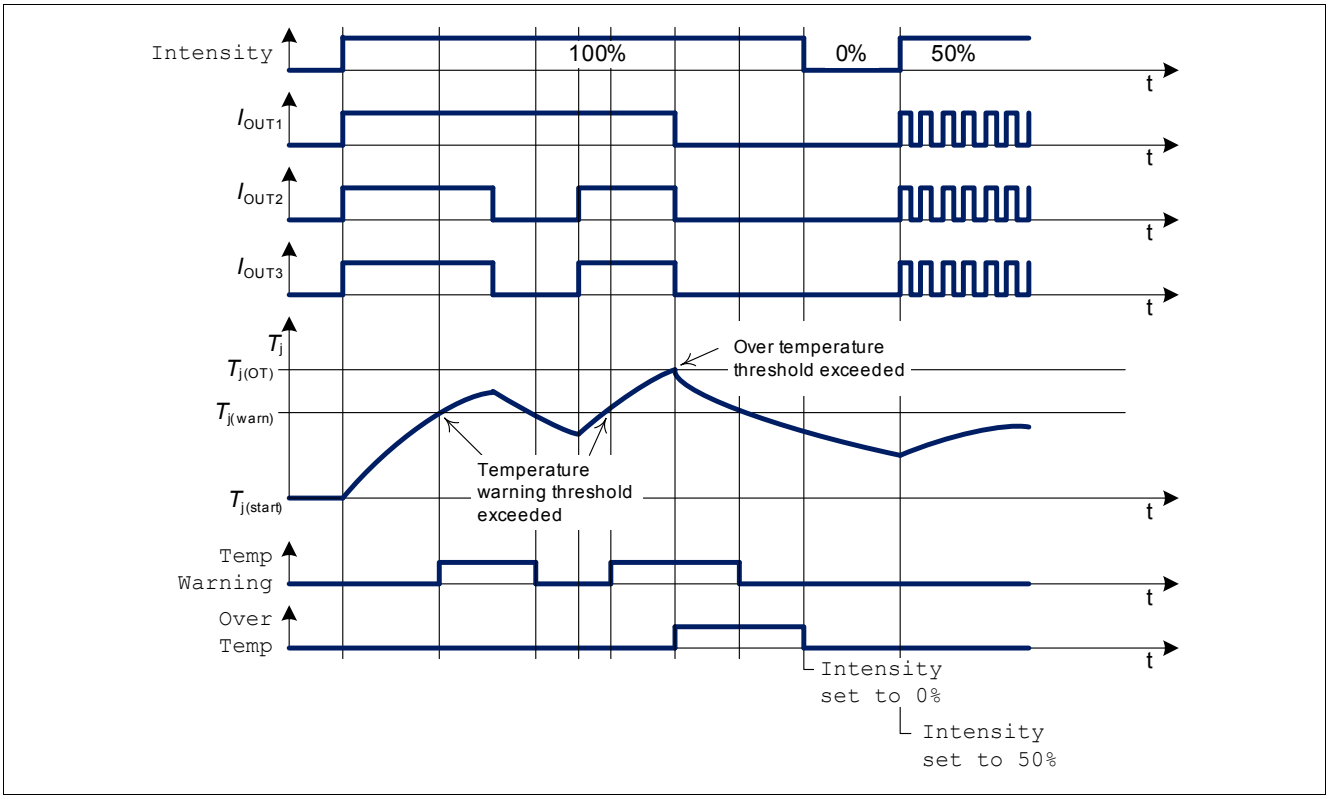


Figure 13 Temperature warning and over temperature shut down

9.5 Electrical Characteristics Protection and Diagnosis

Electrical Characteristics: Protection and Diagnosis

V_S = 7 V to 18 V, T_j = -40 °C to 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.5.10	Over temperature prewarning threshold	$T_{j(warn)}$	125	140	155	°C	1) default $T_{j(warn)}$ selected
9.5.11	Over Load protection / Over temperature output deactivation threshold	$T_{j(OT)}$	150	175	–	°C	1)
9.5.12	Minimum difference between Over temperature warning and deactivation threshold	$T_{j(OT)}$ - $T_{j(warn)}$	25	–	–	K	1)

1) Not subject to production test, specified by design

10 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

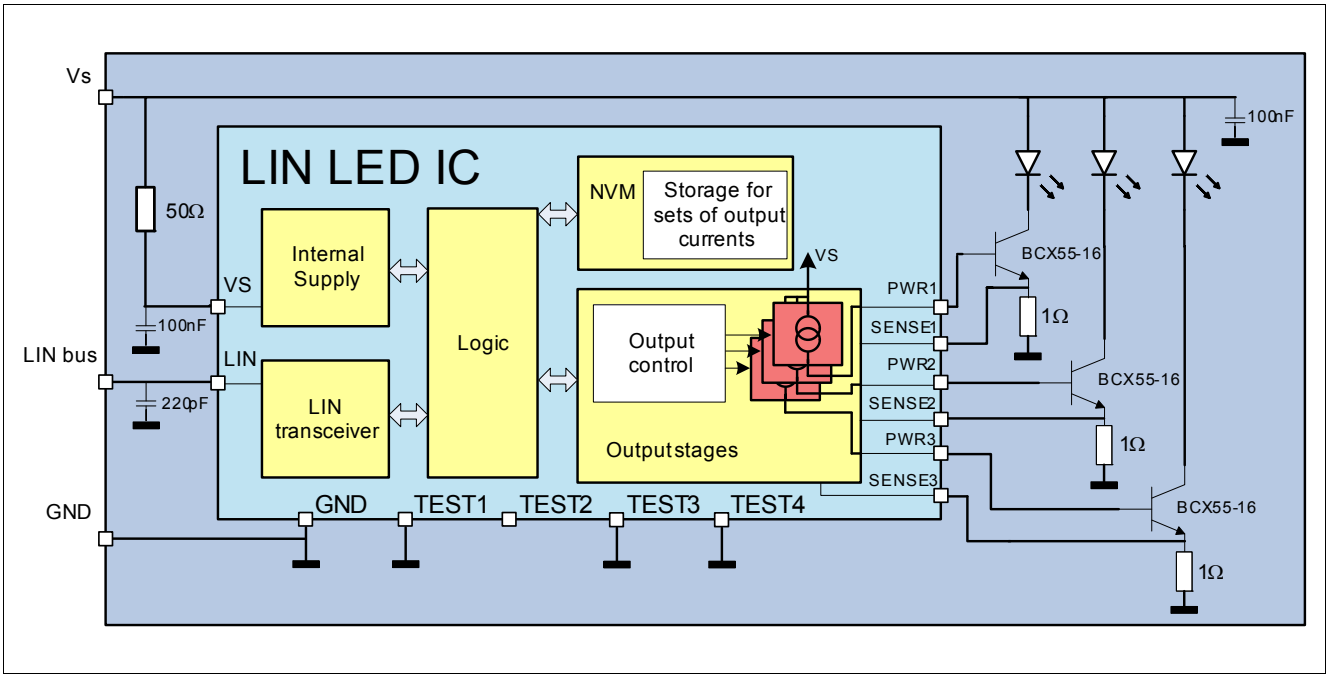


Figure 14 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

10.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**

11 Package Outlines

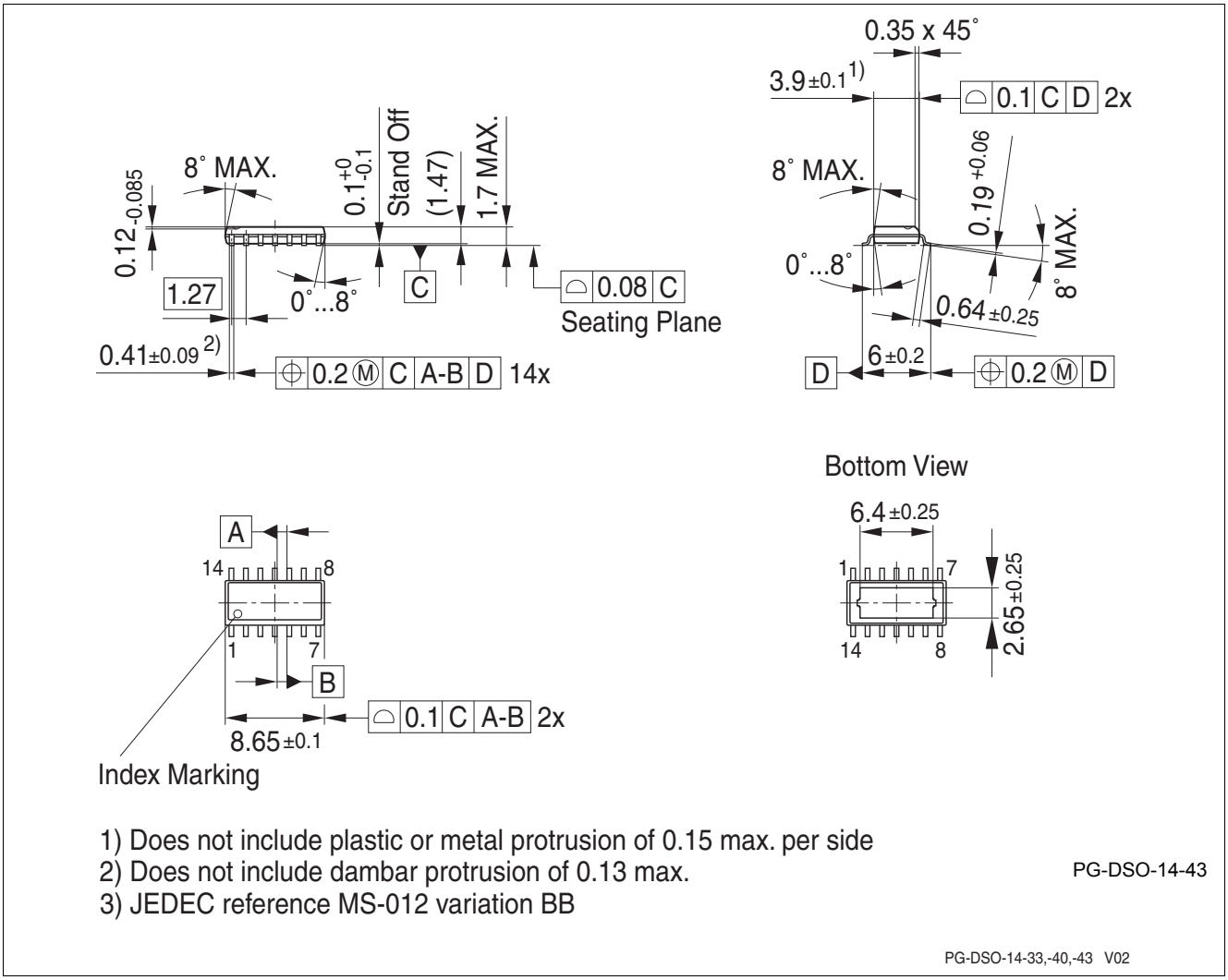


Figure 15 PG-DSO-14-43

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

12 Revision History

Revision	Date	Changes
1.0	2012-07-02	Initial revision

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