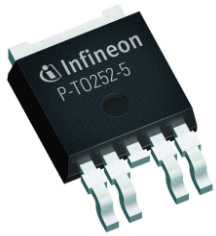
Linear Voltage Regulator
3.3 V Fixed Output Voltage

TLE 4275 V33

Feature Overview

- Output voltage 3.3 V ± 2 %
- Current capability 400 mA
- Stable with ceramic output capacitor
- Reset circuit functional without supply voltage present
- Reset output active low down to V_Q = 1 V
- Reset circuit sensing the output voltage with programmable delay time
- Maximum input voltage -42 V ≤ V_I ≤ +45 V
- ESD Resistivity 4 kV (Human Body Model)
- Reverse polarity protection
- Short circuit protection
- Overtemperature shutdown
- Automotive temperature range -40 °C ≤ T_j ≤ 150 °C
- Green Product (RoHS compliant)
- AEC qualified



PG-TO252-5-11

PG-TO263-5-1

The TLE 4275 V33 is a monolithic integrated low dropout fixed output voltage regulator for loads up to 400mA. An integrated reset generator with adjustable power-on delay time as well as several protection circuits predestine the IC for supplying microprocessor systems in an automotive environment.

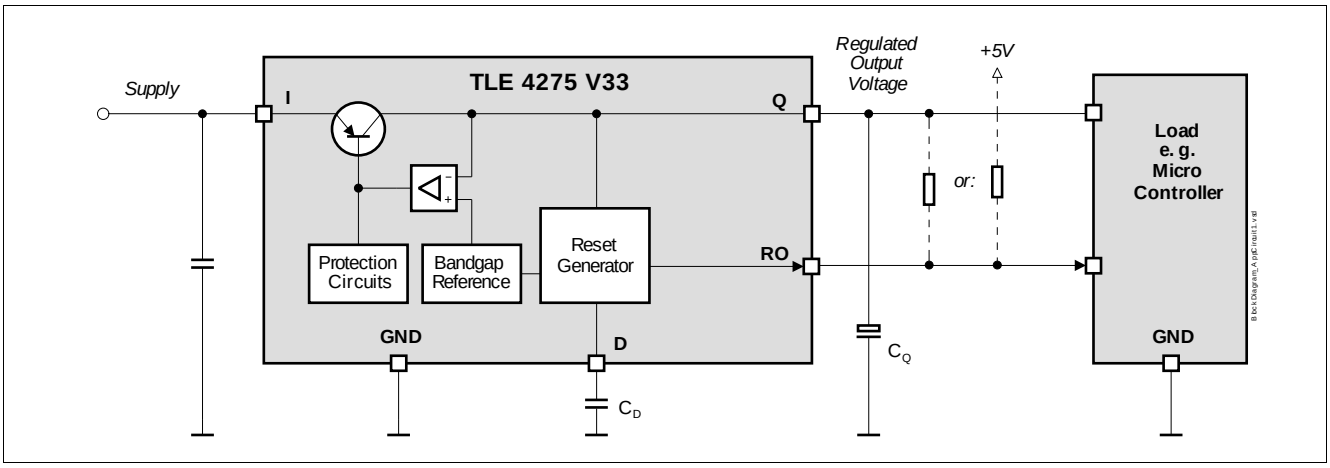
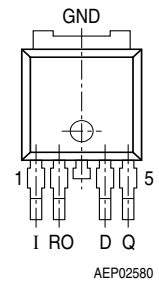


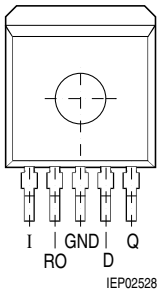
Figure 1 Simplified Block Diagram and Typical Application

Type	Package
TLE 4275 D V33	PG-TO252-5-11 (RoHS compliant)
TLE 4275 G V33	PG-TO263-5-1 (RoHS compliant)

1 Pin Definitions and Functions



PG-TO252-5-11



PG-TO263-5-1

Figure 2 Pin Assignment

Pin	Symbol	Function
1	I	**Regulator Input and IC Supply.** • For compensating line influences, a capacitor to GND close to the IC terminals is recommended.
2	RO	**Reset Output.** • Open collector output. External pull-up resistor to a positive voltage rail required. • Leave open if the reset function is not needed.
3	GND	**PG-TO263-5-1 only: Ground Reference.** • Connect to TAB and heatsink area
4	D	**Reset Delay Timing.** • Connect a ceramic capacitor to GND for reset delay timing adjustment. • Leave open if the reset function is not needed.
5	Q	**Regulator Output**. • Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table “Functional Range”.
TAB	GND	**PG-TO252-5-11 only: Ground Reference.** • Connect to heatsink area.
TAB	–	**PG-TO263-5-1 only:** • Connect to heatsink area and ground reference (pin 3).

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

-40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Regulator Input and IC Supply I						
2.1.1	Voltage	V_I	-42	45	V	–
2.1.2	Current	I_I	–	–	mA	internally limited
Regulator Output Q						
2.1.3	Voltage	V_Q	-1	16	V	–
2.1.4	Current	I_Q	–	–	mA	internally limited
Reset Output RO						
2.1.5	Voltage	V_{RO}	-0.3	25	V	–
2.1.6	Current	I_{RO}	-5	5	mA	
Reset Delay Timing D						
2.1.7	Voltage	V_D	-0.3	7	V	–
2.1.8	Current	I_D	-2	2	mA	
Ground GND						
2.1.9	Current	I_{GND}	–	–	mA	internally limited
Temperatures						
2.1.10	Junction Temperature	T_j	-40	150	°C	–
2.1.11	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
2.1.12	ESD Resistivity	$V_{ESD,HBM}$	-4	4	kV	HBM[1)]
2.1.13		$V_{ESD,CDM}$	-500	500	V	CDM[2)]
Moisture Level						
2.1.14	Moisture Level	MSL	1		–	–

1) ESD susceptibility, Human Body Model “HBM” according to EIA/JESD 22-A114B.

2) ESD susceptibility, Charged Device Model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

2.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions / Remarks
			Min.	Max.		
2.2.1	Input Voltage	V_I	4.4	42	V	$V_Q = V_I - V_{dr}$ 1)
2.2.2	Junction Temperature	T_j	-40	150	°C	–
2.2.3	Output Capacitor	C_Q	22	–	µF	– 2)
2.2.4		ESR_{CQ}	–	3	Ω	–

1) For details on max. output current vs. input voltage see Table 1: Electrical Characteristics Voltage Regulator

2) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

2.3 Thermal Resistance

Pos.	Parameter	Symbol	Typ. Value	Unit	Conditions
Package P-TO252-5:					
2.3.1	Junction – Ambient PG-TO252-5-11	$R_{th,j-a}$	144	K/W	Footprint only[1)]
2.3.2			78	K/W	300 mm² PCB heatsink area[1)]
2.3.3			55	K/W	600 mm² PCB heatsink area[1)]
2.3.4	Junction – Case PG-TO252-5-11	$R_{th,j-c}$	1.8	K/W	
Package P-TO263-5:					
2.3.1	Junction – Ambient PG-TO263-5-1	$R_{th,j-a}$	79	K/W	Footprint only[1)]
2.3.2			53	K/W	300 mm² PCB heatsink area[1)]
2.3.3			39	K/W	600 mm² PCB heatsink area[1)]
2.3.4	Junction – Case PG-TO263-5-1	$R_{th,j-c}$	1.3	K/W	

1) EIA/JESD 52_2, FR4, 80 × 80 × 1.5 mm; 35µ Cu, 5µ Sn; horizontal position; zero airflow.
Not subject to production test; specified by design.

3 Block Description and Electrical Characteristics

3.1 Voltage Regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "Operating Range" have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor C_I is strongly recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 22 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behaviour of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC lifetime.

The TLE 4275 V33 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions For details see typical performance graphs.

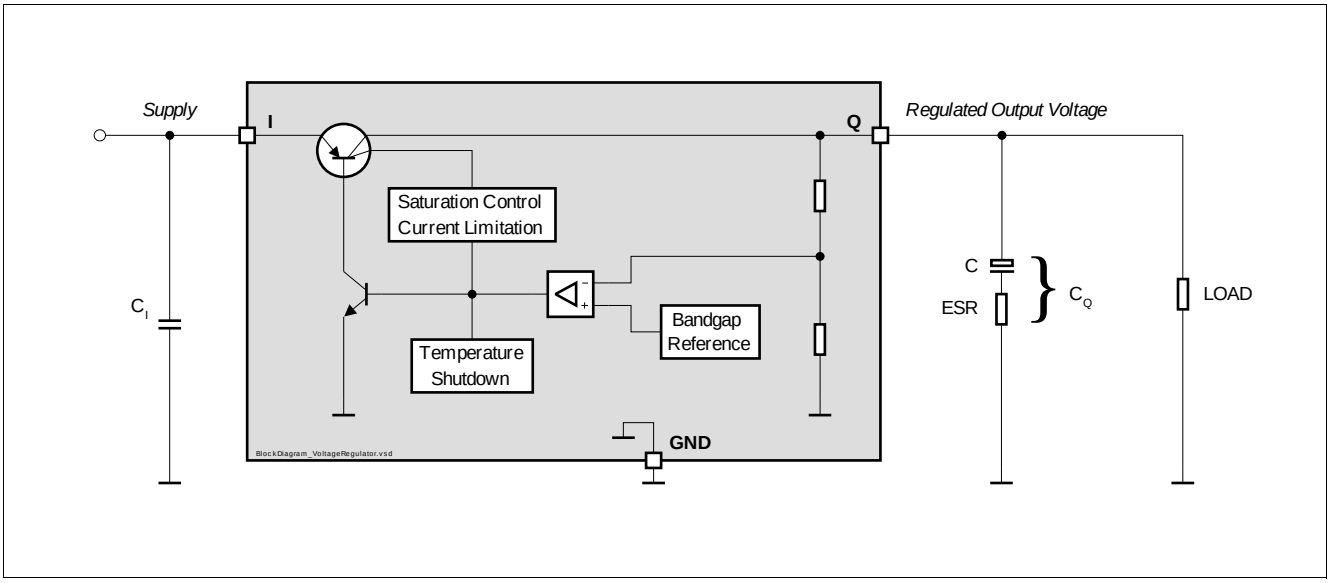


Figure 3 Block Diagram Voltage Regulator Circuit

Table 1 Electrical Characteristics Voltage Regulator

V_I = 13.5 V; -40 °C ≤ T_j ≤ 150 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Remark / Test Condition
			Min.	Typ.	Max.		
3.1.1	Output Voltage	V_Q	3.23	3.3	3.37	V	1 mA ≤ I_Q ≤ 400 mA; 5 V ≤ V_I ≤ 28 V
3.1.1			3.23	3.3	3.37	V	1 mA ≤ I_Q ≤ 300 mA; 4.4 V ≤ V_I ≤ 28 V
3.1.2			3.23	3.3	3.37	V	1 mA ≤ I_Q ≤ 200 mA; 4.4 V ≤ V_I ≤ 40 V
3.1.3	Load Regulation steady-state	$dV_{Q,load}$	-30	-15	–	mV	I_Q = 5 mA to 400 mA; V_I = 6 V
3.1.4	Line Regulation steady-state	$dV_{Q,line}$	–	5	15	mV	V_I = 8 V to 32 V; I_Q = 5 mA
3.1.5	Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 0.5 Vpp [1]
3.1.6	Output Current Limitation	$I_{Q,max}$	401	–	1000	mA	V_Q = 3.0 V
3.1.7	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing [1]
3.1.8	Overtemperature Shutdown Threshold Hysteresis	$T_{j,hy}$	–	25	–	K	

1) Parameter not subject to production test; specified by design.

3.2 Current Consumption

Table 2 Electrical Characteristics Current Consumption

V_I = 13.5 V; -40 °C ≤ T_j ≤ 150 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
3.2.1	Current Consumption $I_q = I_Q - I_I$	I_q	–	180	220	µA	I_Q = 1 mA; T_j = 25 °C
3.2.2			–	180	240	µA	I_Q = 1 mA; T_j ≤ 85 °C
3.2.3			–	8	12	mA	I_Q = 250 mA
3.2.4			–	20	30	mA	I_Q = 400 mA

3.3 Reset Function

The reset function contains serveal features:

Output Undervoltage Reset:

An output undervoltage condition is indicated setting the Reset Output “RO” to low. This signal might be used to reset a microcontroller during low supply voltage.

In case the battery voltage is already lower than the buffered output voltage V_Q of the voltage regulator, the reset circuit is supplied from the output “Q”, ensuring a defined reset switching threshold also at V_I = 0 V. The Reset Output “RO” is held “low” down to an output voltage of V_Q = 1 V, even if the input voltage V_I is 0 V.

Power-On Reset Delay Time:

The power-on reset delay time $t_{d,PWR-ON}$ allows a microcontoller and oscillator to start up. This delay time is the time period from exceeding the reset switching threshold V_{RT} until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time $t_{d,PWR-ON}$ is defined by an external delay capacitor C_D connected to pin “D” which is charged up by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

For easy calculating the power-on reset delay time, a multiplier factor $F_{d,PWR-ON} = t_{d,PWR-ON} / C_D$ is specified. Hence, $t_{d,PWR-ON}$ becomes:

$$t_{d,PWR-ON} = F_{d,PWR-ON} * C_D \ . \quad (1)$$

For a precise calculation consider also the delay capacitor’s tolerance.

Undervoltage Reset Delay Time:

Unlike the power-on reset delay time, the undervoltage reset delay t_d time considers a short output undervoltage event where the delay capacitor C_D is assumed to be discharged to $V_D = V_{DST,lo}$ only before the charging sequence restarts. Therefore, the undervoltage reset delay time t_d is defined by the delay capacitor charge current $I_{D,ch}$ starting from $V_D = V_{DST,lo}$ and the external delay capacitor C_D.

For easy calculating the undervoltage reset delay time, a multiplier factor $F_d = t_d / C_D$ is specified. Hence, t_d becomes:

$$t_d = F_d * C_D \ . \quad (2)$$

For a precise calculation consider also the delay capacitor’s tolerance.

Reset Reaction Time:

The total reset reaction rime $t_{rr,total}$ considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D (see typical performance graph for details). Hence, the total reset reaction rime becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \ . \quad (3)$$

Reset Output “RO” Low for $V_Q \geq 1$ V:

In case of an undervoltage reset condition reset output “RO” is held “low” for $V_Q \geq 1$ V, even if the input voltage V_I is 0 V. This is achieved by supplying the reset circuit from the output capacitor.

Reset Output "RO":

The Reset Output "RO" is an open collector output requiring an external pull-up resistor to a voltage rail V_{IO}. As the maximum Reset Output Sink Current $I_{RO,max}$ is limited, the minimum external pull-up resistor calculates:

$$R_{RO,external,min} = V_{IO} / I_{RO,max}. \quad (4)$$

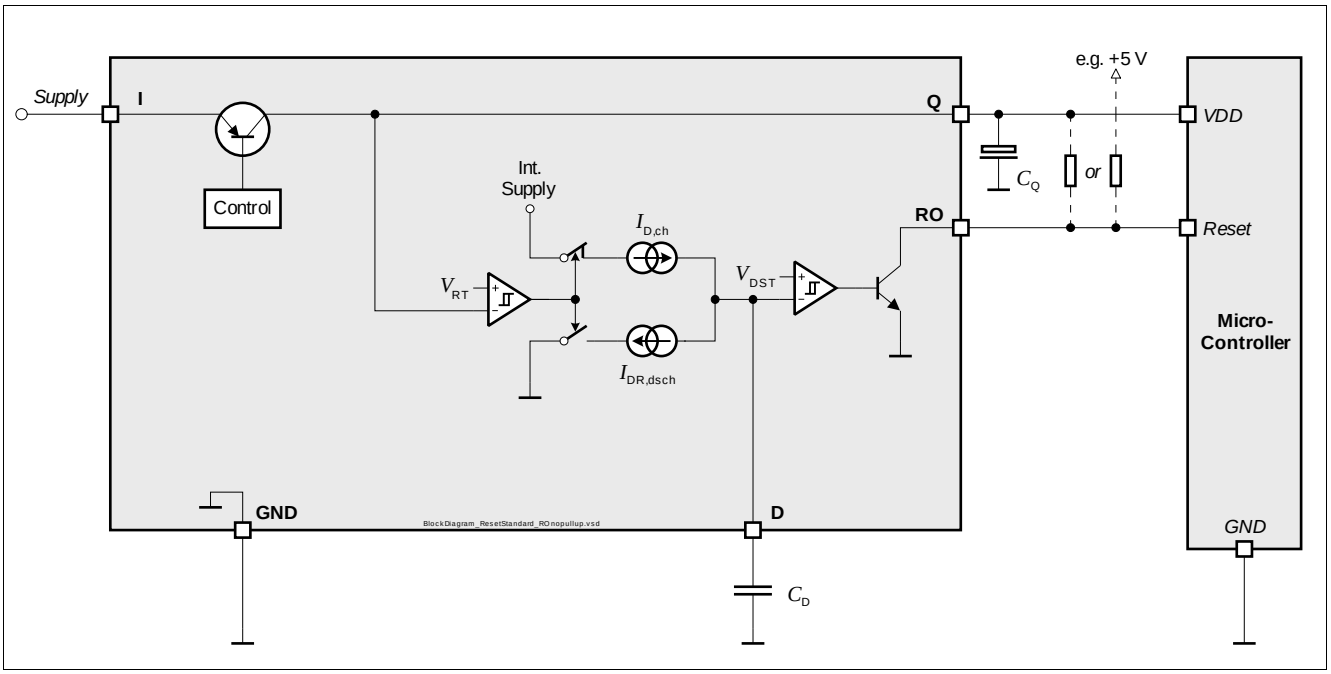


Figure 4 Block Diagram Reset Circuit

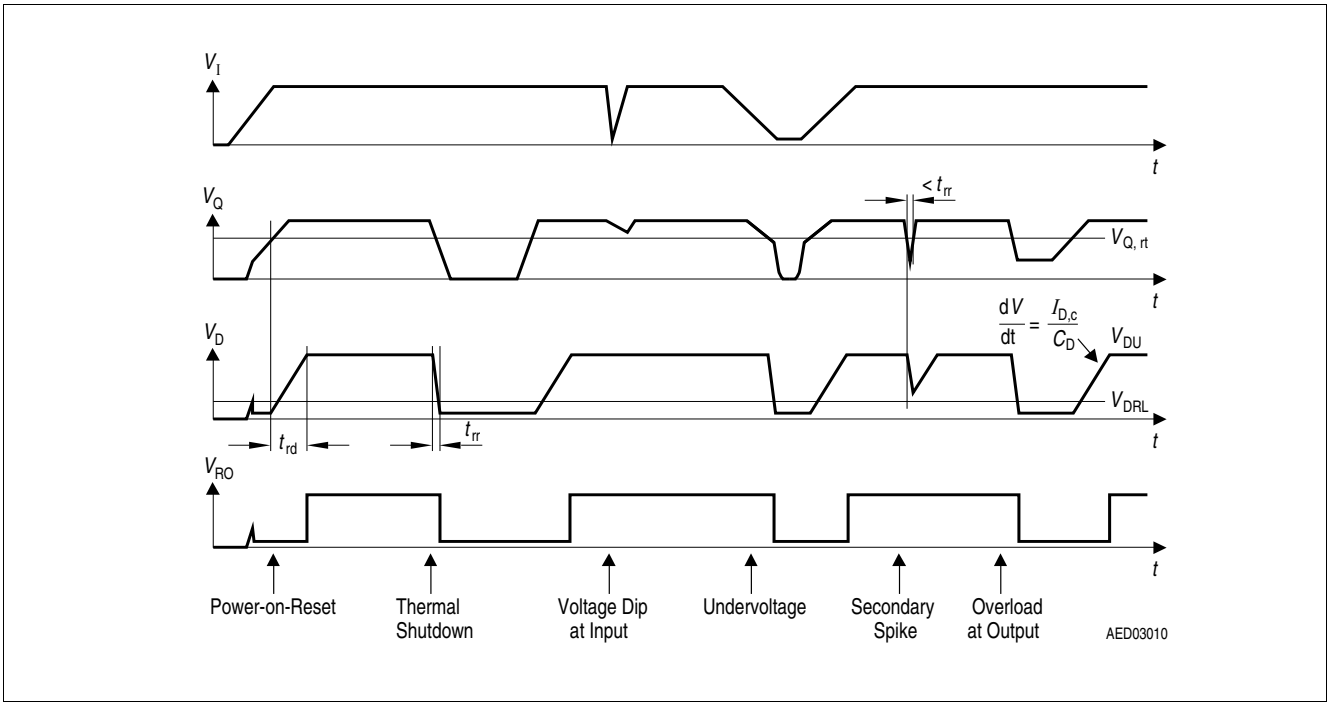


Figure 5 Timing Diagram Reset

Table 3 Electrical Characteristics Reset Function

V_I = 13.5 V; -40 °C ≤ T_j ≤ 150 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Pos.	**Parameter**	**Symbol**	**Limit Values**			**Unit**	**Conditions / Remarks**
			Min.	**Typ.**	**Max.**		
Output Undervoltage Reset Comperator:							
3.3.1	Output Undervoltage Reset Switching Threshold	V_{RT1}	3.06	3.13	3.2	V	$V_I \geq 4.4$ V V_Q decreasing
3.3.2		V_{RT2}	2.5	2.9	V_{RT1}	V	V_I = 0 V V_Q decreasing
3.3.3	Output Undervoltage Reset Headroom	V_{RH}	100	130	–	mV	Calculated Value: $V_{Q,nom}$ - V_{RT} . $V_I \geq 4.4$ V
Reset Output RO:							
3.3.4	Reset Output Low Voltage	$V_{RO,low}$	–	0.2	0.4	V	1 V ≤ V_Q ≤ V_{RT} ; I_{RO} = 0.3 mA
3.3.5	Reset Output Sink Current Limitation	$I_{RO,max}$	0.3	–	–	mA	1 V ≤ V_Q < V_{RT} ; V_{RO} = 3.3V
3.3.6	Reset Output External Pull-up Resistor to V_Q	R_{RO}	3.3	–	–	kΩ	V_{RO} ≤ 0.4 V at reset condition
3.3.7	Reset Output Leakage Current	$I_{RO,leak}$	–	0	2	µA	V_{RO} = 5 V
Reset Delay Timing:							
3.3.8	Upper Delay Switching Threshold	$V_{DST,hi}$	–	1.8	–	V	–
3.3.9	Lower Delay Switching Threshold	$V_{DST,lo}$	–	0.6	–	V	–
3.3.10	Delay Capacitor Charge Current	$I_{D,ch}$	–	6	–	µA	V_D = 1 V
3.3.11	Delay Capacitor Reset Discharge Current	$I_{DR,dsch}$	–	70	–	mA	V_D = 1 V
3.3.12	Undervoltage Reset Delay Time Factor $F_d = t_d / C_D$	F_d	0.13	0.20	0.27	ms / nF	Calculated Value: $F_d = (V_{DST,hi} - V_{DST,lo}) / I_{D,ch}$ $C_D \geq 10$ nF [1]
3.3.13	Power-on Reset Delay Time Factor $F_{d,PWR-ON} = t_{d,PWR-ON} / C_D$	$F_{d,PWR-ON}$	0.21	0.30	0.39	ms / nF	Calculated Value: $F_d = V_{DST,hi} / I_{D,ch}$ $C_D \geq 10$ nF [1]
3.3.14	Delay Capacitor Discharge Time	$t_{rr,d}$	–	0.7	2	µs	Calculated Value: $t_{rr,d} = C_D*(V_{DST,hi} - V_{DST,lo})/ I_{D,dsch}$ C_D = 47 nF
3.3.15	Internal Reset Reaction Time	$t_{rr,int}$	–	2	6.5	µs	C_D = 0 nF [2]

1) For lower values of C_D, the accuracy given is not guaranteed; see typ. performance graph for details.

2) Parameter not subject to production test; specified by design.

4 Package Outlines

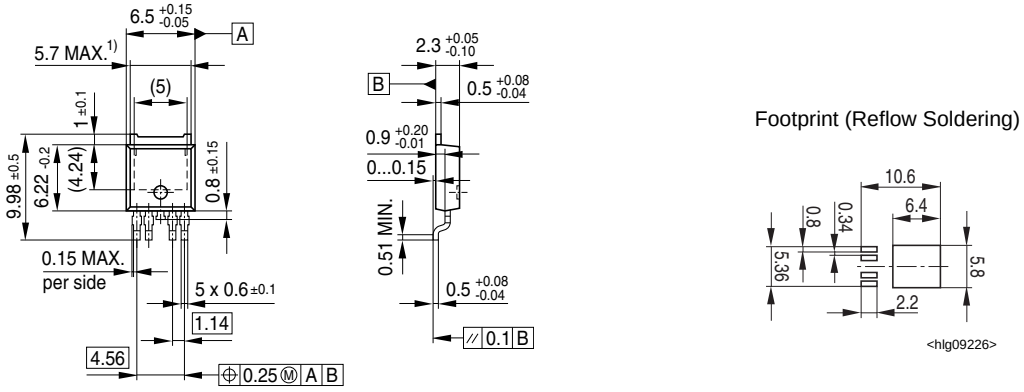


Figure 6 PG-TO252-5-11 Package Outline and Footprint

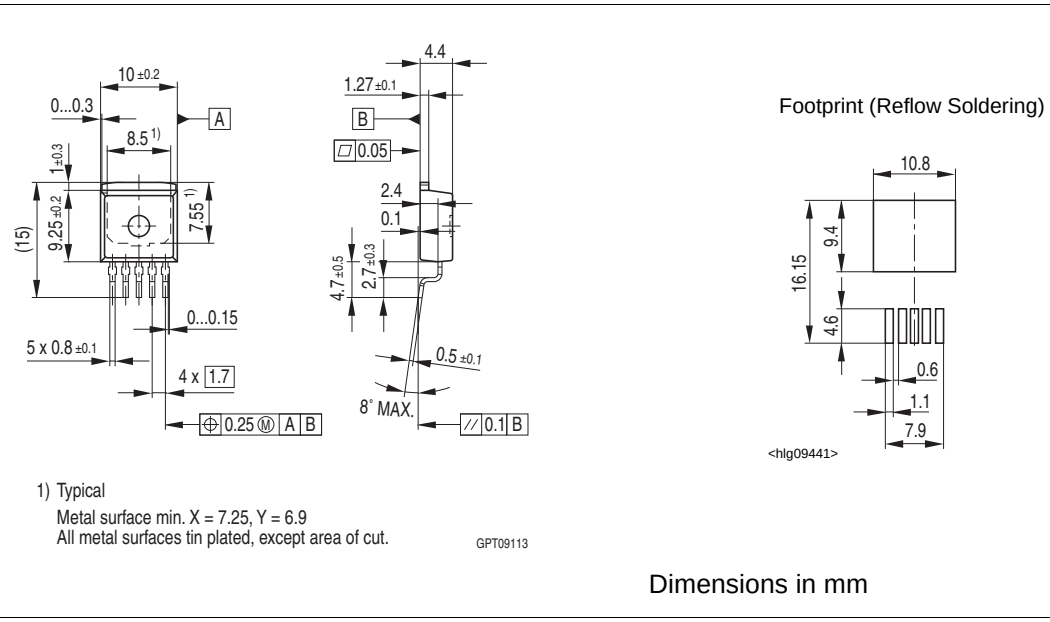


Figure 7 PG-TO263-5-1 Package Outline and Footprint

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Find more package information on the Infineon Internet Page: http://www.infineon.com/packages.

5 Revision History

Revision	Date	Changes
1.2	2015-12-18	Page 7 update on formula 1 and 2. Page 9 update on 3.3.13 formula in conditions column
1.1	2015-01-15	Parameter **2.1.14** MSL Min. value changed from 3 to 1.
1.0	2006-09-22	

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