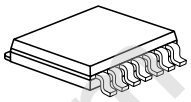
Triple Voltage Regulator

TLE 4418 G

Target Data

Features

- Triple Output voltage 2.6 V(1.2 A), 3.3 V(1.2 A) and 8.0 V(0.2 A)
- Wide input voltage range
- Overtemperature protection
- Short circuit proof
- SMD-Power package



P-SFMG-7-1

Type	Ordering Code	Package
▼ TLE 4418 G		P-SFMG-7-1 (SMD)

▼ New type

Functional Description

The TLE 4418 G is a monolithic integrated voltage regulator with a fixed triple output voltage of 2.6 V with max. 1.2 A, 3.3 V with max. 1.2 A and 8.0V with max. current 0.2 A. The regulator is supplied by two input voltages: V_{CC} (nominal 5 V)= 4.75 V to 40 V and V_{DD} (nominal 12 V)= 10.8 V to 40 V. It can also be operated without the V_{DD} input voltage resulting in a reduced output voltage precision/ higher drop voltage. The IC is short circuit proof due to its integrated overcurrent and overtemperature protection circuits. The operating temperature range extends from T_J=0°C to 125°C with a thermal shutdown disabling all output voltages at typ. 150°C.

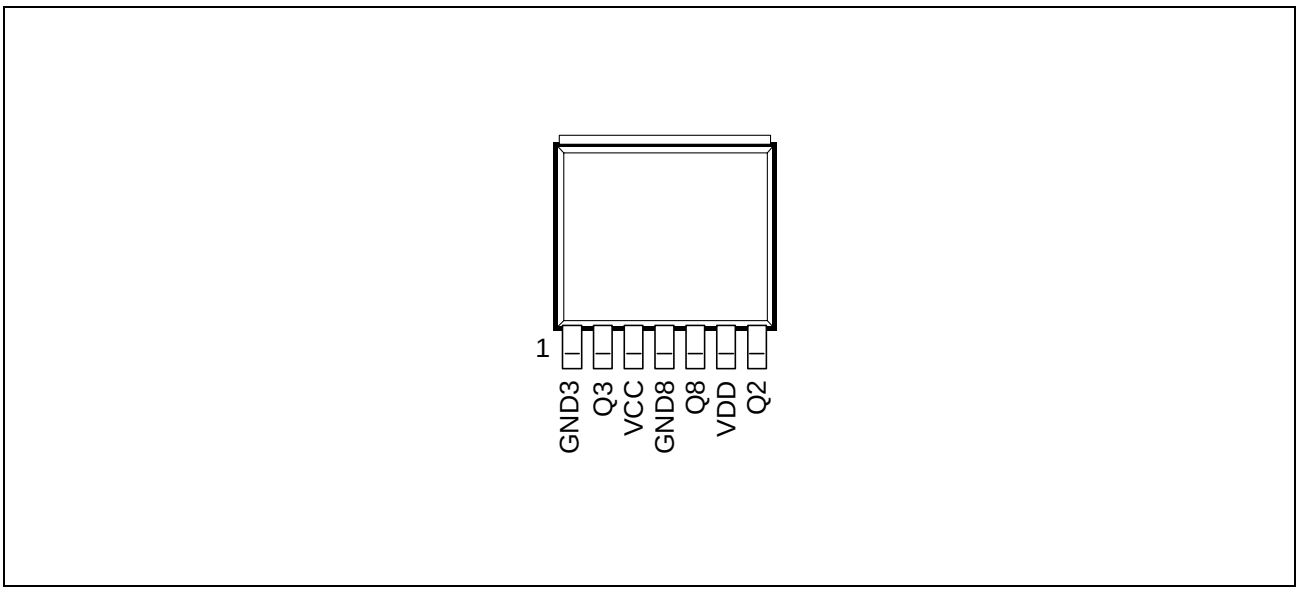


Figure 1 **Pin Configuration** (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	GND3	**Ground** for Q2 and Q3
2	Q3	**Output 3.3 V**; connect to GND via a capacitor $C_{Q3} \geq 2.2$ µF, ESR≤ 4 Ω.
3	VCC	**Supply Input**; 5V nominal input voltage. Block to GND directly at the IC with a 100 nF ceramic capacitor.
4	GND8	**Ground** for Q8
5	Q8	**Output 8 V**; connect to GND via a capacitor $C_{Q8} \geq 2.2$ µF, ESR≤ 4 Ω
6	VDD	**Supply Input**; 12V nominal input voltage. Block to GND directly at the IC with a 100 nF ceramic capacitor.
7	Q2	**Output 2.6 V**; connect to GND via a capacitor $C_{Q2} \geq 2.2$ µF, ESR≤ 4 Ω.

Circuit Description

Each of the output voltages features a reference voltage kept highly accurate by internal resistance adjustment. An error amplifier compares this reference voltage to the divided output voltage and drives the base of the Darlington power element. Over-saturation of the power element is prevented by an integrated saturation control circuit. While the output current is driven by V_{CC} maintaining a reasonable power dissipation the higher voltage level at V_{DD} allows to keep the drop voltage relatively low and supplies the 8.0 V output. The regulation loops are kept stable even for low output capacitances down to 2.2 µF (ESR $\leq$ 4 Ω).

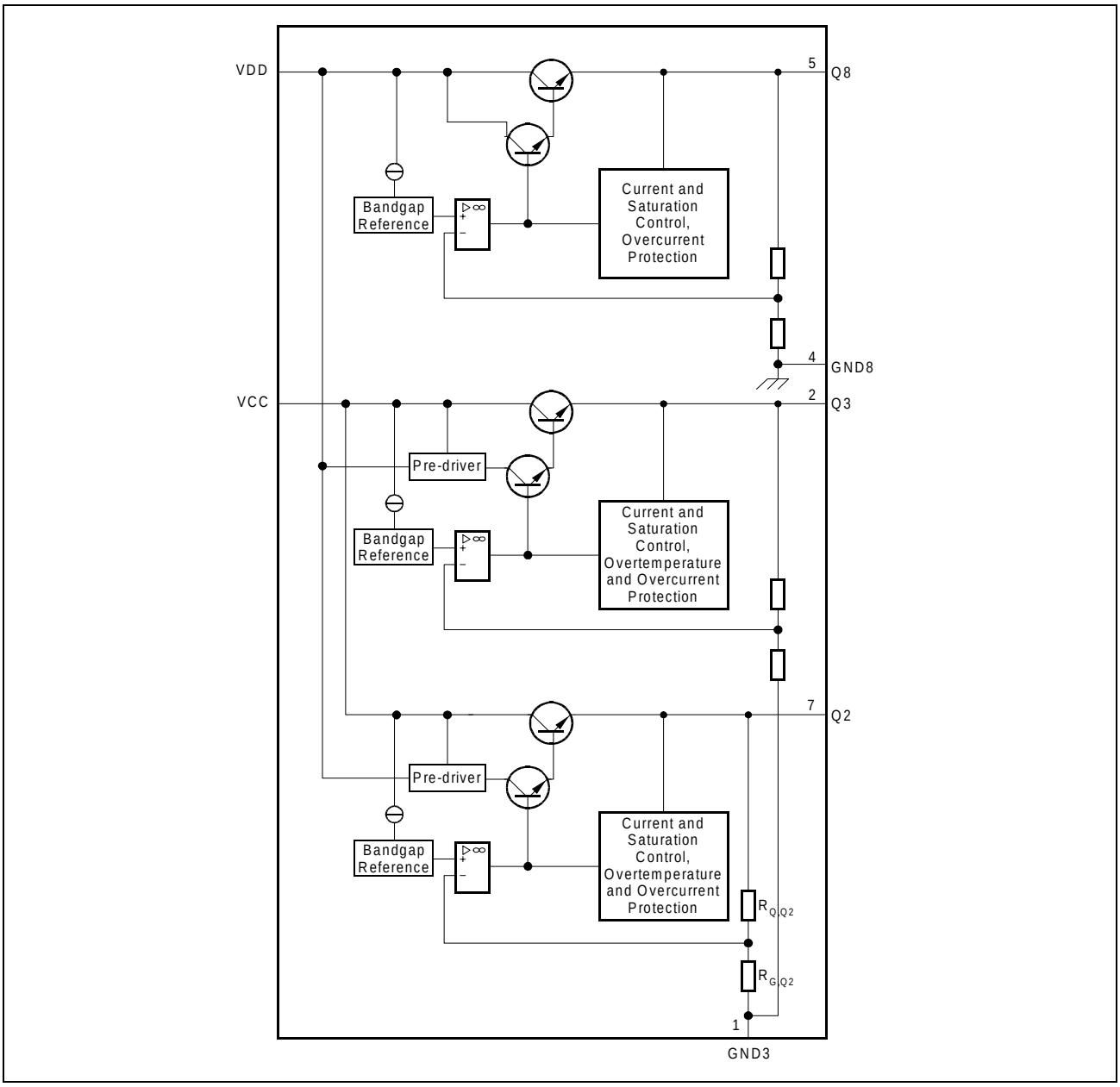


Figure 2 Block Diagram

Absolute Maximum Ratings

0 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Input					
Voltage	V_{CC}	– 0.3	40	V	–
Current	I_{CC}	– 20	*	mA	*internally limited
V_{DD} Input					
Voltage	V_{DD}	– 0.3	40	V	–
Current	I_{DD}	– 20	*	mA	*internally limited
Output Q2					
Voltage	V_{Q2}	– 0.3	16	V	–
Current	I_{Q1}	– 20	*	mA	*internally limited
Output Q3					
Voltage	V_{Q3}	– 0.3	16	V	–
Current	I_{Q3}	– 20	*	mA	*internally limited
Output Q8					
Voltage	V_{Q8}	– 0.3	16	V	–
Current	I_{Q8}	– 20	*	mA	*internally limited
Temperatures					
Junction temperature	T_j	0	150	°C	–
Storage temperature	T_{stg}	– 65	150	°C	–

Absolute Maximum Ratings (cont'd)
0 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Thermal Resistances

Junction ambient	R_{thja}	–	65	K/W	300 mm^2 heat sink area[1)]
		–	50	K/W	600 mm^2 heat sink area[1)]

1) Worst case in still air according to JEDEC JESD51-2.

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input voltage V_{CC}	V_{CC}	4.75	40	V	–
Input voltage V_{DD}	V_{DD}	10.8	40	V	–
Input voltage V_{DD}	V_{DD}	0	10.8	V	reduced output voltage precision
Junction temperature	T_j	0	150	°C	–

Electrical Characteristics

V_{CC}=5.0V; V_{DD}=12.0V; 0 °C < T_j < 125 °C; unless otherwise specified; all voltages with respect to ground; positive current defined flowing into pin

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Q2						
Output voltage	V_{Q2}	2.55	2.60	2.65	V	1mA≤I_{Q2}≤1.2 A; 4.75V≤V_{CC}≤5.25V
Output voltage	V_{Q2}	2.20		2.65	V	V_{DD}=0V, I_{Q2}=500 mA
Output current limit	I_{Q2max}	1.5	–	–	A	V_{Q2}=2.4V
Line Regulation	$\Delta V_{Q2,Li}$	–	–	5	mV	4.75V≤V_{CC}≤5.25V; 10.8V≤V_{DD}≤13.2V
Load Regulation	$\Delta V_{Q2,Lo}$	–	–	10	mV	10mA≤I_{Q2}≤1.5A
Drop Voltage	V_{DRQ2}	–	–	1.7	V	I_{Q2}=1.2A[1)]
Output Q3						
Output voltage	V_{Q3}	3.20	3.30	3.40	V	1mA≤I_{Q3}≤1.2 A; 4.75V≤V_{CC}≤5.25V
Output voltage	V_{Q3}	2.90		3.40	V	V_{DD}=0V, I_{Q3}=500 mA
Output current limit	I_{Q3max}	1.5	–	–	A	V_{Q3}=3.1V
Line Regulation	$\Delta V_{Q3,Li}$	–	–	7	mV	4.75V≤V_{CC}≤5.25V; 10.8V≤V_{DD}≤13.2V
Load Regulation	$\Delta V_{Q3,Lo}$	–	–	15	mV	10mA≤I_{Q3}≤0.7A
Drop Voltage	V_{DRQ3}	–	–	1.5	V	I_{Q3}=1.2 A[1)]
Output Q8						
Output voltage	V_{Q8}	7.76	8.00	8.24	V	1 mA≤I_{Q8}≤200 mA; 10.8 V≤V_{DD}≤13.2 V
Output current limit	I_{Q8max}	250	–	–	mA	V_{Q8}=7.66 V
Line Regulation	$\Delta V_{Q8,Li}$	–	–	16	mV	4.75V≤V_{CC}≤5.25V; 10.8V≤V_{DD}≤13.2V
Load Regulation	$\Delta V_{Q8,Lo}$	–	–	32	mV	10 mA≤I_{Q8}≤200 mA
Drop Voltage	V_{DRQ8}	–	–	2.2	V	I_{Q8}=200 mA[1)]

Electrical Characteristics (cont'd)

V_{CC}=5.0V; V_{DD}=12.0V; 0 °C < T_j < 125 °C; unless otherwise specified; all voltages with respect to ground; positive current defined flowing into pin

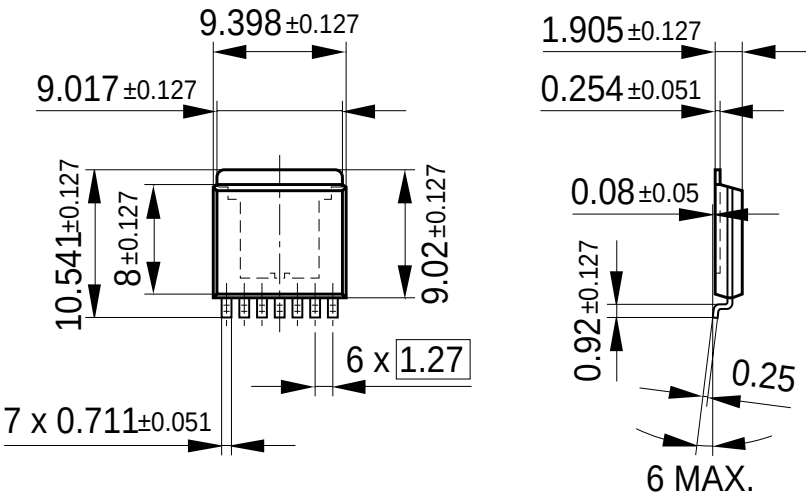
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Voltage						
Current Consumption	I_{CC}	–	1.75	2.6	mA	I_{Q2}=I_{Q3}=I_{Q8}=100µA
Current Consumption	I_{DD}	–	1.80	3.0	mA	I_{Q2}=I_{Q3}=I_{Q8}=100µA

[1] measured where the output voltage has dropped 1% below its nominal value

Application Information

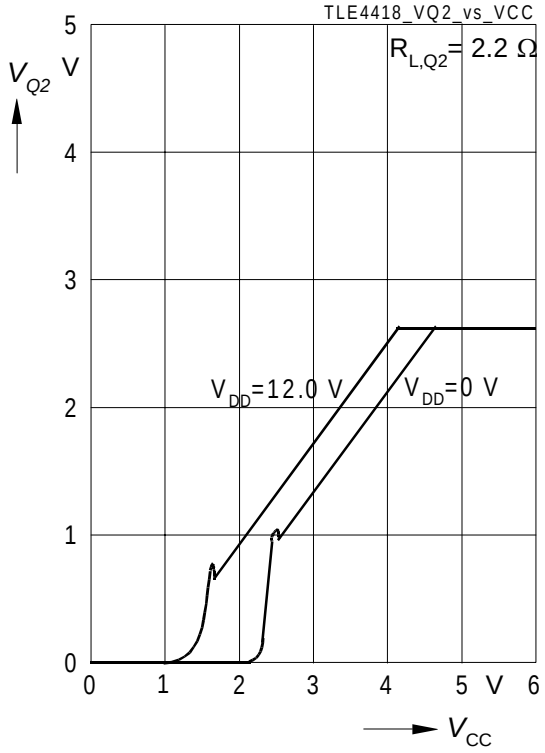
The output capacitors C_{Q2}, C_{Q3} and C_{Q8} are required with a capacitance of $C_{Q2/3/8}$≥2.2 µF and an ESR ≤ 4 Ω in order to maintain the stability of the regulation loop under all operating conditions. The output capacitors should be placed nearby the corresponding output voltage pin. For the Inputs V_{CC} and V_{DD} a ceramic capacitor in the range of 100 nF... 470 nF connected to GND close to the pins is needed in order compensate line influences.

P-SFMG-7-1
(SMD Package)

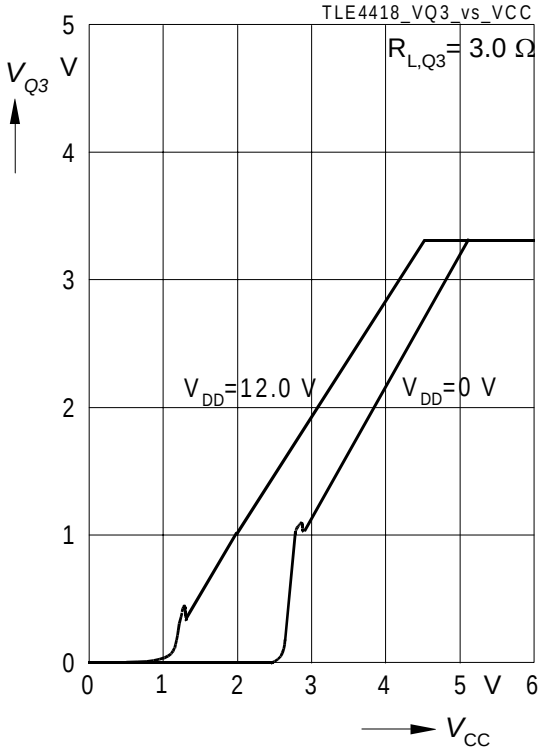


Typical Performance Characteristics

Output Voltage V_{Q2} versus Input Voltage V_{CC}



Output Voltage V_{Q3} versus Input Voltage V_{CC}



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